

N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVNL120A

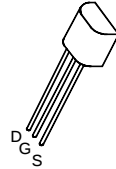
ISSUE 2 – MARCH 94

FEATURES

- * 200 Volt V_{DS}
- * $R_{DS(on)}=10\Omega$
- * Low threshold

APPLICATIONS

- * Telephone handsets



**E-Line
TO92 Compatible**

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	200	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	180	mA
Pulsed Drain Current	I_{DM}	2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	700	mW
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

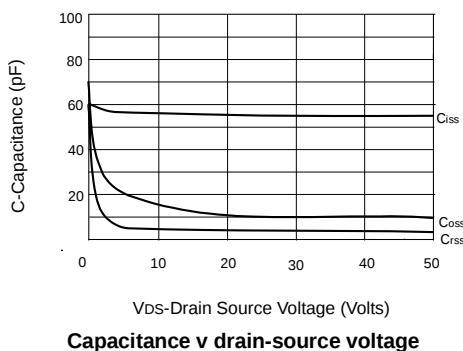
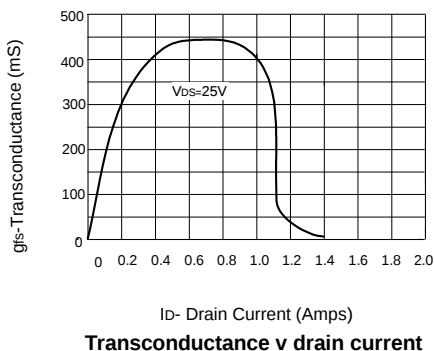
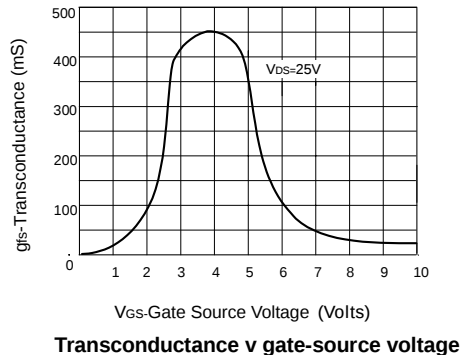
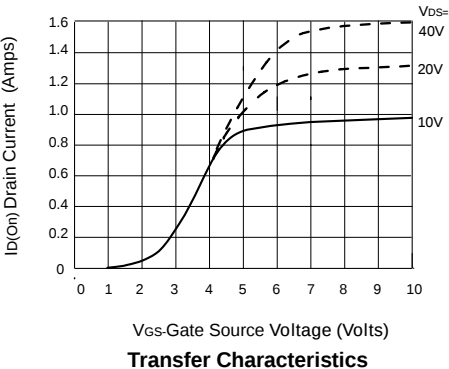
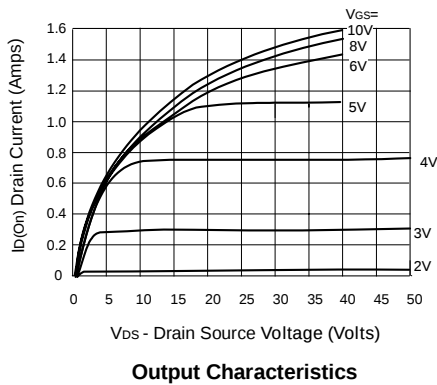
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	200		V	$I_D=1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.5	1.5	V	$I_D=1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}		10 100	μA μA	$V_{DS}=200V, V_{GS}=0$ $V_{DS}=160V, V_{GS}=0V, T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	500		mA	$V_{DS}=25V, V_{GS}=5V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		10 10	Ω Ω	$V_{GS}=5V, I_D=250mA$ $V_{GS}=3V, I_D=125mA$
Forward Transconductance (1)(2)	g_{fs}	200		mS	$V_{DS}=25V, I_D=250mA$
Input Capacitance (2)	C_{iss}		85	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	C_{oss}		20	pF	
Reverse Transfer Capacitance (2)	C_{rss}		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	$V_{DD}=25V, I_D=250mA$
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		20	ns	
Fall Time (2)(3)	t_f		12	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.

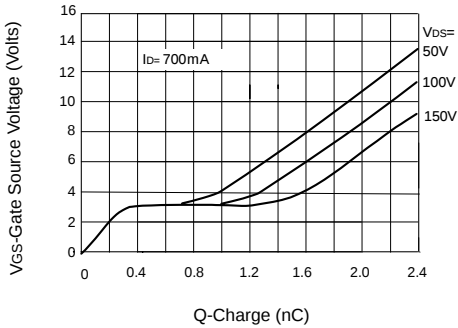
(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator

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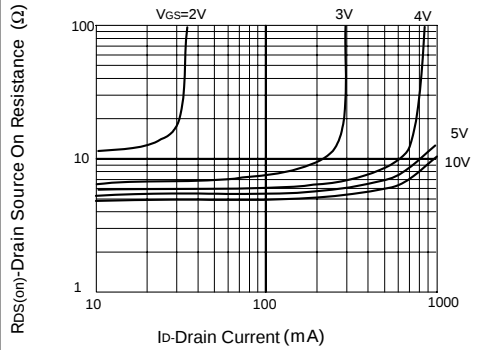
TYPICAL CHARACTERISTICS



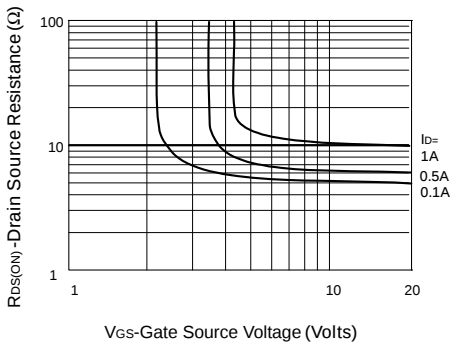
TYPICAL CHARACTERISTICS



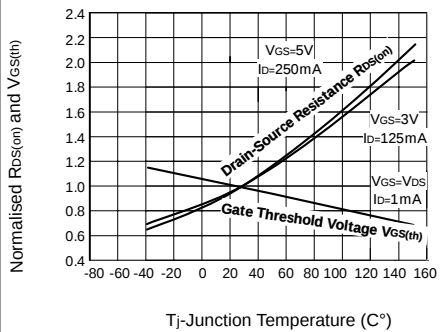
Gate charge v gate-source voltage



On-resistance v drain current



On-resistance vs gate-source voltage



Normalised $R_{DS(on)}$ and $V_{GS(th)}$ vs Temperature