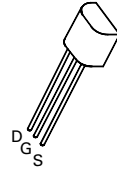


P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP4105A

ISSUE 2 – MARCH 94
FEATURES

- * 50 Volt V_{DS}
- * $R_{DS(on)}=10\Omega$
- * Low threshold



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-50	V
Continuous Drain Current at $T_{amb}=25^{\circ}\text{C}$	I_D	-175	mA
Pulsed Drain Current	I_{DM}	-520	mA
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}\text{C}$	P_{tot}	625	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-50		V	$I_D=-0.25\text{mA}$, $V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-0.8	-2.0	V	$I_D=-1\text{mA}$, $V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		10	nA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}		-15 -60 -100	μA μA nA	$V_{DS}=-50\text{V}$, $V_{GS}=0\text{V}$ $V_{DS}=-50\text{V}$, $V_{GS}=0\text{V}$, $T=125^{\circ}\text{C}(2)$ $V_{DS}=-25\text{V}$, $V_{GS}=0\text{V}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		10	Ω	$V_{GS}=-5\text{V}$, $I_D=-100\text{mA}$
Forward Transconductance (1)(2)	g_{fs}	50		mS	$V_{DS}=-25\text{V}$, $I_D=-100\text{mA}$
Input Capacitance (2)(4)	C_{iss}		40	pF	$V_{DS}=-25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$
Common Source Output Capacitance (2)(4)	C_{oss}		15	pF	
Reverse Transfer Capacitance (2)(4)	C_{rss}		6	pF	
Turn-On Delay Time (2)(3)(4)	$t_{d(on)}$		10	ns	$V_{DD}\approx -30\text{V}$, $I_D=-270\text{mA}$
Rise Time (2)(3)(4)	t_r		10	ns	
Turn-Off Delay Time (2)(3)(4)	$t_{d(off)}$		18	ns	
Fall Time (2)(3)(4)	t_f		25	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$

(2) Sample test.

(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator