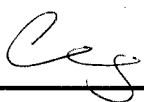


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SPECIFICATION
OF
LCD MODULE TYPE
ITEM NO.: BTHQ 42005VSS-02

DEPARTMENT	NAME	SIGNATURE	DATE
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**Specification
of
LCD Module Type
Item No.: BTHQ 42005VSS-02**

1. General Description

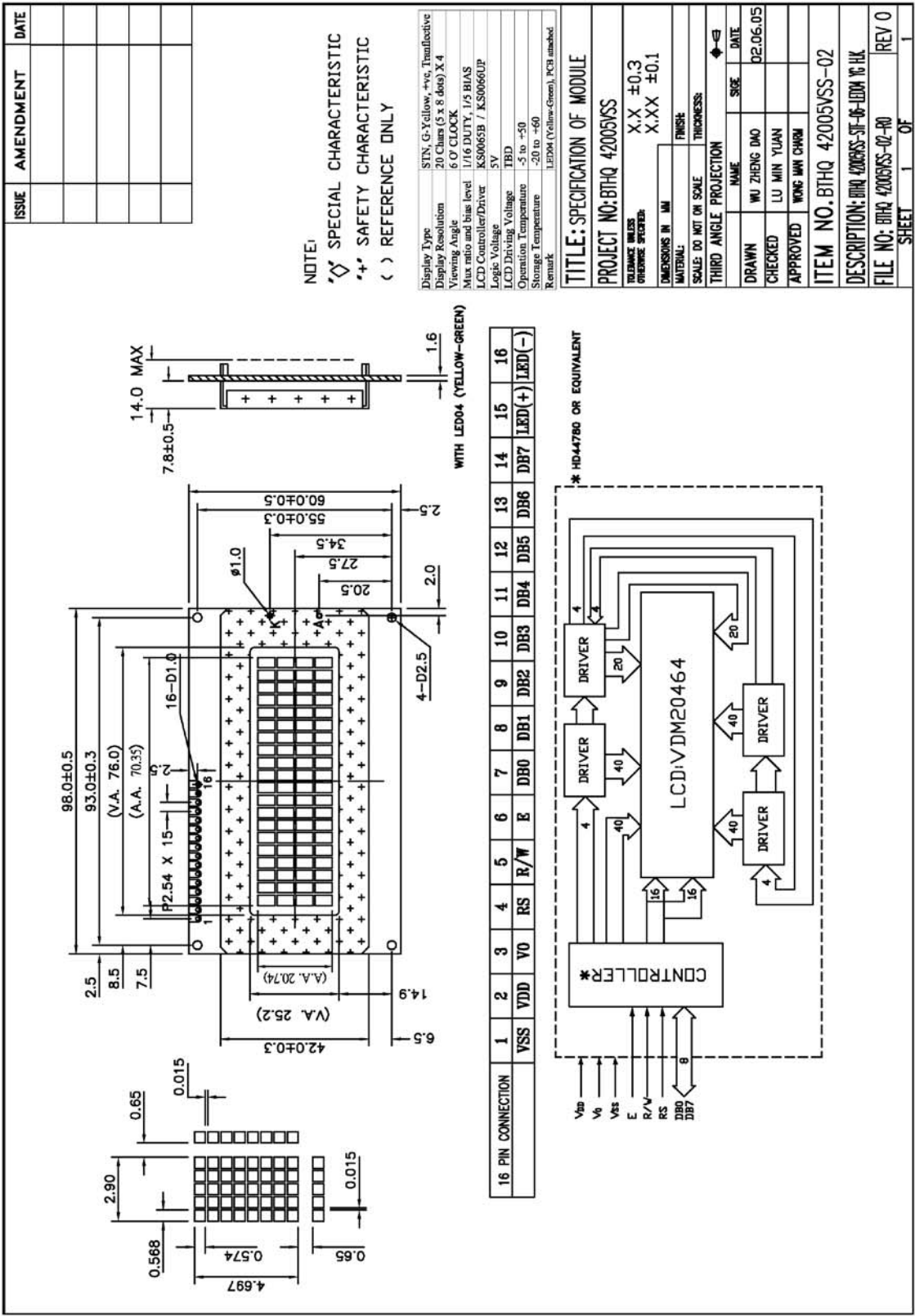
- 20 characters (5 x 8 dots) x 4 lines STN Positive G-Yellow Transflective LCD Character Module.
- Viewing Angle: 6 O'clock direction.
- Driving duty: 1/16 Duty, 1/5 bias.
- 'SAMSUNG' KS0066UP-10BCC (Die form) LCD Controller & Driver or equivalent.
- 'SAMSUNG' KS0065B-PCC (Die form) LCD Segment Drivers or equivalent.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	98.0(W) x 60.0(H) x 14.0 MAX.(D)	mm
Effective viewing area	76.0(W) x 25.2(H)	mm
Active area	70.35(W) x 20.74(H)	mm
Display format	20 characters x 4 lines	-
Character size	2.90(W) x 4.697(H) (5 x 8 dots)	mm
Character spacing	0.65(W) x 0.65(H)	mm
Character pitch	3.55(W) x 5.347(H)	mm
Dot size	0.568(W) x 0.574(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.583(W) x 0.589(H)	mm
Weight	Approx. 71	grams



3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic (+5.0V).
3	V0	Power supply for LCD driver.
4	RS	Register Select Input: "High" for Data register (for read and write). "Low" for Instruction register (for write), Busy flag, address counter (for read).
5	R/W	Read/Write signal: 'High' for Read mode. 'Low' for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15 or A	LED(+)	Anode of LED Backlight
16 or K	LED(-)	Cathode of LED Backlight

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD-VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD =VDD-V0	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-5°C	+50°C	-20°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD -VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD –V0	VDD = 5V, Note (1)	4.1	4.5	4.9	V
Input signal voltage for E,DB0-DB7,R/W,RS.	V _{IH}	”H” level	2.2	-	VDD	V
	V _{IL}	” L” level	-0.3	-	0.6	V
Supply Current (Logic & LCD)	IDD	Character mode, VDD=5V, Note 1	-	1.0	1.5	mA
		Checker board mode, VDD=5V, Note 1	-	1.2	1.8	mA
Supply Current (LCD)	I0	Character mode, VDD=5V, Note 1	-	0.2	0.3	mA
		Checker board mode, VDD=5V, Note 1	-	0.2	0.3	mA
Supply voltage of yellow-green LED04 backlight	VLED	Forward current =240mA Number of LED dies =2x24 =48.	3.9	4.1	4.3	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At $T_a = -5\text{ }^{\circ}\text{C}$ To $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Refer to [Fig. 2](#), the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit
E Cycle Time	t_c	500	-	ns
E Rise/Fall Time	t_R, t_F	-	20	ns
E Pulse Width(high, low)	t_W	230	-	ns
R/W and RS Setup Time	t_{SU1}	40	-	ns
R/W and RS Hold Time	t_{H1}	10	-	ns
Data Set-up Time	t_{SU2}	80	-	ns
Data Hold Time	t_{H2}	10	-	ns

Refer to [Fig. 3](#), the bus timing diagram for read mode.

Table 7

Parameter	Symbol	Min.	Max.	Unit
E Cycle Time	t_c	500	-	ns
E Rise/Fall Time	t_R, t_F	-	20	ns
E Pulse Width(high, low)	t_W	230	-	ns
R/W and RS Setup Time	t_{SU}	40	-	ns
R/W and RS Hold Time	t_H	10	-	ns
Data Output Delay Time	t_D	-	120	ns
Data Hold Time	t_{DH}	5	-	ns

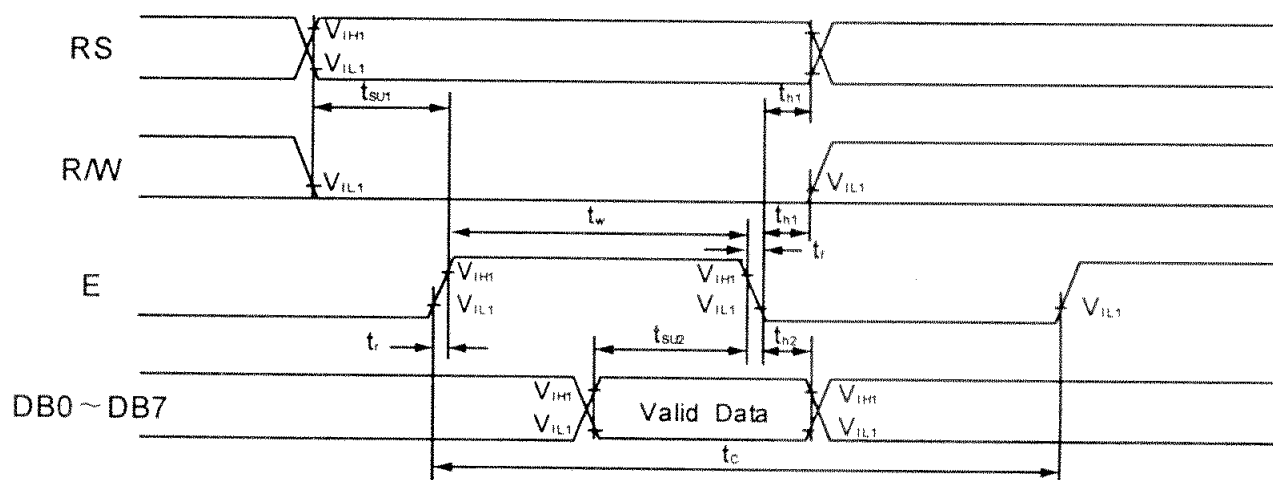


Figure 2: Write Mode Timing Diagram

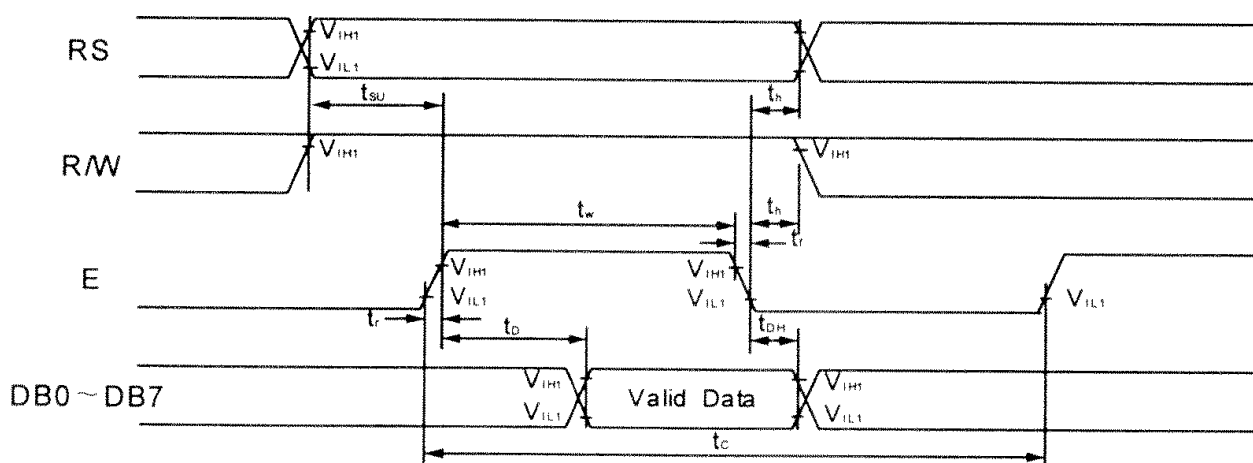


Figure 3: Read Mode Timing Diagram

5.3 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

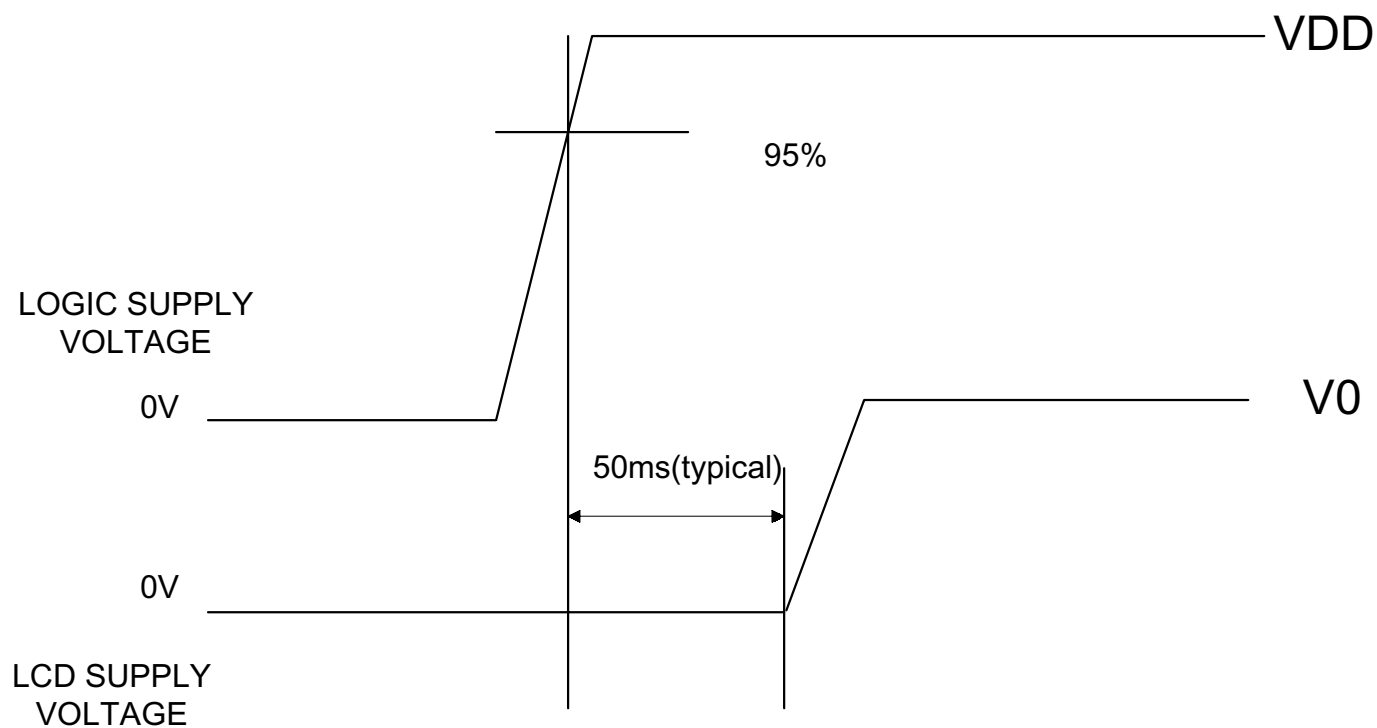


Figure 4: Timing Diagram of VDD Against V0.

Upper 4bit Lower 4bit	LLLL	LL LH	LL HL	LL HH	LH LL	LH LH	LH HL	LH HH	HL LL	HL LH	HL HL	HL HH	HH LL	HH LH	HH HL	HH HH
LLLL	CG RAM (1)															
LL LH	(2)															
LL HL	(3)															
LL HH	(4)															
LH LL	(5)															
LH LH	(6)															
LH HL	(7)															
LH HH	(8)															
HL LL	(1)															
HL LH	(2)															
HL HL	(3)															
HL HH	(4)															
HH LL	(5)															
HH LH	(6)															
HH HL	(7)															
HH HH	(8)															