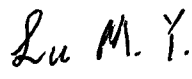


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VL-FS-BTHQ 21603VSS-01 REV.B
(BTHQ 21603V-SRE-CONN.)

DOCUMENT TITLE:
SPECIFICATION
OF
LCD MODULE TYPE
ITEM NO.: BTHQ 21603VSS-01

APPROVALS:

EFFECTIVE DATE

DEPARTMENT	NAME	SIGNATURE	DATE
MARKETING (TECHNICAL SUPPORT)	PHILIP CHENG		2002.1.15
LCM(DSIGN)	M.Y.LU		2002.1.15
MARKETING (TECHNICAL SUPPORT)	CYRUS CHEUNG		2002/1/15

Page No.	1	2	3	4	5	6	7	8	9	10	11	12
Rev. No.	B	B	A	B	B	A	A	A	A	A	A	A

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A B	2002.01.14	Items 1 to 3 were updated: 1.) (Page 4, point 1) “(CON-IL-402)” was added. 2.)(Page 4, point 2) “(Excluded connector)” was added. 3.)(Page 5, Fig. 1) Outline drawing was updated.	PHILIP CHENG	M.Y.LU

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**Specification
of
LCD Module Type
Item No.: BTHQ 21603VSS-01**

1. General Description

- 16 characters (5x8 dots) x 2 lines STN Positive Yellow Reflective Dot Matrix LCD module.
- Viewing Angle: 6 O'clock direction.
- Driving scheme: 1/16 Duty, 1/5 bias.
- 'NOVATEK' NT3881DH-01/AI (Die form) LCD Controller and Driver or equivalent
- 'SAMSUNG' KS0065B-PCC (Die form) or equivalent 40-Channel Segment/Common Driver for Dot Matrix LCD.
- Connector: 16 pins ZIF SMD connector (CON-IL-402).

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

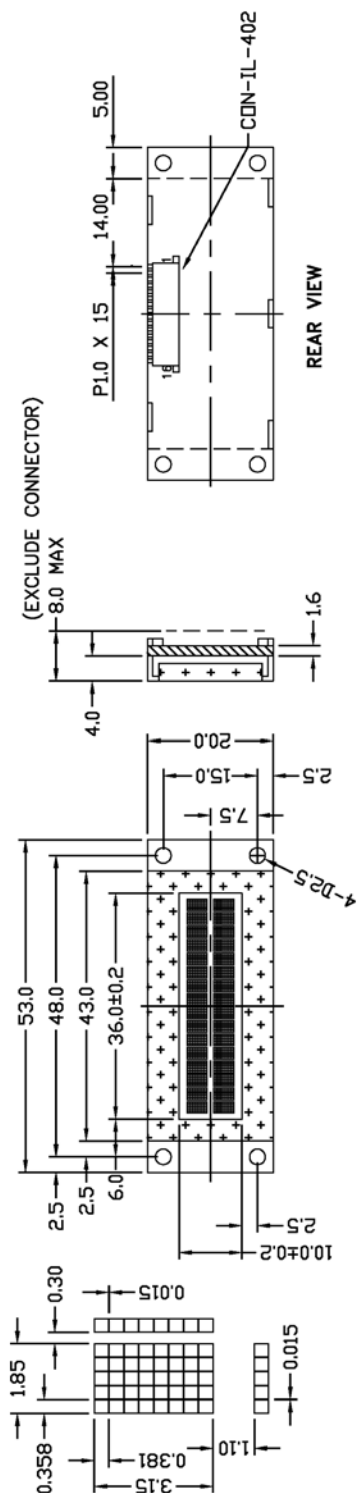
Parameter	Specifications	Unit
Outline dimensions	53.0(W) x 20.0(H) x 8.0 MAX.(D) (Excluded connector)	mm
Effective viewing area	36.0(W) x 10.0(H)	mm
Display format	16 characters x 2 lines	-
Character size	1.85(W) x 3.15(H) (5 x 8 dots)	mm
Character spacing	0.30(W) x 1.10(H)	mm
Character pitch	2.15(W) x 4.25(H)	mm
Dot size	0.358(W) x 0.381(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.373(W) x 0.396(H)	mm
Weight:	TBD	grams

Supplied by:

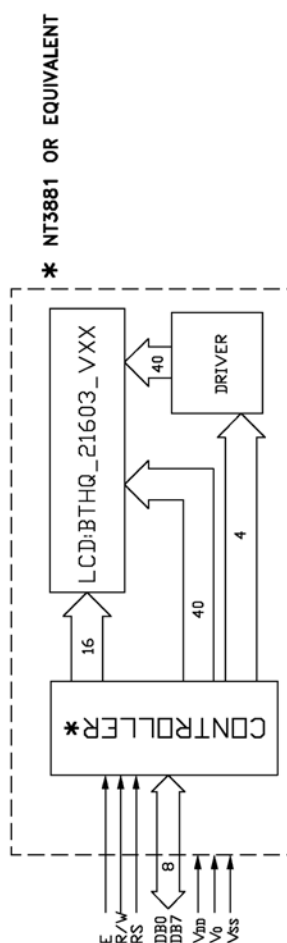
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[illegible]

16 PIN CONNECTION		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	VDD	V0	RS	R/W	E	D0	D1	D2	D3	D4	D5	D6	D7	LED(+)	LED(-)		



TITLE: SPECIFICATION OF MODULE	
PROJECT NO: BTHQ 21603VSS	
TOLERANCE UNLESS OTHERWISE SPECIFIED: X:X ± 0.3 X:X X ± 0.1	
DIMENSIONS IN MM	FINISH
MATERIAL:	THICKNESS:
SCALE: DO NOT ON SCALE	
THIRD ANGLE PROJECTION	
NAME	SIGN
DATE	
DRAWN	HE ZUOBING
CHECKED	WONG M.C
APPROVED	ANDY LEUNG
ITEM NO. BTHQ 21603VSS-01	
DESCRIPTION: BT 21603VSS-SRE-HQ-CUNLN	
FILE NO: MODULE BT21603V-HQ REV 0	
SHEET NO.	

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings($T_a = 25^\circ\text{C}$)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+13.5	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for $T_a \leq 40^\circ\text{C}$ < 95% RH for $T_a > 40^\circ\text{C}$				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: $981 \text{ m/s}^2 = 100\text{g}$ Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

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4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	VSS	Ground(0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: "High" for Data register (for read and write) "Low" for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: "High" for Read mode. "Low" for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15	LED(+)	Anode of LED backlight
16	LED(-)	Cathode of LED backlight

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4.2 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.00	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD =5.0V, Note1.	4.0	4.5	5.0	V
Input signal voltage 1 for E,DB0-DB7,R/W,RS.	V _{IH1}	”H” level	2.2	-	VDD	V
	V _{IL1}	” L” level	-0.3	-	0.8	V
Input signal voltage 2 for OSC1.	V _{IH2}	” H” level	VDD -1.0	-	VDD	V
	V _{IL2}	” L” level	VSS	-	1.0	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.3	2.0	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.2	0.3	mA

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

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4.3 Timing Specifications

At $T_a = 0\text{ }^{\circ}\text{C}$ To $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +5V \pm 5\%$, $V_{SS} = 0V$.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	t_{CYCE}	500	-	ns	
Enable "High" level pulse width	t_{WHE}	300	-	ns	
Enable rise time	t_{RE}	-	25	ns	
Enable fall time	t_{FE}	-	25	ns	
RS, R/W set-up time	t_{AS}	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	t_{AH}	10	-	ns	
Data output delay	t_{DS}	100	-	ns	
Data hold time	t_{DHR}	10	-	ns	

Refer to Fig. 3, the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	t_{CYCE}	500	-	ns	
Enable "High" level pulse width	t_{WHE}	300	-	ns	
Enable rise time	t_{RE}	-	25	ns	
Enable fall time	t_{FE}	-	25	ns	
RS, R/W set-up time	t_{AS}	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	t_{AH}	10	-	ns	
Read data output delay	t_{RD}	-	190	ns	
Read data hold time	t_{DHR}	20	-	ns	

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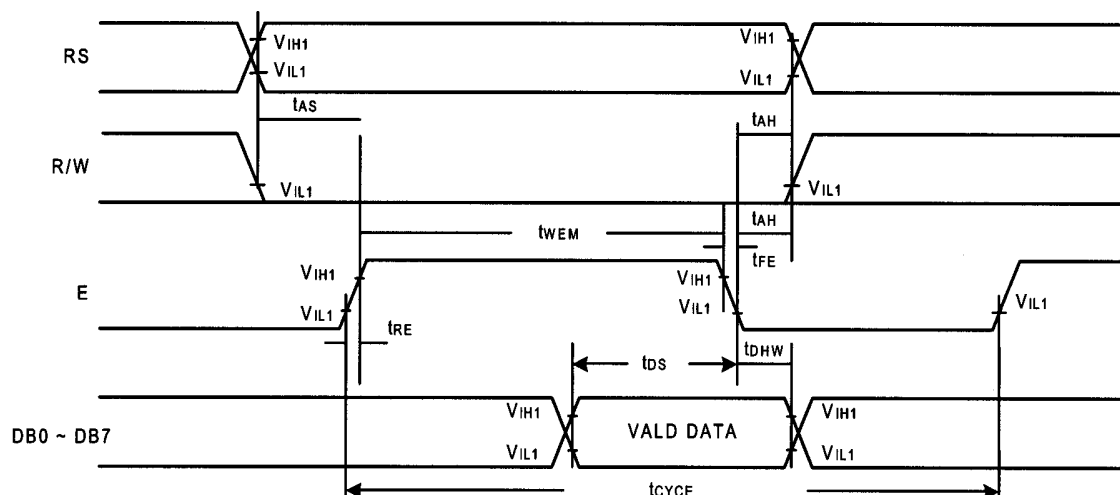


Figure 2: Bus write operation sequence (Writing data from MPU to NT3881).

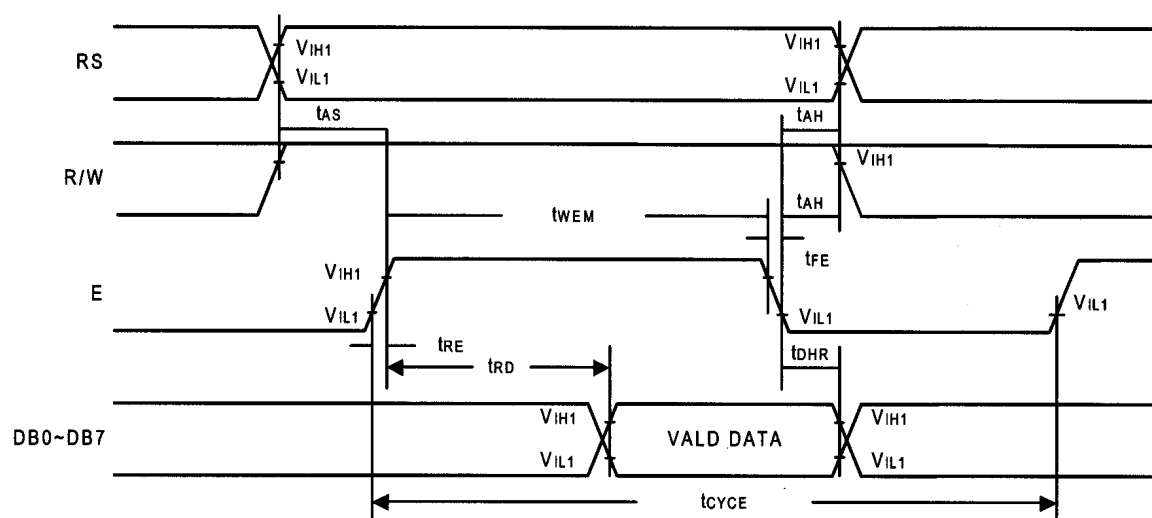


Figure 3: Bus read operation sequence (Reading out data from NT3881 to MPU).

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4.4 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

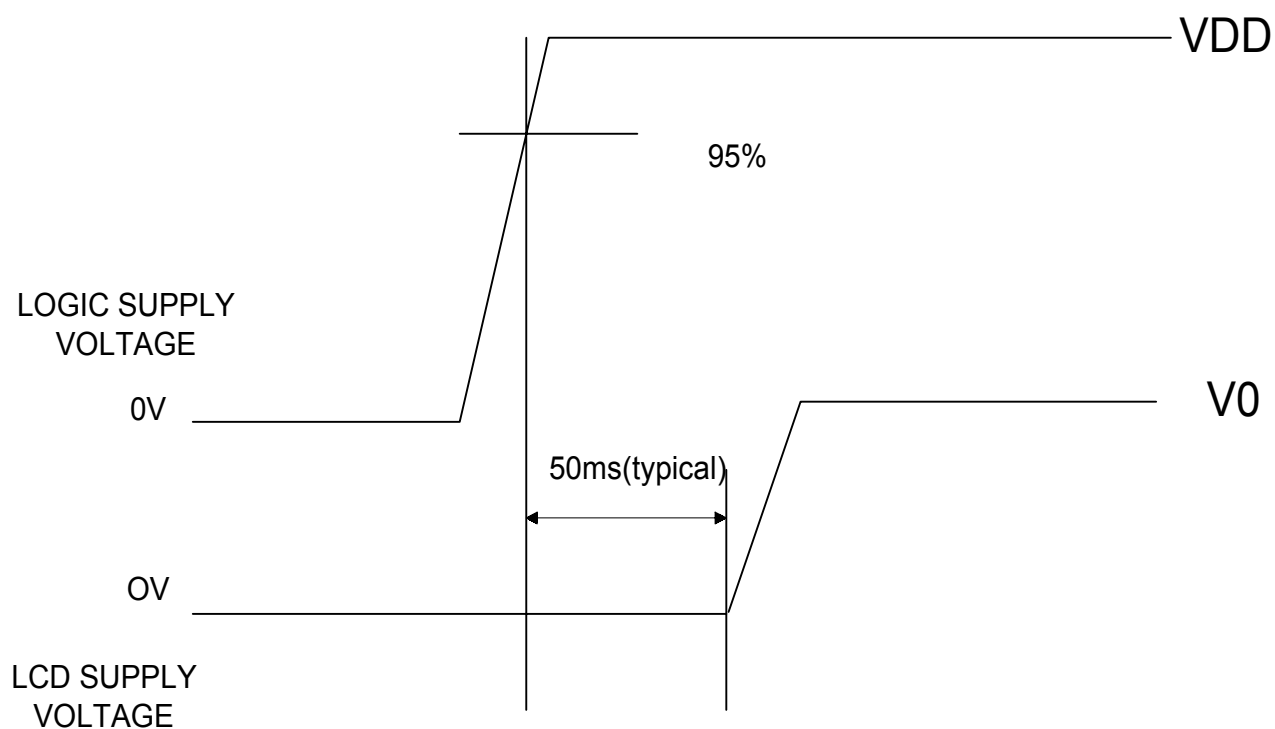


Figure 4: Timing diagram of VDD against V0.

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4.5 Correspondence between Character Codes and Character Patterns (NOVATEK Standard NT3881D-01)

		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)			0	a	P	`	P				一	夕	三	α	p
	1	CG RAM (2)		!	1	A	Q	a	q			□	ア	チ	△	ä	q
	2	CG RAM (3)		"	2	B	R	b	r			「	イ	ウ	×	β	θ
	3	CG RAM (4)		#	3	C	S	c	s			」	ウ	テ	〒	ε	ω
	4	CG RAM (5)		\$	4	D	T	d	t			、	エ	ト	ト	μ	Ω
	5	CG RAM (6)		%	5	E	U	e	u			・	オ	ナ	1	δ	Ü
	6	CG RAM (7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
	7	CG RAM (8)		'	7	G	W	g	w			ア	キ	ヌ	ラ	g	π
	8	CG RAM (1)		(	8	H	X	h	x			イ	ク	ネ	リ	フ	Σ
	9	CG RAM (2)		)	9	I	Y	i	y			ウ	ケ	ル	ル	リ	Y
	A	CG RAM (3)		*	:	J	Z	j	z			エ	コ	ン	レ	j	〒
	B	CG RAM (4)		+	;	K	Ł	k	ł			オ	サ	ヒ	ロ	*	斤
	C	CG RAM (5)		,	<	L	¶	l	¶			カ	シ	フ	ワ	¢	円
	D	CG RAM (6)		—	=	M	Ј	m	Ј			ユ	ズ	へ	ン	モ	÷
	E	CG RAM (7)		„	>	N	^	n	→			ヨ	セ	ホ	°	ñ	
	F	CG RAM (8)		/	?	O	_	o	+			ッ	リ	マ	°	ö	

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