

IRLR8103VPbF

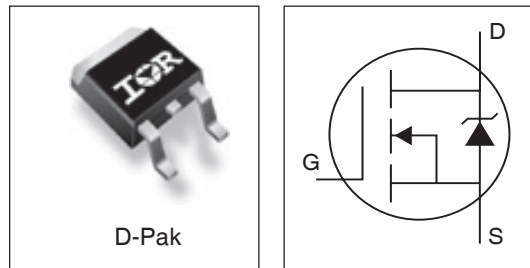
- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications
- 100% R_G Tested
- Lead-Free

Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRLR8103V has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and C_{dv}/dt -induced turn-on immunity. The IRLR8103V offers an extremely low combination of Q_{sw} & $R_{DS(on)}$ for reduced losses in both control and synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.



DEVICE CHARACTERISTICS^⑤

	IRLR8103V
$R_{DS(on)}$	7.9 m Ω
Q_G	27 nC
Q_{SW}	12 nC
Q_{OSS}	29nC

Absolute Maximum Ratings

Parameter	Symbol	IRLR8103V	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain or Source Current	I_D	91	A
($V_{GS} > 10V$)		63	
Pulsed Drain Current ^①	I_{DM}	363	
Power Dissipation ^③	P_D	115	W
		60	
Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$
Continuous Source Current (Body Diode)	I_S	91	A
Pulsed Source Current ^①	I_{SM}	363	

Thermal Resistance

Parameter	Symbol	Typ.	Max.	Units
Maximum Junction-to-Ambient ^{③⑥}	$R_{\theta JA}$	—	50	$^{\circ}C/W$
Maximum Junction-to-Case ^⑥	$R_{\theta JC}$	—	1.09	

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	6.9	9.0	$m\Omega$	$V_{GS} = 10V, I_D = 15A$ ②
		—	7.9	10.5		$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-to-Source Leakage Current	I_{DSS}	—	—	50	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	20	μA	$V_{DS} = 24V, V_{GS} = 0$
		—	—	100	μA	$V_{DS} = 24V, V_{GS} = 0, T_J = 100^\circ C$
Gate-Source Leakage Current	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V$
Total Gate Charge, Control FET	Q_G	—	27	—	nC	$V_{GS} = 5V, I_D = 15A, V_{DS} = 16V$
Total Gate Charge, Synch FET	Q_G	—	23	—		$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}	—	4.7	—		$V_{DS} = 16V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}	—	2.0	—		
Gate to Drain Charge	Q_{GD}	—	9.7	—		
Switch Charge ($Q_{gs2} + Q_{gd}$)	Q_{SW}	—	12	—		
Output Charge	Q_{OSS}	—	29	—		$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	R_G	0.8	—	3.1	Ω	
Turn-On Delay Time	$t_{d(on)}$	—	10	—	ns	$V_{DD} = 16V$ $I_D = 15A$ $V_{GS} = 5.0V$ Clamped Inductive Load
Rise Time	t_r	—	9	—		
Turn-Off Delay Time	$t_{d(off)}$	—	24	—		
Fall Time	t_f	—	18	—		
Input Capacitance	C_{iss}	—	2672	—	pF	$V_{GS} = 16V, V_{GS}=0$
Output Capacitance	C_{oss}	—	1064	—		
Reverse Transfer Capacitance	C_{rss}	—	109	—		

Source-Drain Rating & Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Diode Forward Voltage	V_{SD}	—	0.9	1.3	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge ④	Q_{rr}	—	103	—	nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_F = 15A$
Reverse Recovery Charge (with Parallel Schottky) ④	$Q_{rr(s)}$	—	96	—	nC	$di/dt = 700A/\mu s$, (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_F = 15A$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
 ③ When mounted on 1 inch square copper board, $t < 10$ sec.
 ④ Typ = measured - Q_{oss}
 ⑤ Typical values of $R_{DS(on)}$ measured at $V_{GS} = 4.5V$, Q_G , Q_{SW} and Q_{OSS} measured at $V_{GS} = 5.0V$, $I_F = 15A$.

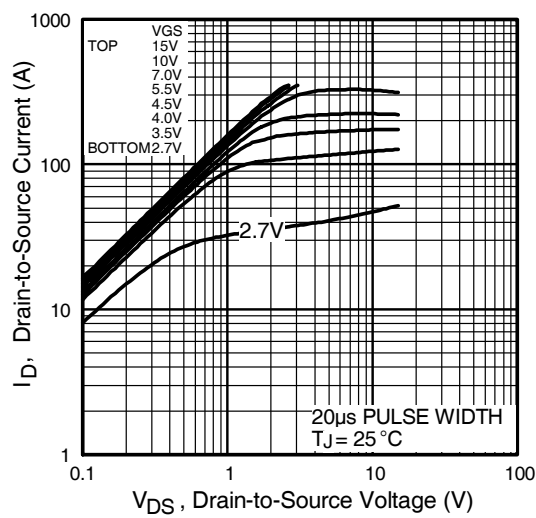


Fig 1. Typical Output Characteristics

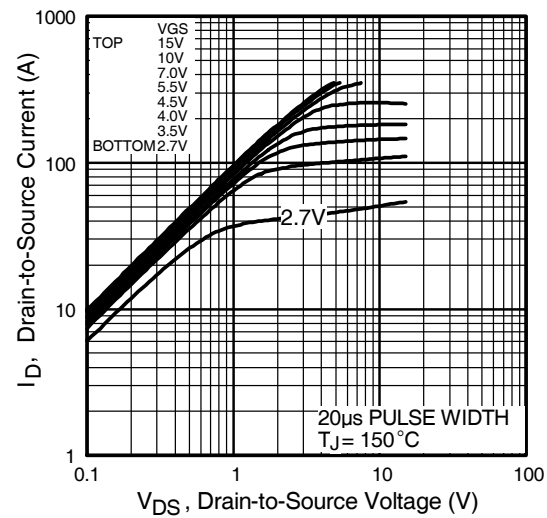


Fig 2. Typical Output Characteristics

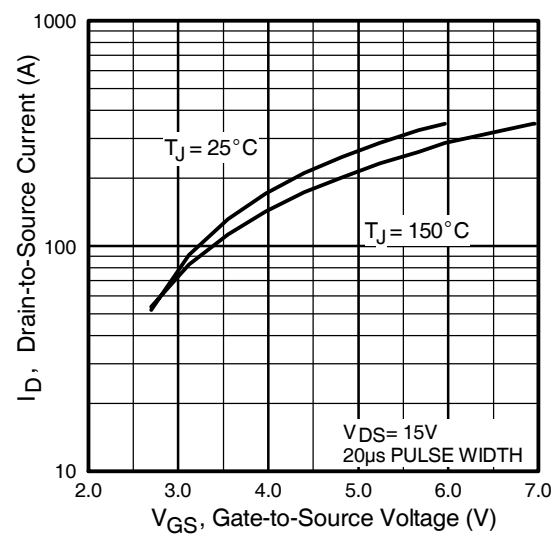


Fig 3. Typical Transfer Characteristics

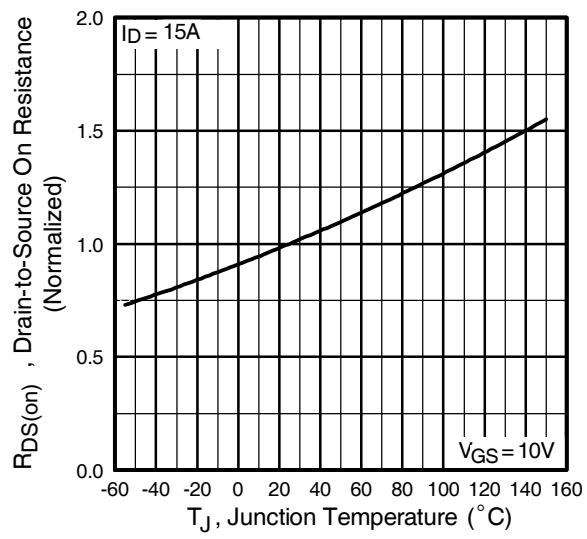
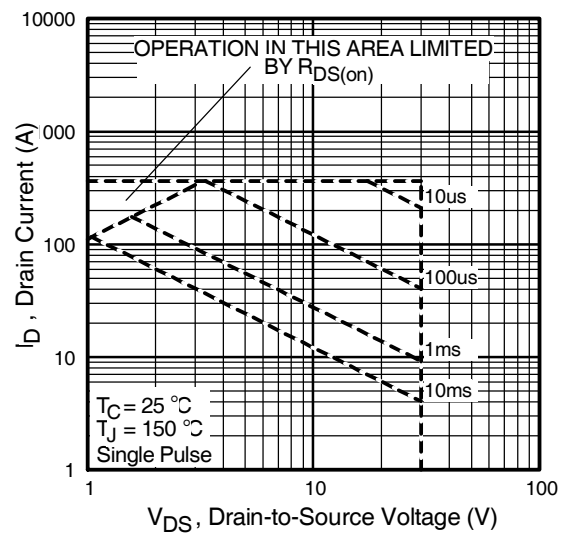
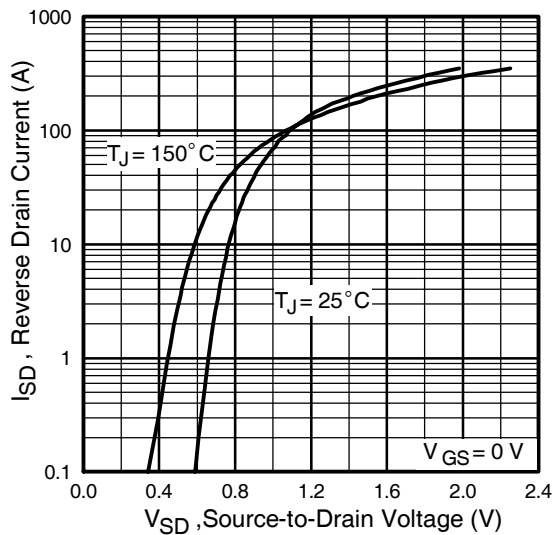
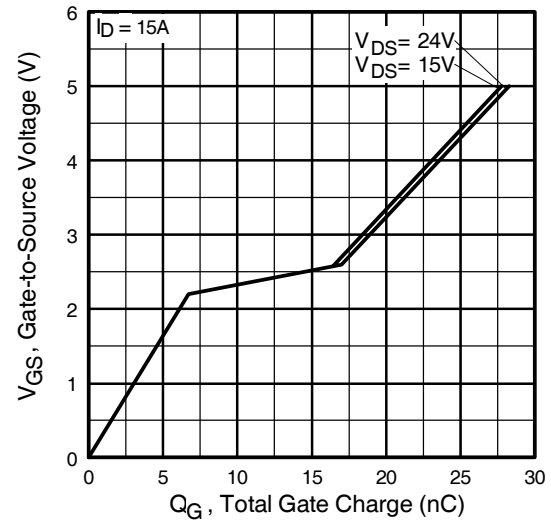
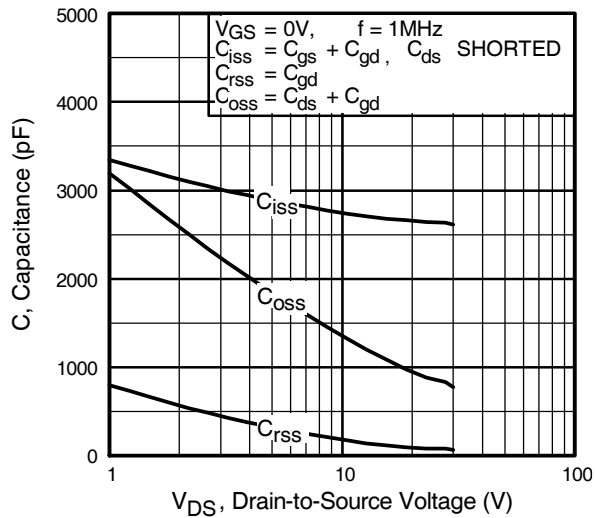


Fig 4. Normalized On-Resistance Vs. Temperature



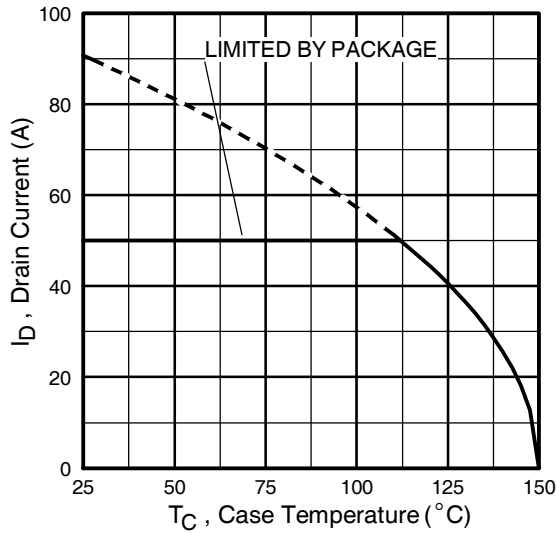


Fig 9. Maximum Drain Current Vs. Case Temperature

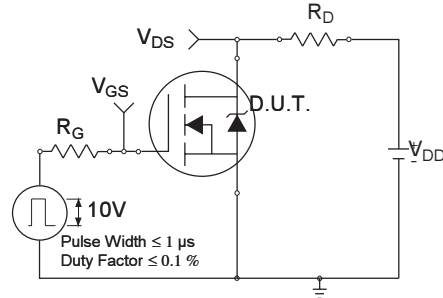


Fig 10a. Switching Time Test Circuit

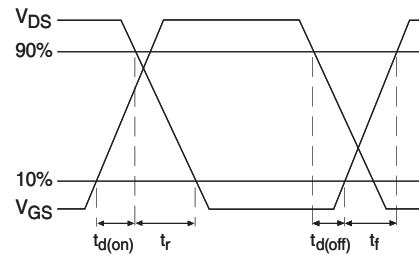


Fig 10b. Switching Time Waveforms

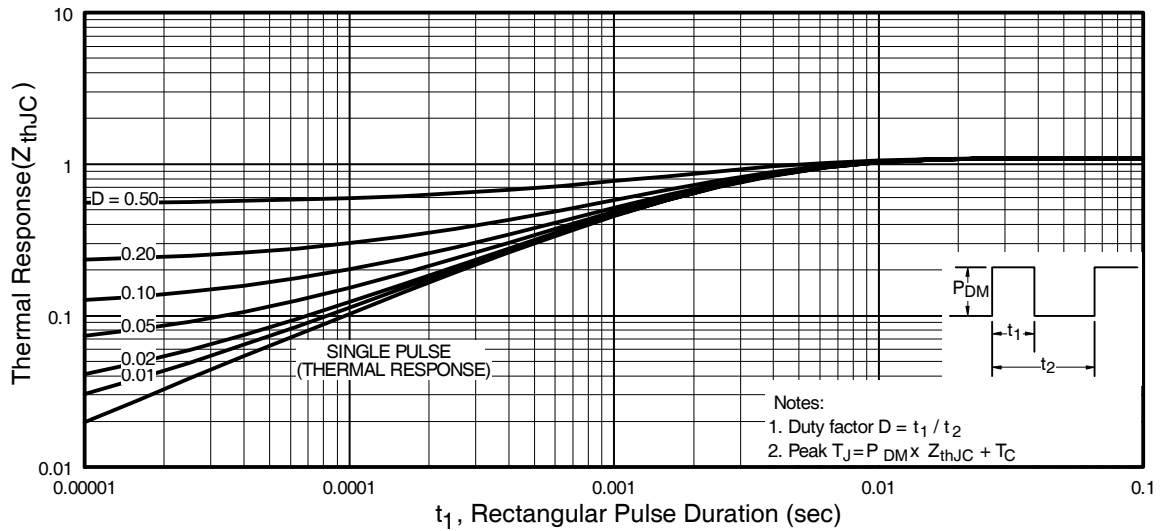


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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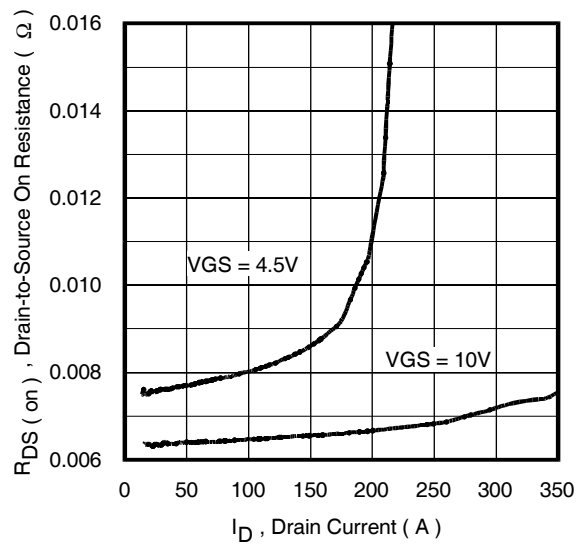


Fig 12. On-Resistance Vs. Drain Current

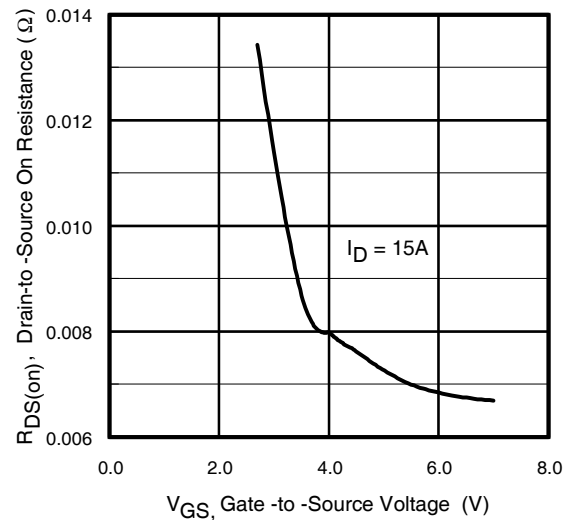


Fig 13. On-Resistance Vs. Gate Voltage

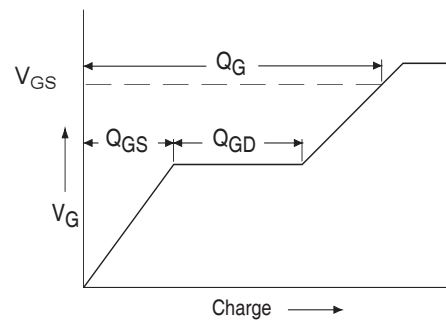
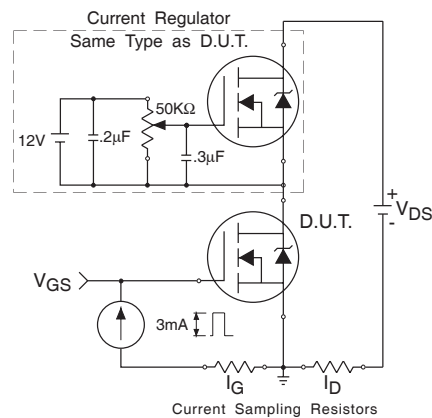
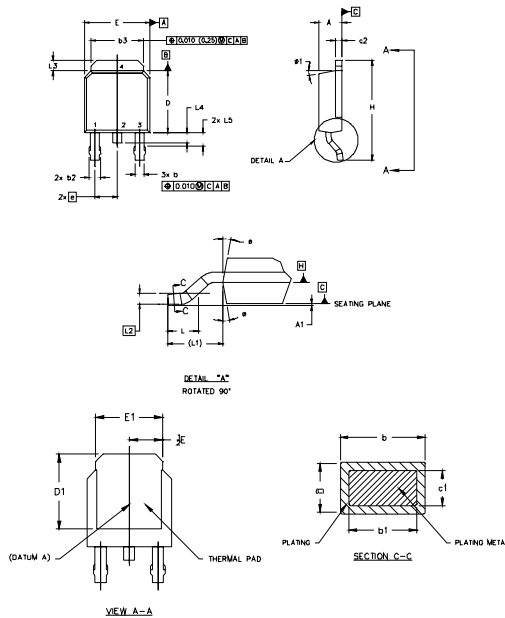


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5.
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 (0.127) AND .010 (0.254) FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.13	0.15	.005	.006	
b	0.84	0.89	.033	.035	5
b1	0.84	0.79	.033	.030	5
b2	0.76	1.14	.030	.045	
b3	4.83	5.46	.189	.215	
c	0.48	0.81	.018	.032	5
c1	0.41	0.56	.016	.022	5
c2	0.40	0.89	.016	.035	5
D	6.97	8.22	.275	.324	6
D1	6.21	-	.245	-	4
E	6.35	6.13	.250	.243	6
E1	4.32	-	.170	-	4
E	2.29	-	.090	WSC	
H	6.40	10.41	.250	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.	-	.108 REF.	-	
L2	0.89 WSC	-	.035 WSC	-	
L3	0.88	1.27	.035	.050	
L4	1.14	1.52	.045	.060	
L5	1.14	1.52	.045	.060	
#	0"	10"	0"	10"	
#1	0"	10"	0"	10"	

LEAD ASSIGNMENTS

HEXMET

1- GATE
2- DRAIN
3- SOURCE
4- DRAIN

IGBTs, GSPACK

1- GATE
2- COLLECTOR
3- EMITTER
4- COLLECTOR

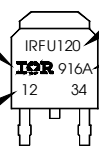
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRRF120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

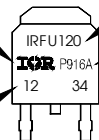


PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

OR

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE



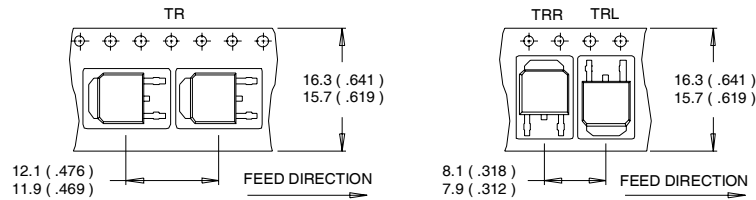
PART NUMBER
DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 16
A = ASSEMBLY SITE CODE

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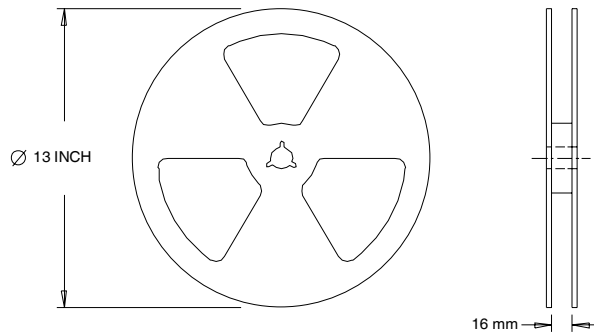
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
IR Rectifier

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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.12/04

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>