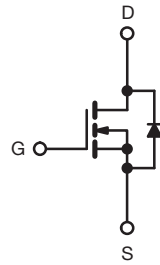
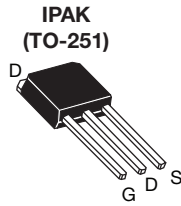


## Power MOSFET



N-Channel MOSFET

### FEATURES

- Straight lead
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### PRODUCT SUMMARY

$V_{DS}$ (V)	100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.54
$Q_g$ (Max.) (nC)	8.3	
$Q_{gs}$ (nC)	2.3	
$Q_{gd}$ (nC)	3.8	
Configuration	Single	

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

### ORDERING INFORMATION

Package	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFU110-GE3
Lead (Pb)-free	IRFU110PbF

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

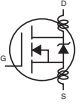

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	100	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed drain current <sup>a</sup>	$I_{DM}$	17		
Linear derating factor		0.2	W/ $^\circ\text{C}$	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	75	mJ	
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	4.3	A	
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	2.5	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	25	W
Peak diode recovery dV/dt <sup>c</sup>		dV/dt	5.5	V/ns
Operating junction and storage temperature range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	for 10 s		300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 8.1\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 4.3\text{ A}$  (see fig. 12)
- $I_{SD} \leq 5.6\text{ A}$ ,  $dI/dt \leq 75\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	5.0		

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.63	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 0.90\text{ A}^b$	-	-	0.54	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 0.90\text{ A}$		1.1	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5		-	180	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	81	-	
Reverse Transfer Capacitance	$C_{rss}$			-	15	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 5.6\text{ A}, V_{DS} = 80\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	8.3	nC
Gate-Source Charge	$Q_{gs}$			-	-	2.3	
Gate-Drain Charge	$Q_{gd}$			-	-	3.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 5.6\text{ A},$ $R_g = 24\text{ }\Omega, R_D = 8.4\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	6.9	-	ns
Rise Time	$t_r$			-	16	-	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-	
Fall Time	$t_f$			-	9.4	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	$L_S$			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	12	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 1.5\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 5.6\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	100	200	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.44	0.88	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

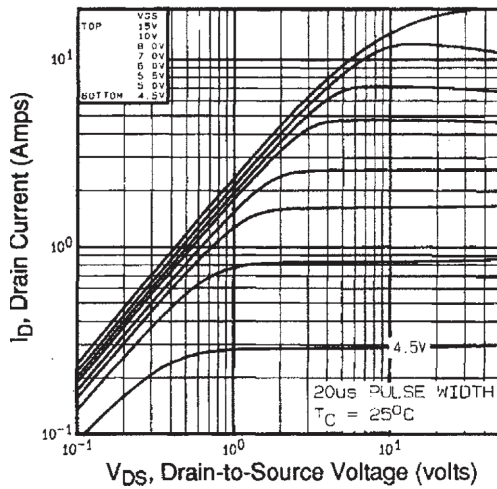


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

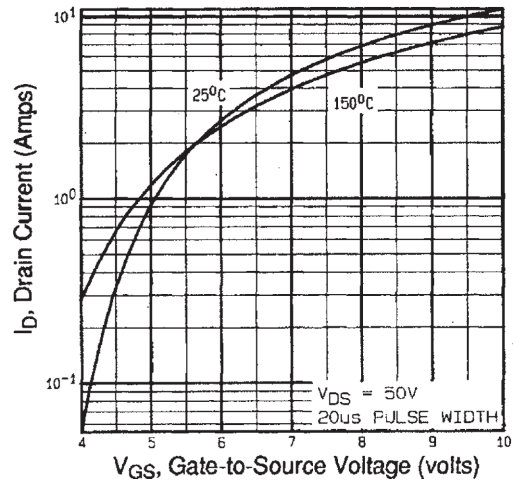


Fig. 2 - Typical Transfer Characteristics

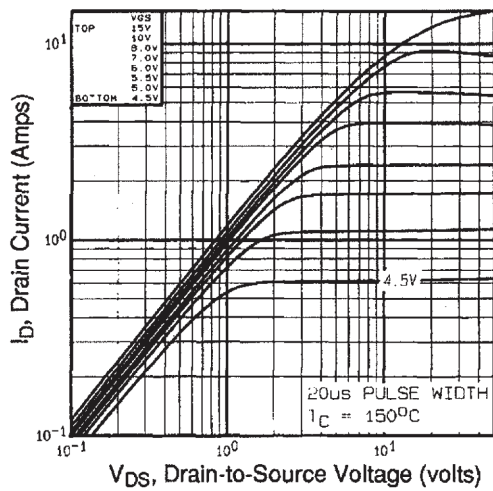


Fig. 1 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

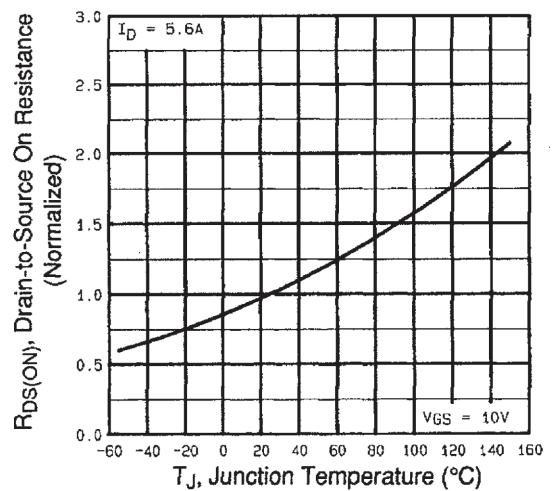


Fig. 3 - Normalized On-Resistance vs. Temperature

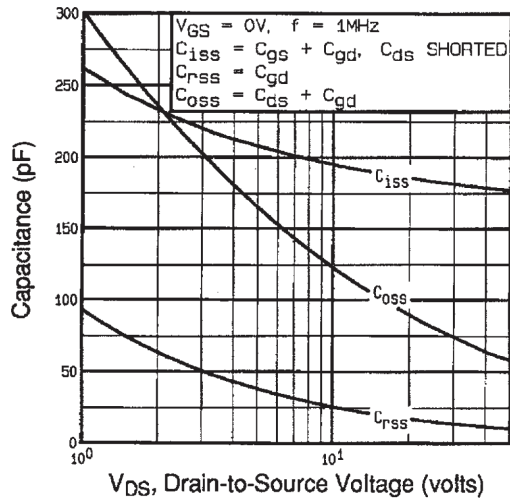


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

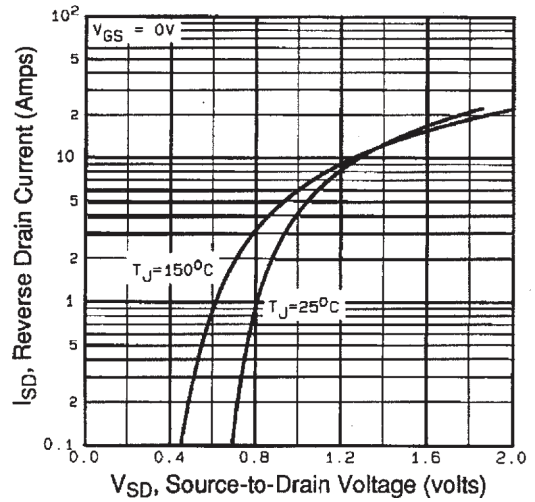


Fig. 6 - Typical Source-Drain Diode Forward Voltage

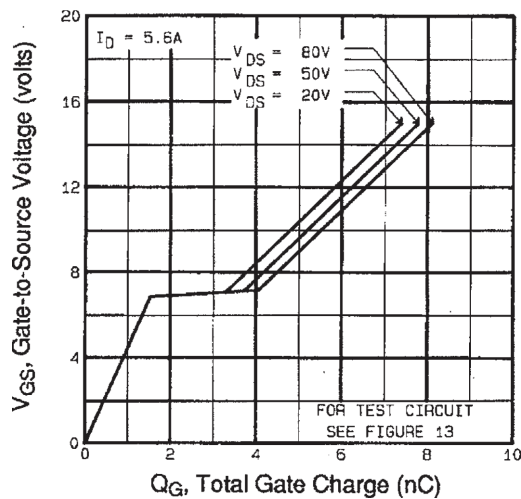


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

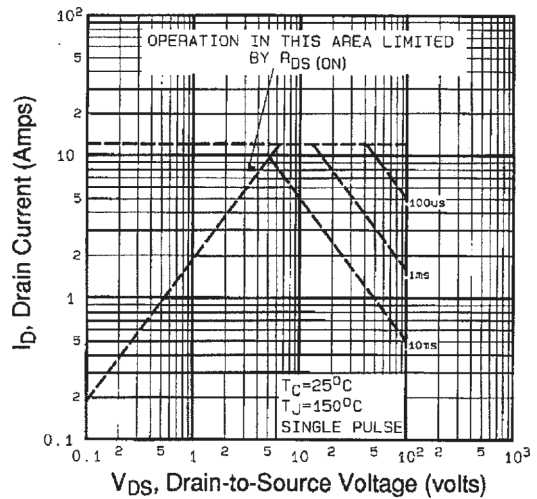


Fig. 7 - Maximum Safe Operating Area

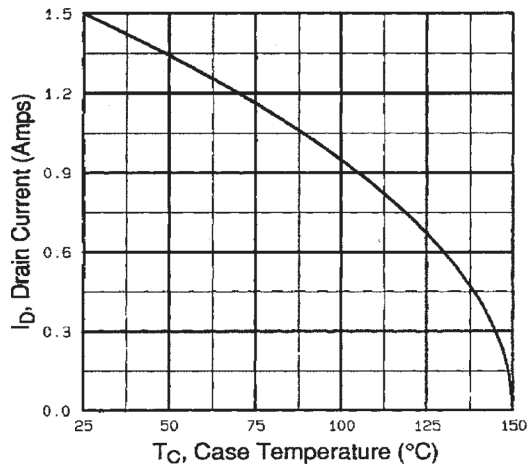


Fig. 8 - Maximum Drain Current vs. Case Temperature

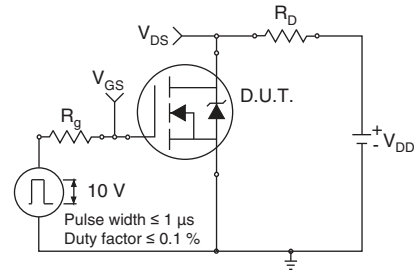


Fig. 10a - Switching Time Test Circuit

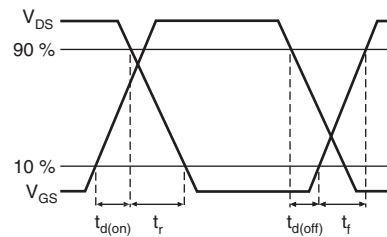


Fig. 10b - Switching Time Waveforms

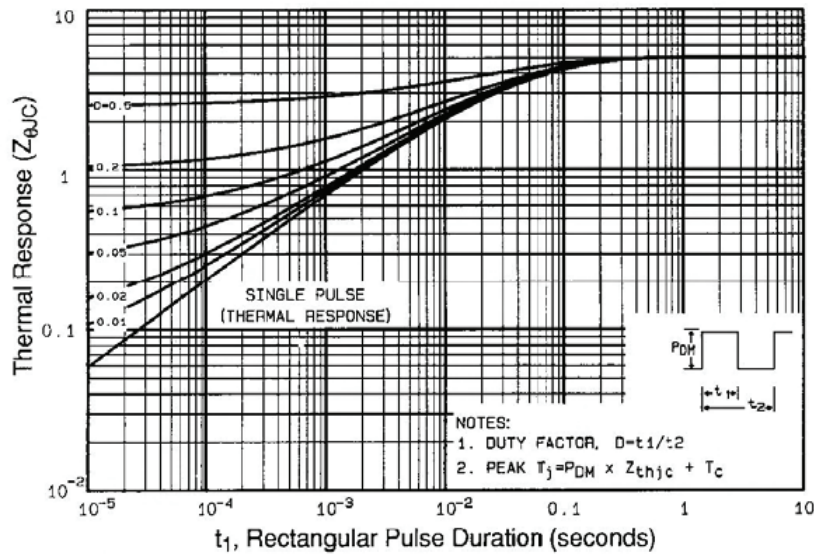


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

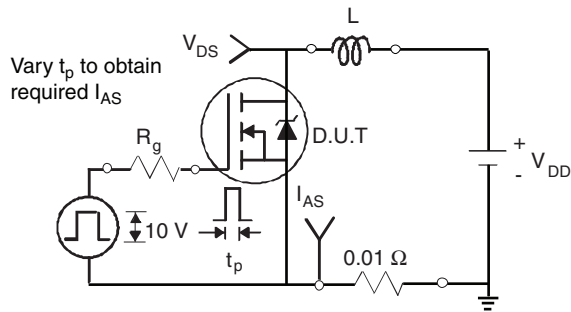


Fig. 12a - Unclamped Inductive Test Circuit

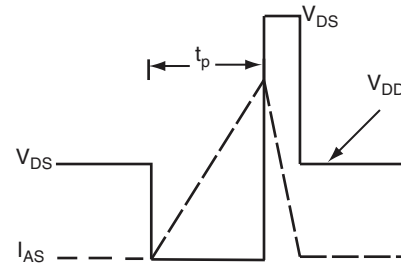


Fig. 12b - Unclamped Inductive Waveforms

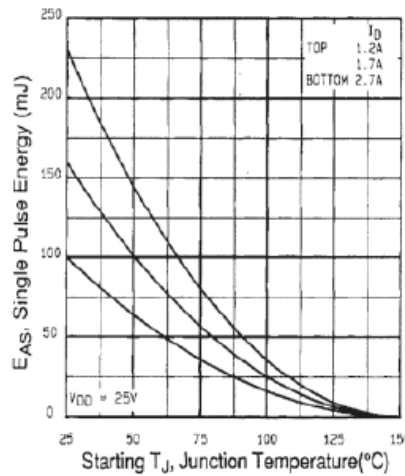


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

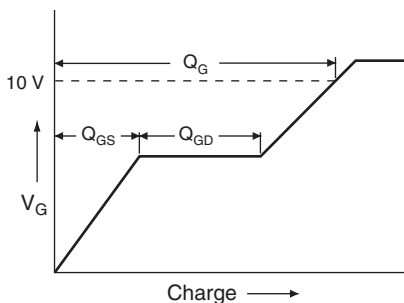


Fig. 13a - Basic Gate Charge Waveform

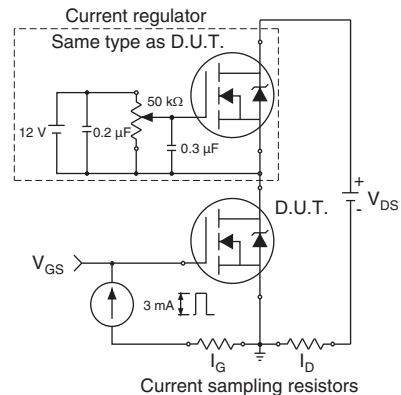
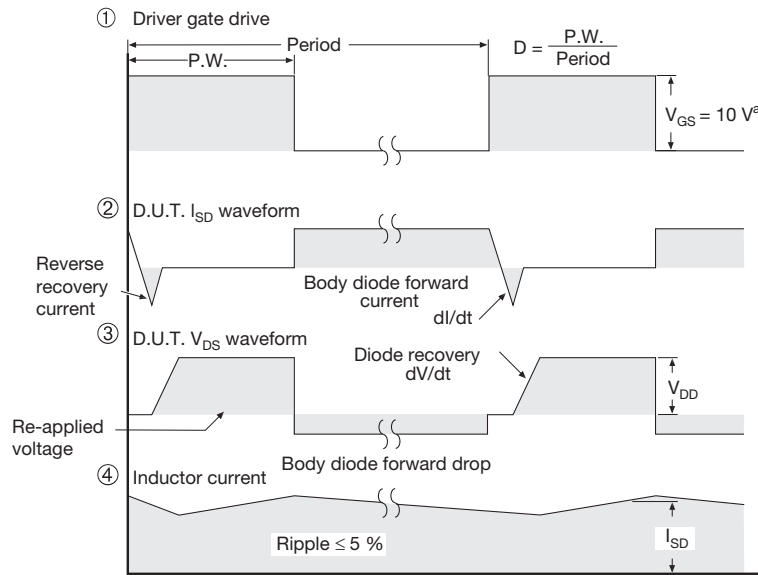
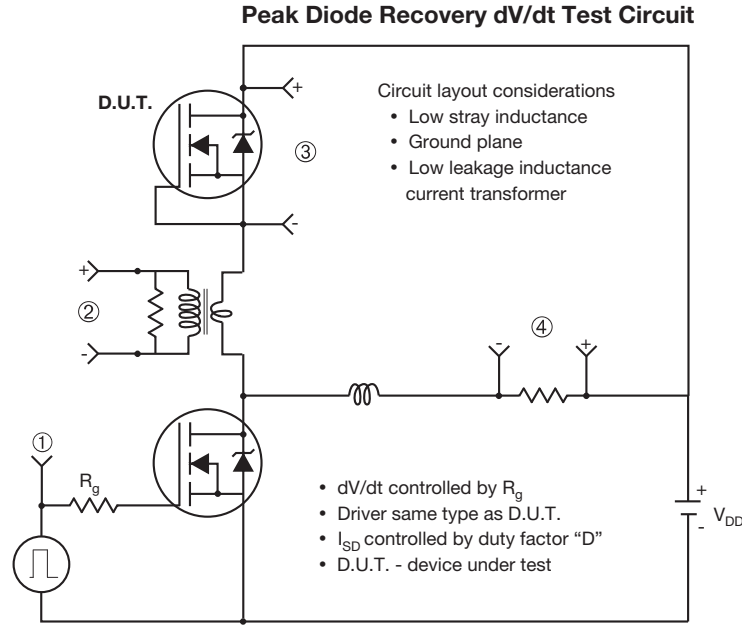


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig.14 - For N-Channel**

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