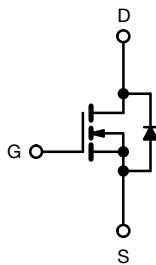
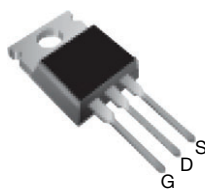


Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Available

RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

APPLICABLE OFF LINE SMPS TOPOLOGIES

- Two transistor forward
- Half and full bridge
- Power factor correction boost

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.52
Q_g max. (nC)	52	
Q_{gs} (nC)	13	
Q_{gd} (nC)	18	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRFB11N50APbF
Lead (Pb)-free and halogen-free	IRFB11N50APbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current	$V_{GS} \text{ at } 10\text{ V}$	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	44	
Linear derating factor		1.3	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	275	mJ
Repetitive avalanche current ^a	I_{AR}	11	A
Repetitive avalanche energy ^a	E_{AR}	17	mJ
Maximum power dissipation	P_D	170	W
Peak diode recovery dV/dt ^c	dV/dt	6.9	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25^\circ\text{C}$, $L = 4.5\text{ mH}$, $R_G = 25\ \Omega$, $I_{AS} = 11\text{ A}$ (see fig. 12)
- $I_{SD} \leq 11\text{ A}$, $dI/dt \leq 140\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.75	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6.6 A ^b	-	-	0.52	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 6.6 A		6.1	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1423	-	pF
Output capacitance	C _{oss}			-	208	-	
Reverse transfer capacitance	C _{rss}			-	8.1	-	
Output capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	2000	-	
			V _{DS} = 400 V, f = 1.0 MHz	-	55	-	
Effective output capacitance	C _{oss eff.}		V _{DS} = 0 V to 400 V	-	97	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 11 A, V _{DS} = 400 V see fig. 6 and 13 ^b	-	-	52	nC
Gate-source charge	Q _{gs}			-	-	13	
Gate-drain charge	Q _{gd}			-	-	18	
Turn-on delay time	t _{d(on)}	V _{DD} = 250 V, I _D = 11 A R _G = 9.1 Ω, R _D = 22 Ω, see fig. 10 ^b		-	14	-	ns
Rise time	t _r			-	35	-	
Turn-off delay time	t _{d(off)}			-	32	-	
Fall time	t _f			-	28	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.5	-	3.2	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	11	A
Pulsed diode forward current ^a	I _{SM}			-	-	44	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 11 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 11 A, dI/dt = 100 A/μs ^b		-	510	770	ns
Body diode reverse recovery charge	Q _{rr}			-	3.4	5.1	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
c. $C_{oss\text{ eff.}}$ effective is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

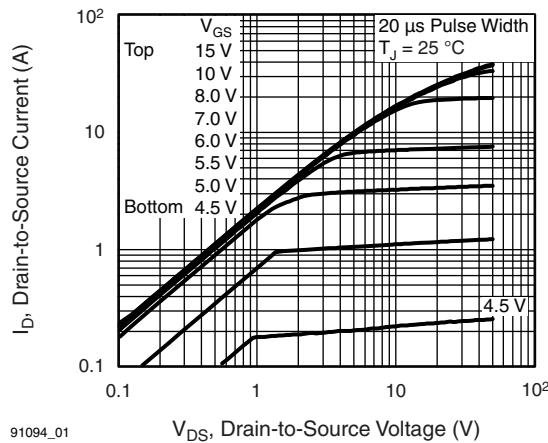


Fig. 1 - Typical Output Characteristics

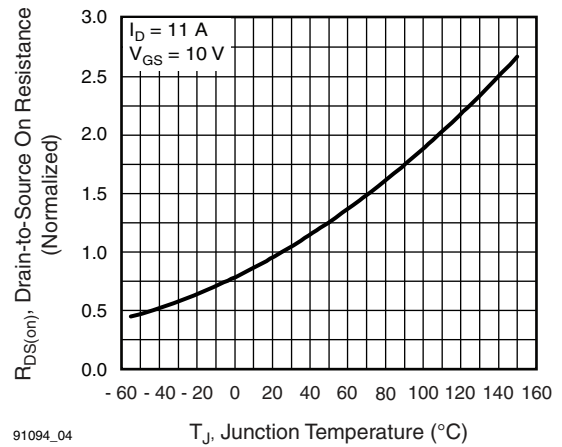


Fig. 4 - Normalized On-Resistance vs. Temperature

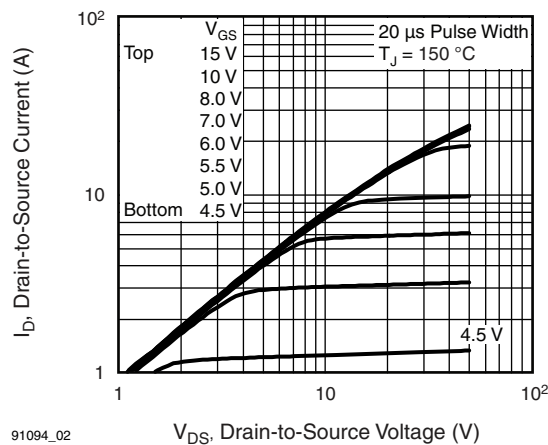


Fig. 2 - Typical Output Characteristics

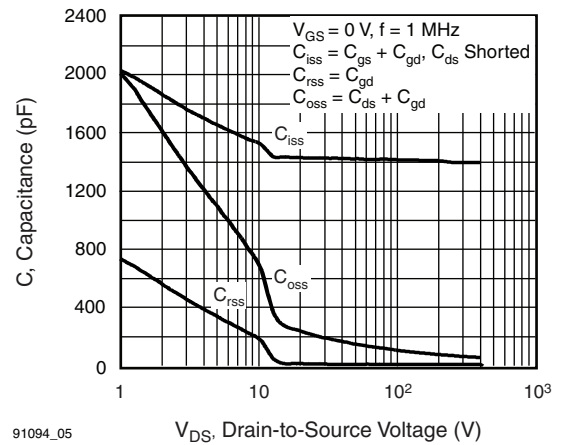


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

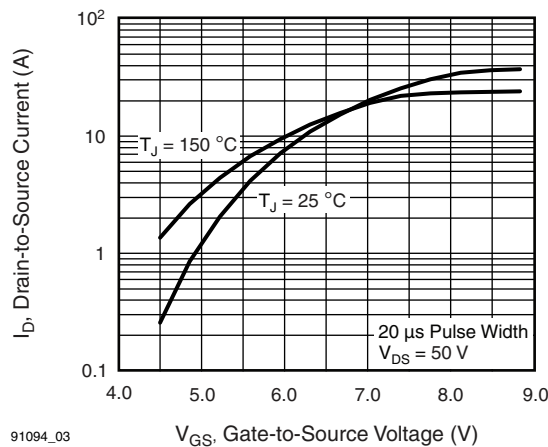


Fig. 3 - Typical Transfer Characteristics

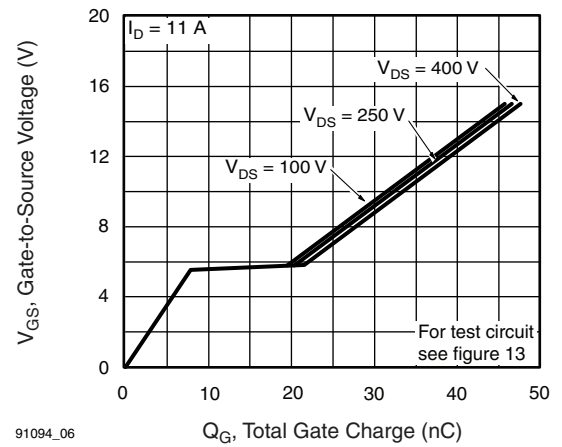
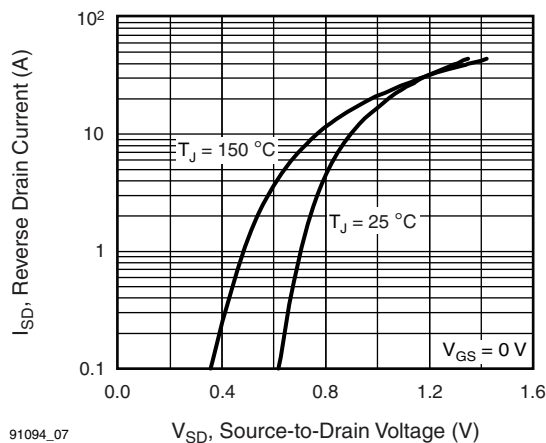
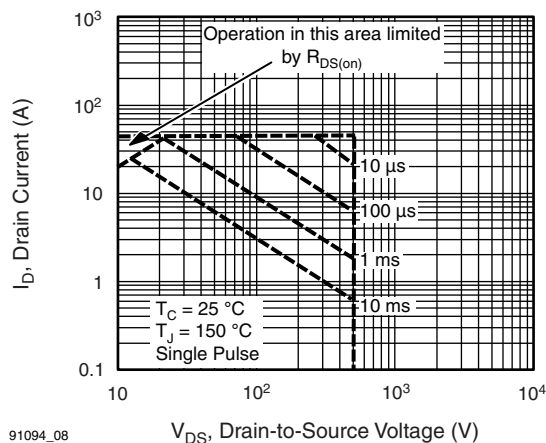
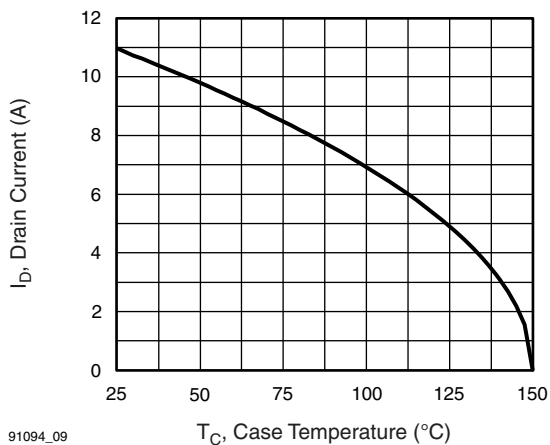
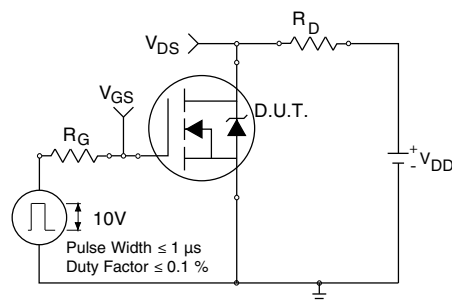
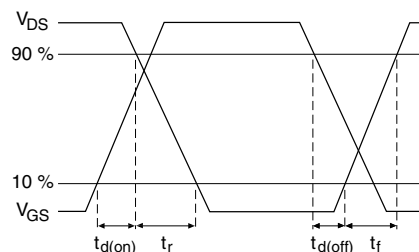
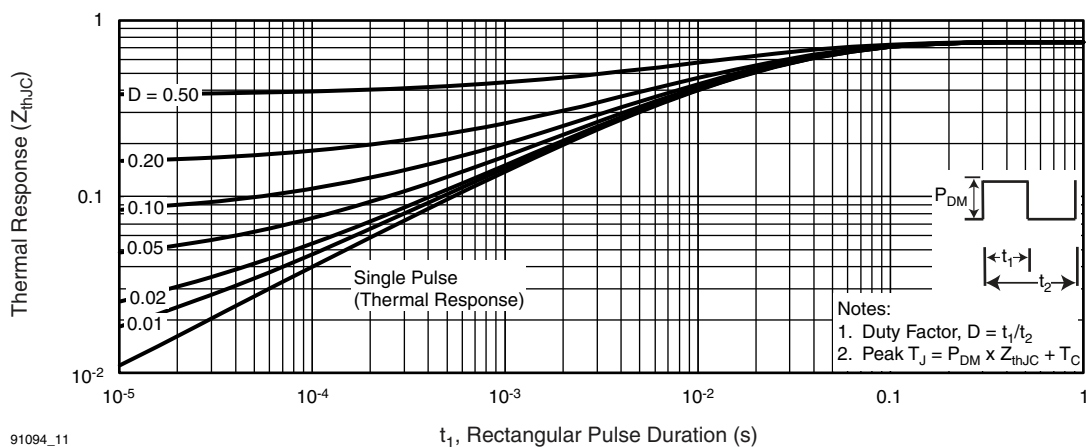
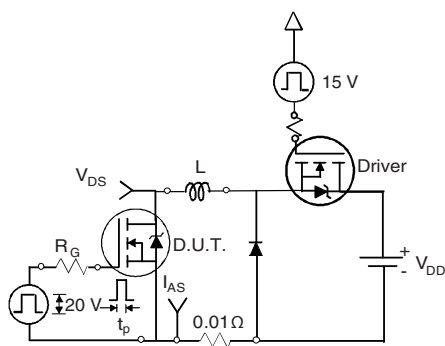
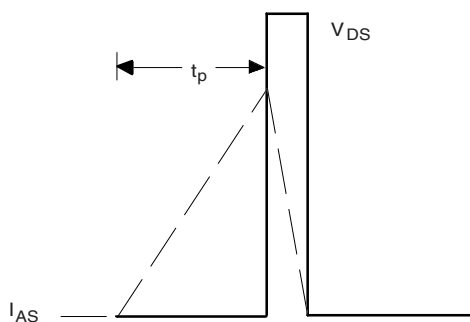
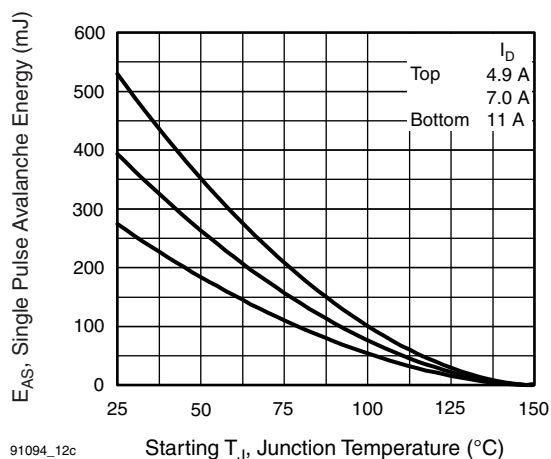
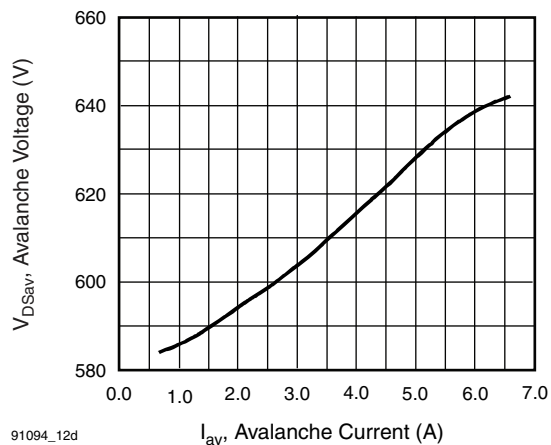
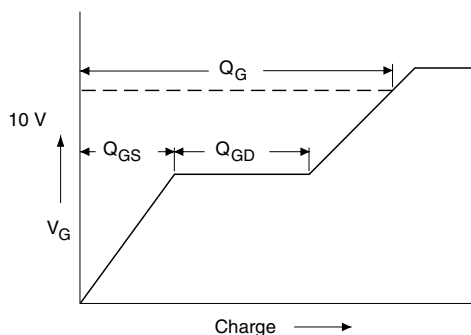
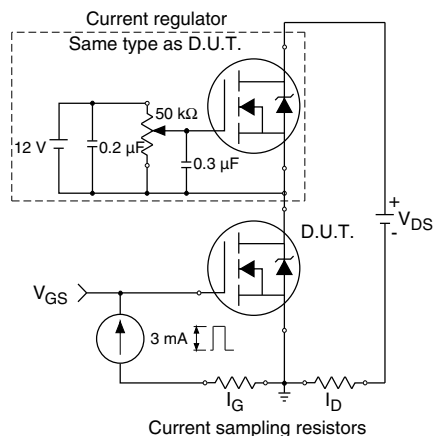
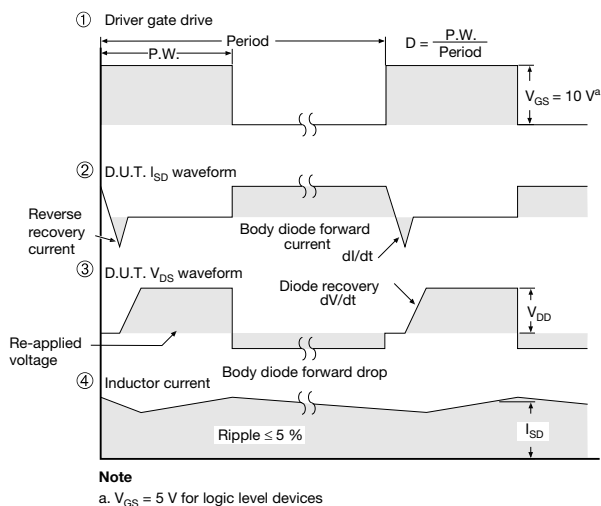
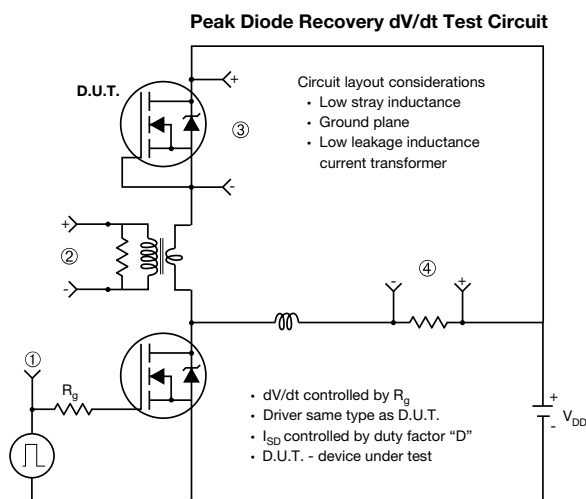


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 8 - Maximum Safe Operating Area

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current


Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Fig. 14 - For N-Channel

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