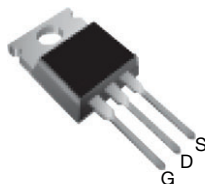


Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V_{DS} (V)	400
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 3.6
Q_g max. (nC)	17
Q_{gs} (nC)	3.4
Q_{gd} (nC)	8.5
Configuration	Single

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF710PbF
Lead (Pb)-free and halogen-free	IRF710PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	400	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	I_D	2.0	A
		1.2	
Pulsed drain current ^a	I_{DM}	6.0	
Linear derating factor		0.29	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	120	mJ
Repetitive avalanche current ^a	I_{AR}	2.0	A
Repetitive avalanche energy ^a	E_{AR}	3.6	mJ
Maximum power dissipation	P_D	36	W
Peak diode recovery dV/dt ^c	dV/dt	4.0	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 52\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.0\text{ A}$ (see fig. 12)
- $I_{SD} \leq 2.0\text{ A}$, $dI/dt \leq 40\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	3.5	

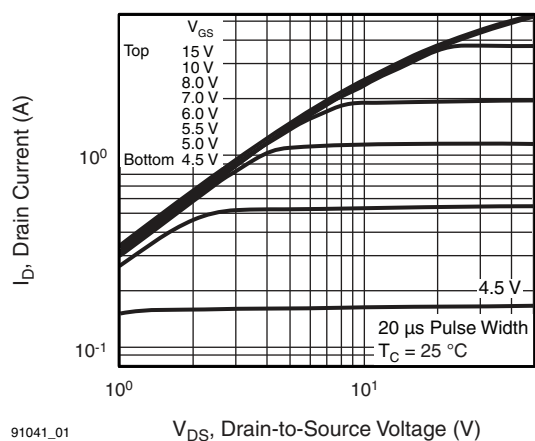
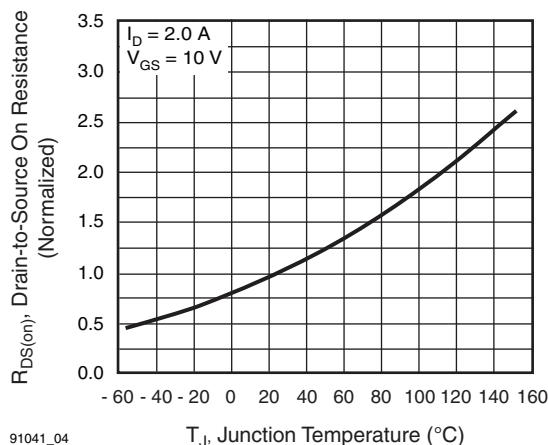
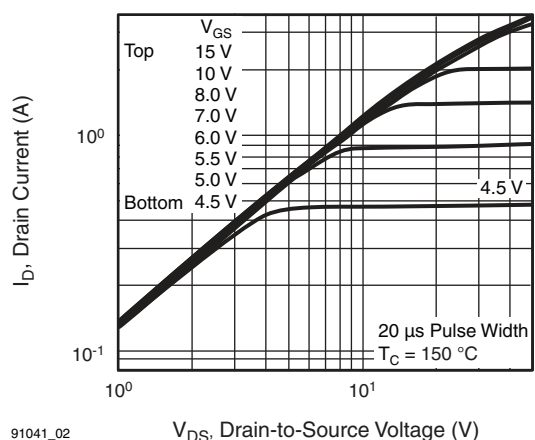
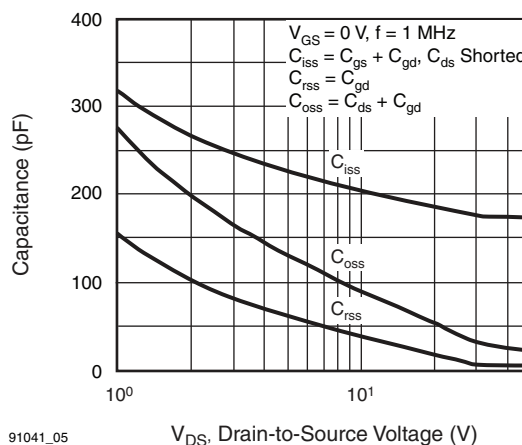
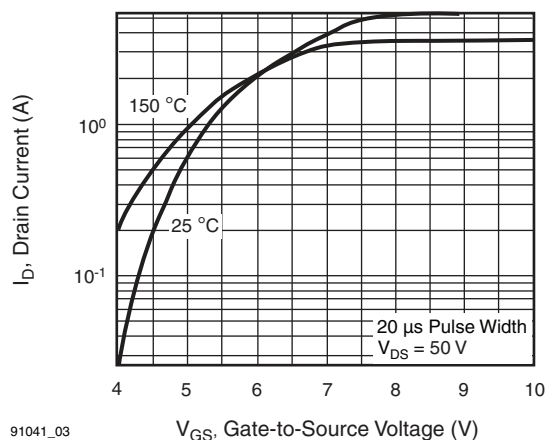
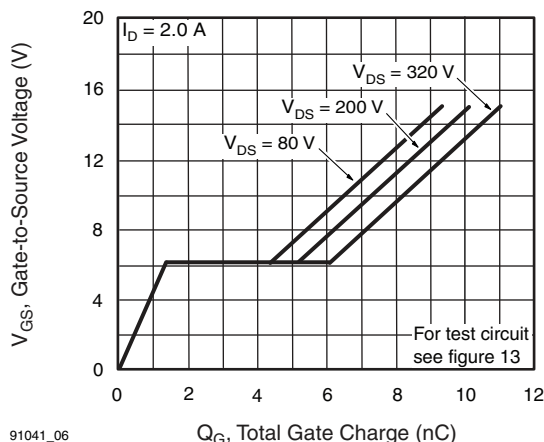
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

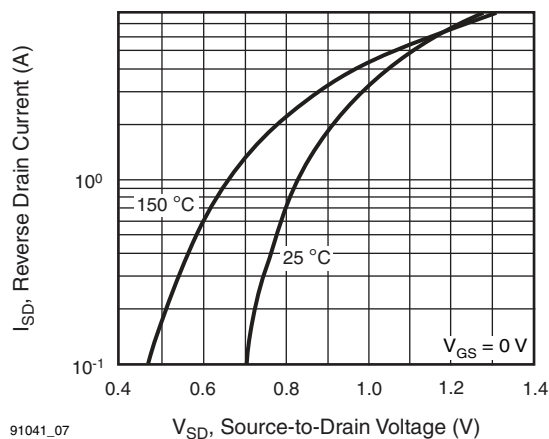
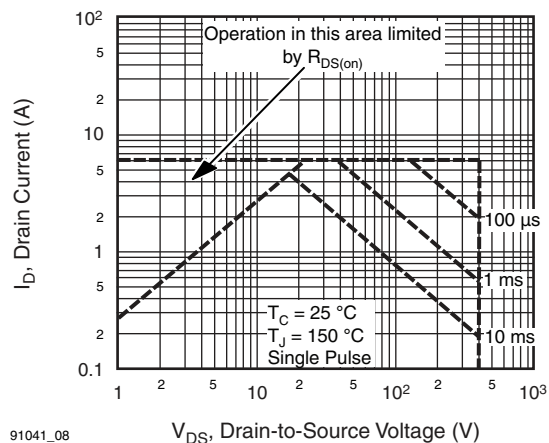
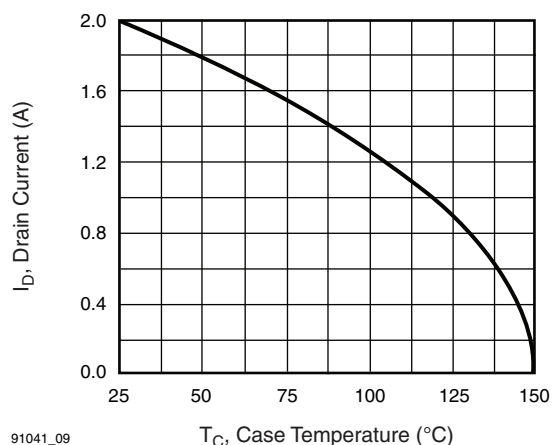
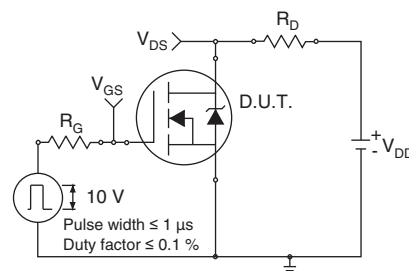
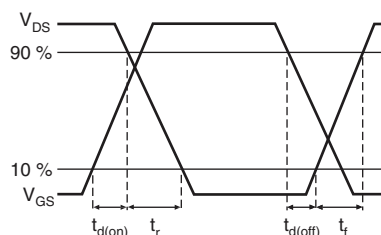
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		400	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.47	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 320V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.2 A ^b	-	-	3.6	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.2 A ^b		1.0	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	170	-	pF
Output capacitance	C _{oss}			-	34	-	
Reverse transfer capacitance	C _{rss}			-	6.3	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 2.0 A, V _{DS} = 320 V see fig. 6 and 13 ^b	-	-	17	nC
Gate-source charge	Q _{gs}			-	-	3.4	
Gate-drain charge	Q _{gd}			-	-	8.5	
Turn-on delay time	t _{d(on)}	V _{DD} = 200 V, I _D = 2.0 A, R _g = 24 Ω, R _D = 95 Ω see fig. 10 ^b		-	8.0	-	ns
Rise time	t _r			-	9.9	-	
Turn-off delay time	t _{d(off)}			-	21	-	
Fall time	t _f			-	11	-	
Gate input resistance	R _g	f = 1 MHz, open drain		1.7	-	11.2	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.0	A
Pulsed diode forward current ^a	I _{SM}			-	-	6.0	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 2.0 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 2.0 A, dI/dt = 100 A/μs ^b		-	240	540	ns
Body diode reverse recovery charge	Q _{rr}			-	0.85	1.6	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 8 - Maximum Safe Operating Area

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

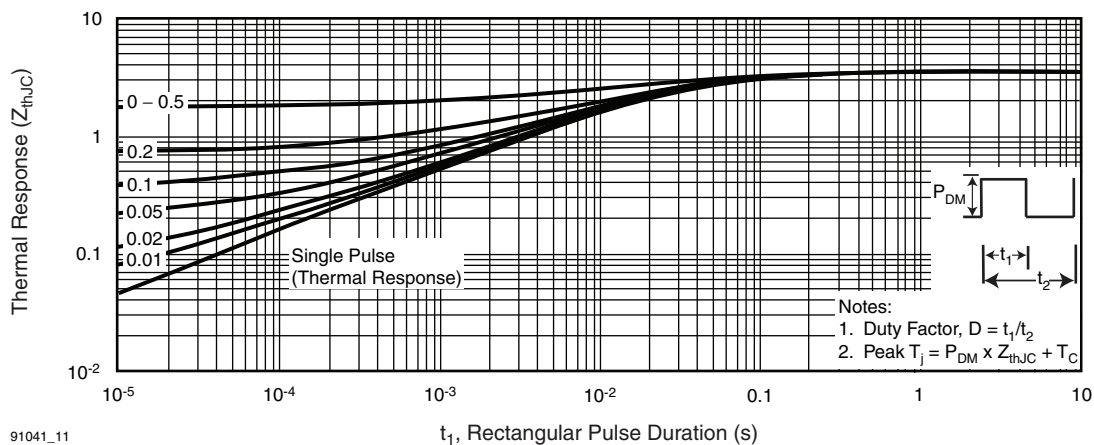


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

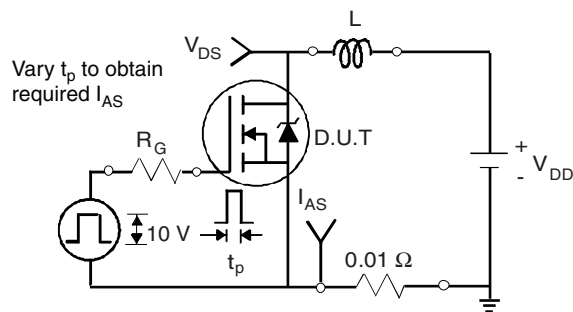


Fig. 12a - Unclamped Inductive Test Circuit

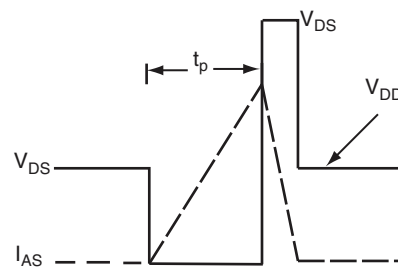


Fig. 12b - Unclamped Inductive Waveforms

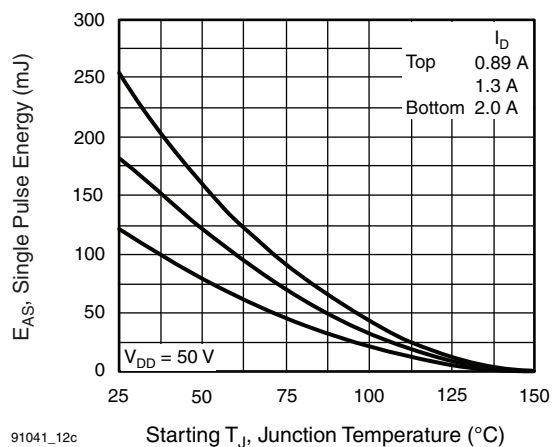
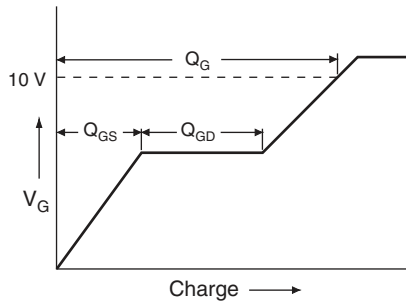
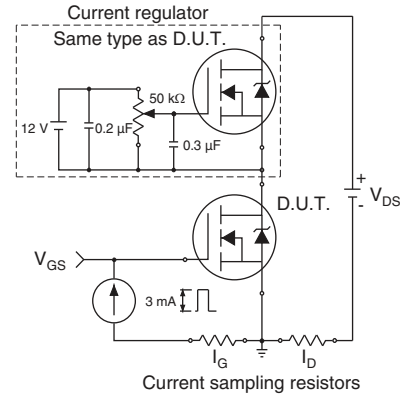
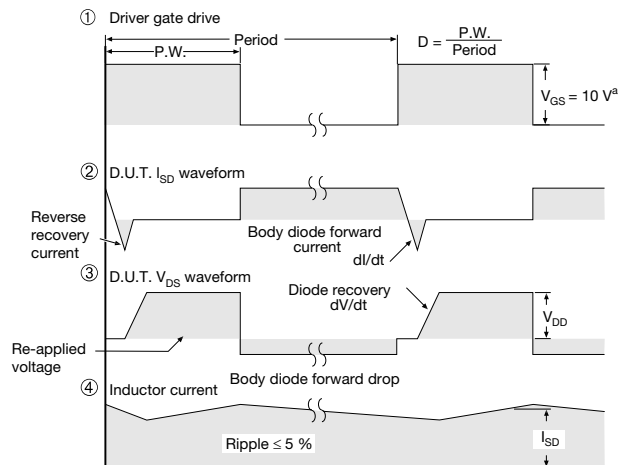
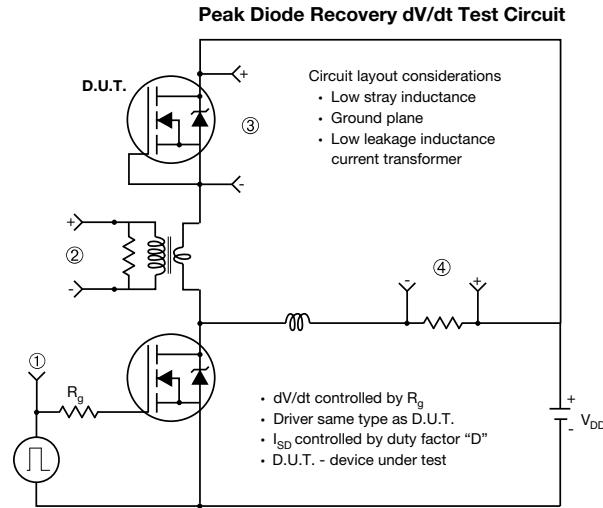


Fig. 12c - Maximum Avalanche Energy vs. Drain Current


Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Note

a. $V_{GS} = 5V$ for logic level devices

Fig. 14 - For N-Channel

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