



# microSD 6.10 Specification

(FxAdv II Series, 3D TLC)

Version 1.3

Address: 28 Genting Lane, #09-03/04/05 Platinum 28, Singapore 349585

Tel : +65-6493 5035

Fax : +65-6493 5037

Website: <http://www.flexxon.com>

Email: [flexxon@flexxon.com](mailto:flexxon@flexxon.com)

ALL RIGHTS ARE STRICTLY RESERVED. ANY PORTION OF THIS PAPER SHALL NOT BE REPRODUCED, COPIED, OR TRANSLATED TO ANY OTHER FORMS WITHOUT PERMISSION FROM FLEXXON.

## Table of Contents

<b>1.</b>	<b>General Description .....</b>	<b>3</b>
1.1.	Introduction.....	3
1.2.	Product Overview .....	3
<b>2.</b>	<b>Product Specifications .....</b>	<b>5</b>
2.1.	Performance .....	5
2.2.	Power .....	5
2.3.	MTBF.....	6
2.4.	Data Retention.....	6
<b>3.</b>	<b>Environmental Specifications.....</b>	<b>7</b>
<b>4.</b>	<b>Electrical Specifications .....</b>	<b>8</b>
4.1.	Absolute Maximum Rating.....	8
4.2.	DC Characteristics .....	8
4.2.1.	Bus Operation Conditions for 3.3V Signaling.....	8
4.2.2.	Bus Signal Line Load.....	9
4.2.3.	Power Up Time of Host .....	9
4.2.4.	Power Up Time of Card .....	10
4.3.	AC Characteristic.....	11
4.3.1.	microSD Interface timing (Default).....	11
4.3.2.	microSD Interface Timing (High-Speed Mode) .....	13
4.3.3.	microSD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes).....	14
4.3.4.	microSD Interface timing (DDR50 Mode) .....	16
<b>5.</b>	<b>Pad Assignment .....</b>	<b>18</b>
<b>6.</b>	<b>Registers .....</b>	<b>19</b>
<b>7.</b>	<b>Physical Dimension .....</b>	<b>20</b>
<b>8.</b>	<b>Ordering Information.....</b>	<b>22</b>

# 1. GENERAL DESCRIPTION

---



## 1.1. Introduction

FLEXON FxAdv II Series microSD 6.1 card is designed for excellent random performance applications, which has good sequential performance, ultimate random performance, high reliability and wide compatibility. It is compliant with the Application performance class (A2) which supports high random performance of at least 4000 read IOPS and 2000 write IOPS. It is suitable for Full HD and 4K Video Recording application.

## 1.2. Product Overview

- ❖ **Flash**
  - 3D TLC
- ❖ **Capacity**
  - 32GB up to 512GB
- ❖ **Support SD system specification version 6.10**
- ❖ **Support SD SPI mode**
- ❖ **Support CPRM (Content Protection for Recordable Media) of SD Card (optional)**
- ❖ **Card removal during read operation will never harm the content**
- ❖ **Password Protection of cards (optional)**
- ❖ **Built-in write protection features (permanent and temporary)**
- ❖ **Support Dynamic and Static Wear Leveling**
- ❖ **Temperature Range**
  - Operation: -25°C ~ 85°C
  - Storage: -40°C ~ 85°C
- ❖ **RoHS Compliant**

❖ **Bus Speed Mode**

■ **UHS-I mode**

- SDR12: SDR up to 25MHz, 1.8V signaling
- SDR25: SDR up to 50MHz, 1.8V signaling
- SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
- SDR104: 1.8V signaling, frequency up to 208MHz, up to 104 MB/sec
- DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

FLEXION CONFIDENTIAL

## 2. PRODUCT SPECIFICATIONS



### 2.1. Performance

Table 2-1 Performance of microSD (FxAdv II)

Capacity	A2		Sequential	
	Read (IOPS)	Write (IOPS)	Read (MB/s)	Write (MB/s)
32GB	9800	2300	100	53
64GB	9800	2300	100	53
128GB	9800	2600	100	90
256GB	9800	2700	100	90
512GB	9800	2700	100	90

**NOTES:**

1. The performance is obtained from TestMetrix Test.
2. Samples are made of Toshiba 3D NAND Flash.
3. Performance may vary from flash configuration and platform.

### 2.2. Power

Table 2-2 Typical Power Consumption of microSD (FxAdv II)

Capacity	Read (mA)	Write (mA)	Standby (mA)
32GB	80	80	0.1
64GB	80	80	0.1
128GB	100	100	0.1
256GB	100	100	0.1
512GB	100	100	0.1

**NOTES:**

1. Power consumption may vary from flash configuration and platform.

### **2.3. MTBF**

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The higher the MTBF value, the higher the reliability of the device. The predicted result of FLEXON's FxAdv II Series microSD is more than 2,000,000 hours.

### **2.4. Data Retention**

- 10 years if > 90% life remaining (@40C)
- 1 year if < 10% life remaining (@40C)

FLEXON CONFIDENTIAL

### 3. ENVIRONMENTAL SPECIFICATIONS



Test Items	Test Conditions
Storage Temperature	-40°C ~ 85°C
Operating Temperature	-25°C ~ 85°C
Storage Humidity	40°C, 93% RH
Operating Humidity	25°C, 95% RH
Shock	1500G, Half Sin Pulse Duration 0.5ms
Vibration	80Hz ~ 2000Hz/20G, 20Hz ~ 80Hz/1.52mm, 3 axis/30min
Drop	150cm free fall, 6 face of each unit
Bending	≥ 10N, Hold 1 min/5 times
Torque	0.1N-m or +/-2.5 deg, Hold 30 seconds/5 times
ESD	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times

FLEXXON CONFIDENTIAL

## 4. ELECTRICAL SPECIFICATIONS



### 4.1. Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}$	Supply Voltage	2.7	3.6	V
2	$T_a$	Operating Temperature	-25	+85	°C
3	$T_{st}$	Storage Temperature	-40	+85	°C

### 4.2. DC Characteristics

#### 4.2.1. Bus Operation Conditions for 3.3V Signaling

Table 4-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	$V_{DD}$	2.7	3.6	V	
Output High Voltage	$V_{OH}$	$0.75 \cdot V_{DD}$		V	$I_{OH} = -2mA$ $V_{DD}$ Min
Output Low Voltage	$V_{OL}$		$0.125 \cdot V_{DD}$	V	$I_{OL} = 2mA$ $V_{DD}$ Min
Input High Voltage	$V_{IH}$	$0.625 \cdot V_{DD}$	$V_{DD} + 0.3$	V	
Input Low Voltage	$V_{IL}$	$V_{SS} - 0.3$	$0.25 \cdot V_{DD}$	V	
Power Up Time			250	ms	From 0V to $V_{DD}$ min

Table 4-2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	$V_{DD} + 0.3$	V	
<b>All Inputs</b>					
Input Leakage Current		-10	10	uA	
<b>All Outputs</b>					
Output Leakage Current		-10	10	uA	

Table 4-3 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
-----------	--------	------	-----	------	-----------

Supply Voltage	$V_{DD}$	2.7	3.6	V	
Regulator Voltage	$V_{DDIO}$	1.7	1.95	V	Generated by $V_{DD}$
Output High Voltage	$V_{OH}$	1.4	-	V	$I_{OH}=-2mA$
Output Low Voltage	$V_{OL}$	-	0.45	V	$I_{OL}=2mA$
Input High Voltage	$V_{IH}$	1.27	2.00	V	
Input Low Voltage	$V_{IL}$	$V_{SS}-0.3$	0.58	V	

**Table 4-4 Input Leakage Current for 1.8V Signaling**

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

#### 4.2.2. Bus Signal Line Load

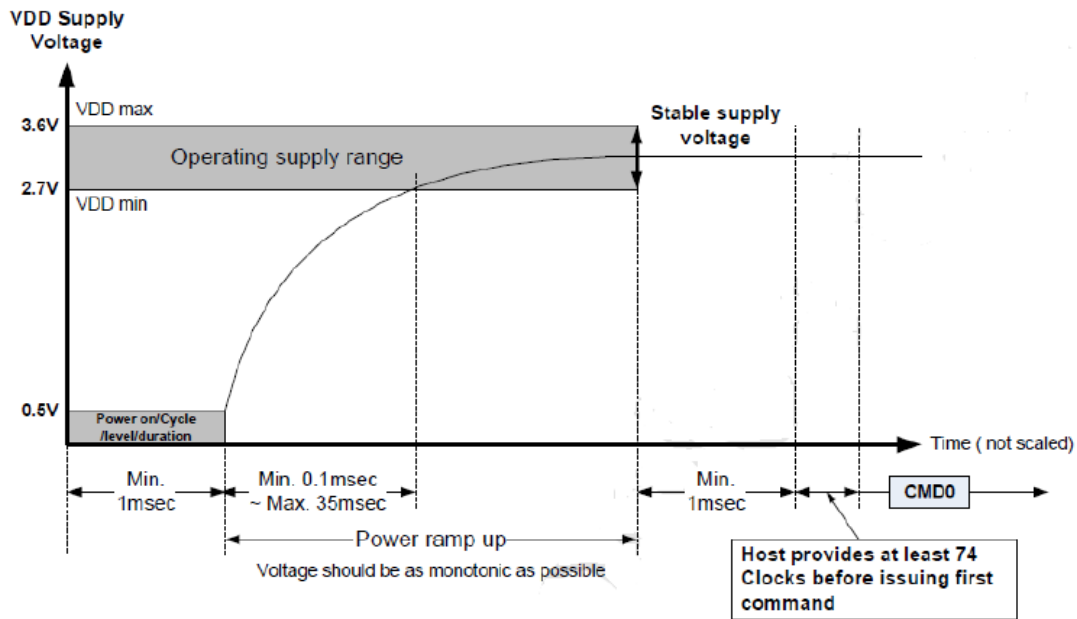
##### Bus Operation Conditions – Signal Line’s Load

$$\text{Total Bus Capacitance} = C_{\text{HOST}} + C_{\text{BUS}} + N C_{\text{CARD}}$$

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	$R_{CMD}$ $R_{DAT}$	10	100	k $\Omega$	to prevent bus floating
Total bus capacitance for each signal line	$C_L$		40	pF	1 card $C_{\text{HOST}}+C_{\text{BUS}}$ shall not exceed 30 pF
Card Capacitance for each signal pin	$C_{\text{CARD}}$		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	$R_{\text{DAT3}}$	10	90	k $\Omega$	May be used for card detection
Capacity Connected to Power Line	$C_C$		5	uF	To prevent inrush current

#### 4.2.3. Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



### Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

- (1) Voltage level shall be below 0.5V
- (2) Duration shall be at least 1ms.

### Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

- (1) Voltage of power ramp up should be monotonic as much as possible.
- (2) The minimum ramp up time should be 0.1ms.
- (3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
- (4) Host shall wait until VDD is stable.
- (5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

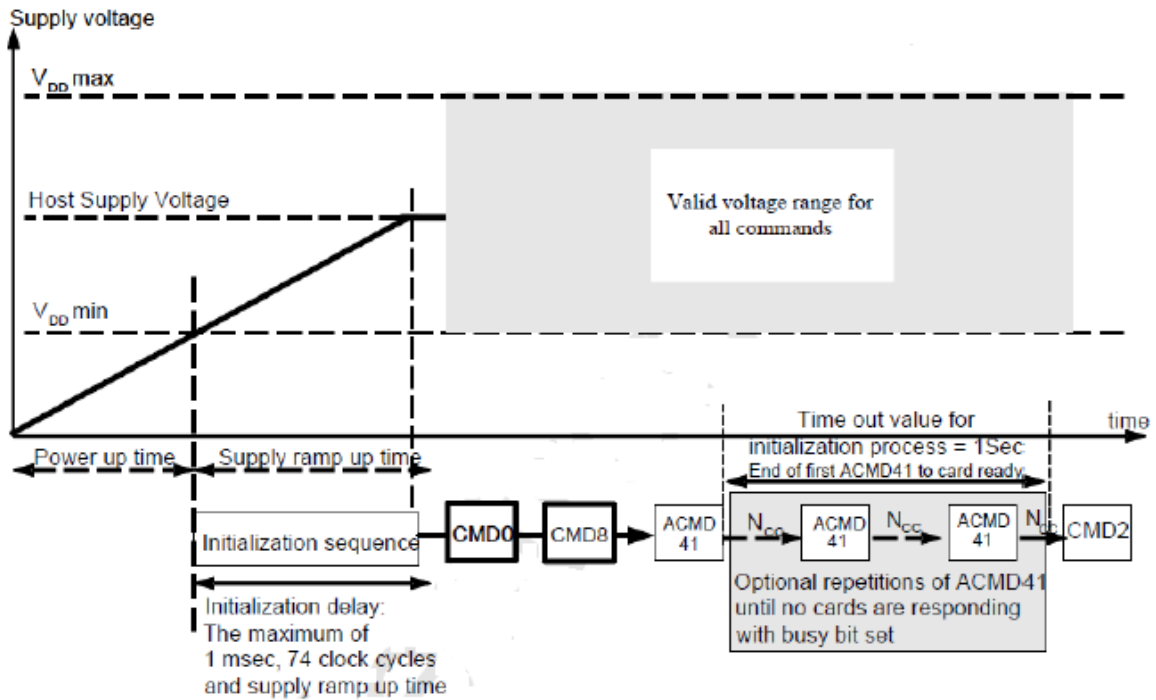
### Power Down and Power Cycle

- When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State*. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

### 4.2.4. Power Up Time of Card

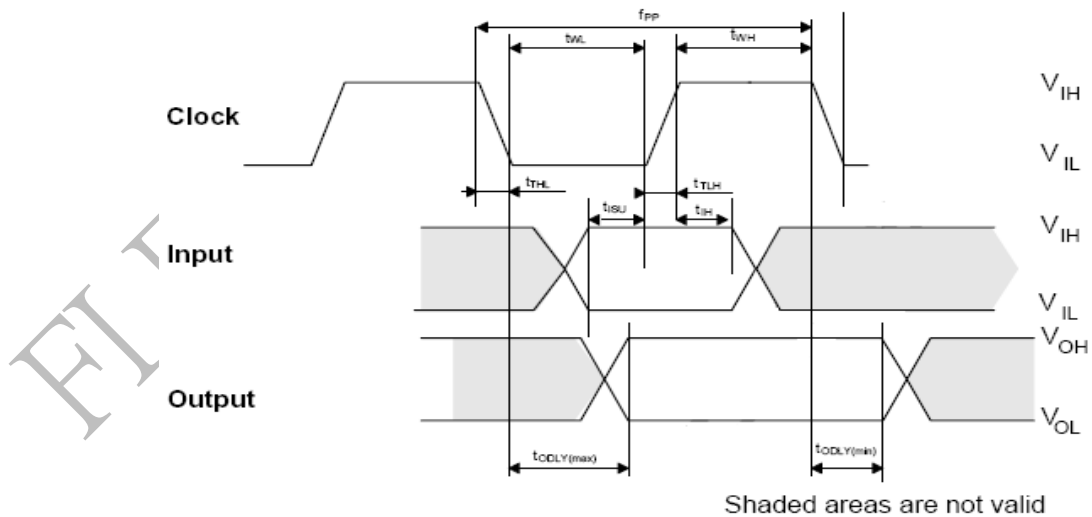
A device shall be ready to accept the first command within 1ms from detecting VDD min.

Device may use up to 74 clocks for preparation before receiving the first command.



### 4.3. AC Characteristic

#### 4.3.1. microSD Interface timing (Default)

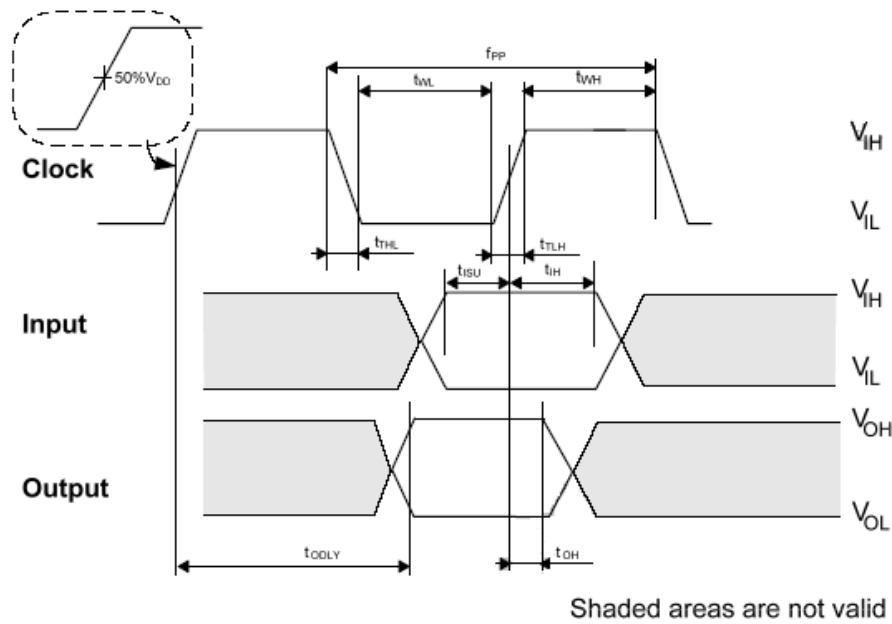


Parameter	Symbol	Min	Max	Unit	Remark
<b>Clock CLK (All values are referred to min(V<sub>IH</sub>) and max(V<sub>IL</sub>))</b>					
Clock frequency Data	f <sub>PP</sub>	0	25	MHz	C <sub>card</sub> ≤ 10 pF

Transfer Mode					(1 card)
Clock frequency Identification Mode	$f_{OD}$	0 <sub>(1)</sub> /100	400	KHz	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock low time	$t_{WL}$	10		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock high time	$t_{WH}$	10		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock rise time	$t_{TLH}$		10	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock fall time	$t_{THL}$		10	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
<b>Inputs CMD, DAT (referenced to CLK)</b>					
Input set-up time	$t_{ISU}$	5		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Input hold time	$t_{IH}$	5		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
<b>Outputs CMD, DAT (referenced to CLK)</b>					
Output Delay time during Data Transfer Mode	$t_{ODLY}$	0	14	ns	$C_L \leq 40 \text{ pF}$ (1 card)
Output Delay time during Identification Mode	$t_{ODLY}$	0	50	ns	$C_L \leq 40 \text{ pF}$ (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continues clock is required.

### 4.3.2. microSD Interface Timing (High-Speed Mode)

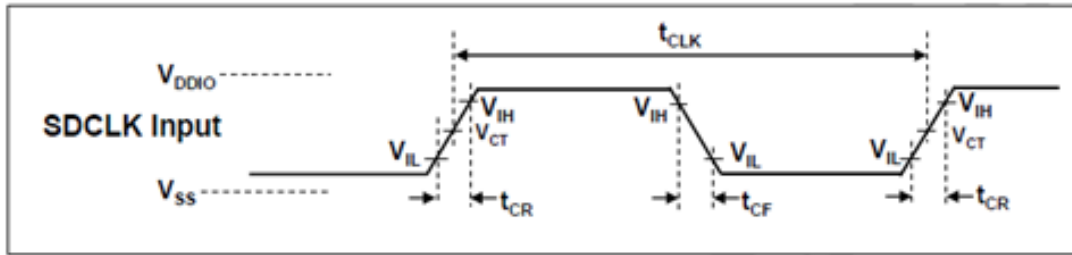


Parameter	Symbol	Min	Max	Unit	Remark
<b>Clock CLK (All values are referred to min(V<sub>IH</sub>) and max(V<sub>IL</sub>))</b>					
Clock frequency Data Transfer Mode	$f_{PP}$	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
Clock low time	$t_{WL}$	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock high time	$t_{WH}$	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock rise time	$t_{TLH}$		3	ns	$C_{card} \leq 10$ pF (1 card)
Clock fall time	$t_{THL}$		3	ns	$C_{card} \leq 10$ pF (1 card)
<b>Inputs CMD, DAT (referenced to CLK)</b>					
Input set-up time	$t_{ISU}$	6		ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	$t_{IH}$	2		ns	$C_{card} \leq 10$ pF (1 card)
<b>Outputs CMD, DAT (referenced to CLK)</b>					
Output Delay time during Data Transfer Mode	$t_{ODLY}$		14	ns	$C_L \leq 40$ pF (1 card)
Output Hold time	$T_{OH}$	2.5		ns	$C_L \leq 15$ pF (1 card)
Total System capacitance of each line <sup>1</sup>	$C_L$		40	pF	$C_L \leq 15$ pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

### 4.3.3. microSD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

**Input:**

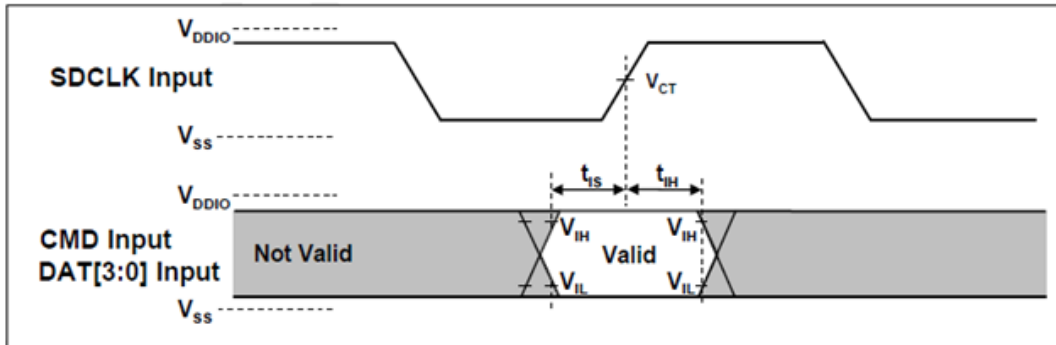


**Clock Signal Timing**

Symbol	Min	Max	Unit	Remark
$t_{CLK}$	4.80	-	ns	208MHz (Max.), Between rising edge, $V_{CT}= 0.975V$
$t_{CR}, t_{CF}$	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 0.96ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of $t_{CR}, t_{CF}$ is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

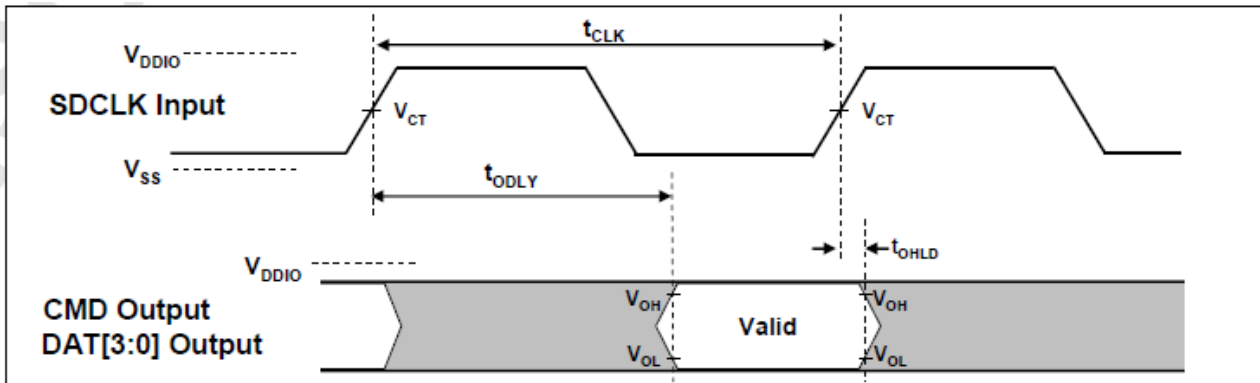
**SDR50 and SDR104 Input Timing:**



**Card Input Timing**

Symbol	Min	Max	Unit	SDR104 Mode
$t_{IS}$	1.40	-	ns	$C_{CARD} = 10pF, V_{CT}= 0.975V$
$t_{IH}$	0.8	-	ns	$C_{CARD} = 5pF, V_{CT}= 0.975V$
Symbol	Min	Max	Unit	SDR50 Mode
$t_{IS}$	3.00	-	ns	$C_{CARD} = 10pF, V_{CT}= 0.975V$
$t_{IH}$	0.8	-	ns	$C_{CARD} = 5pF, V_{CT}= 0.975V$

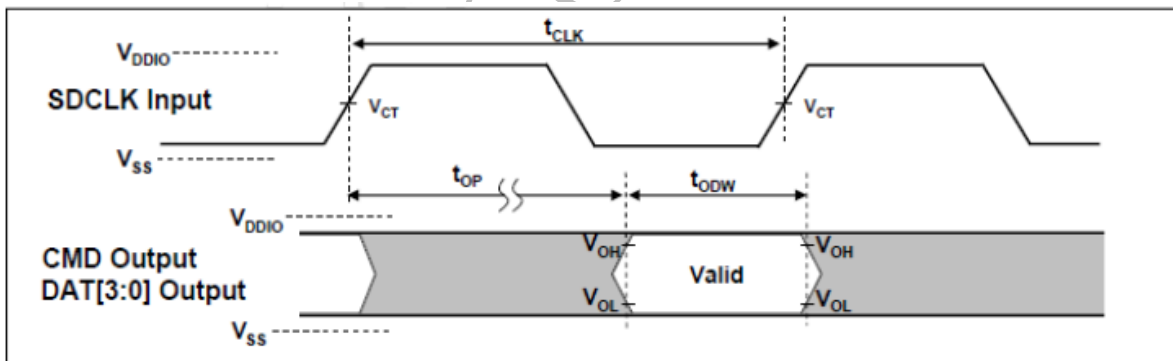
**Output (SDR12, SDR25, SDR50):**



**Output Timing of Fixed Data Window**

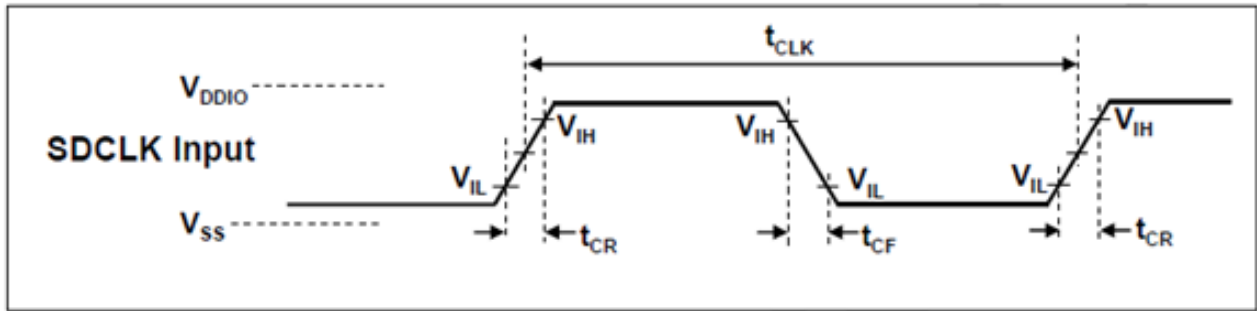
Symbol	Min	Max	Unit	Remark
$t_{ODLY}$	-	7.5	ns	$t_{CLK} \geq 10.0ns$ , $C_L = 30pF$ , using driver Type B, for SDR50
$t_{ODLY}$	-	14	ns	$t_{CLK} \geq 20.0ns$ , $C_L = 40pF$ , using driver Type B, for SDR25 and SDR12,
$T_{OH}$	1.5	-	ns	Hold time at the $t_{ODLY}$ (min.), $C_L = 15pF$

**Output (SDR104 Mode):**



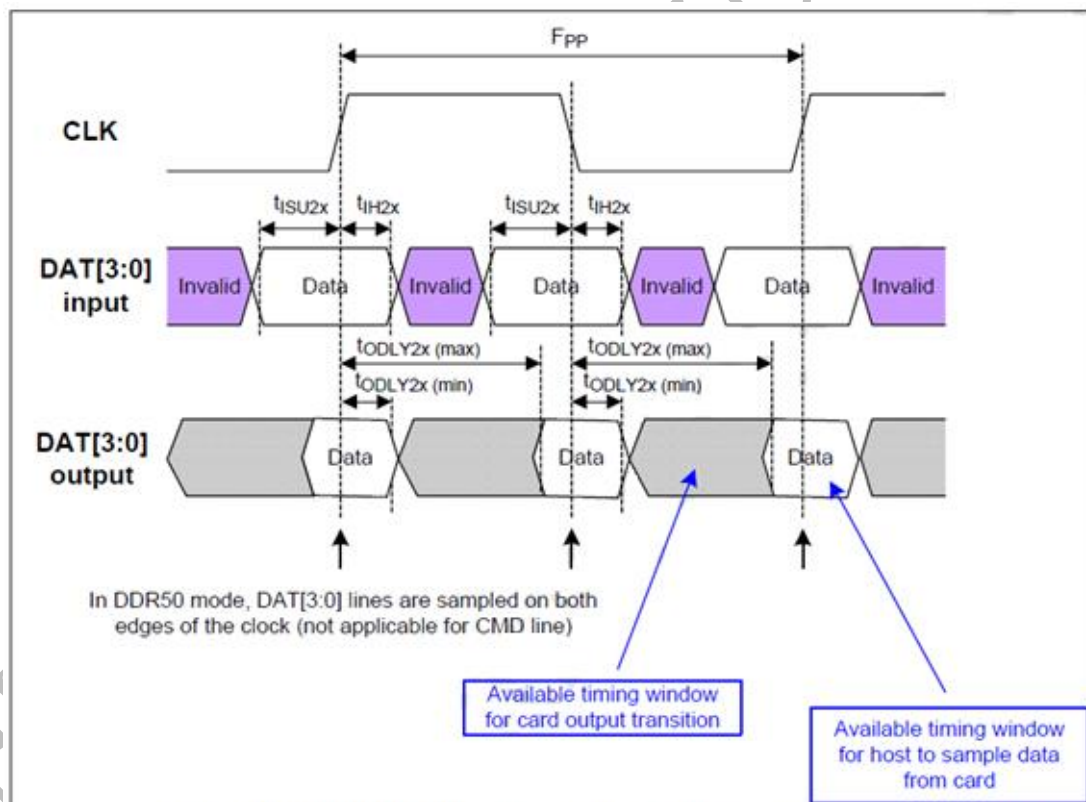
Symbol	Min	Max	Unit	Remark
$t_{OP}$	0	2	UI	Card Output Phase
$\Delta t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
$t_{ODW}$	0.60	-	UI	$t_{ODW} = 2.88ns$ at 208MHz

### 4.3.4. microSD Interface timing (DDR50 Mode)



**Clock Signal Timing**

Symbol	Min	Max	Unit	Remark
$t_{CLK}$	20	-	ns	50MHz (Max.), Between rising edge
$t_{CR}, t_{CF}$	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00ns$ (max.) at 50MHz, $C_{CARD}=10pF$
Clock Duty	45	55	%	



**Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode**

**Bus Timings – Parameters Values (DDR50 Mode)**

Parameter	Symbol	Min	Max	Unit	Remark
<b>Input CMD (referenced to CLK rising edge)</b>					
Input set-up time	$t_{ISU}$	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	$t_{IH}$	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
<b>Output CMD (referenced to CLK rising edge)</b>					
Output Delay time during Data Transfer Mode	$t_{ODLY}$		13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	$T_{OH}$	1.5	-	ns	$C_L \geq 15$ pF (1 card)
<b>Inputs DAT (referenced to CLK rising and falling edges)</b>					
Input set-up time	$t_{ISU2x}$	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	$t_{IH2x}$	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
<b>Outputs DAT (referenced to CLK rising and falling edges)</b>					
Output Delay time during Data Transfer Mode	$t_{ODLY2x}$		7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	$T_{OH2x}$	1.5	-	ns	$C_L \geq 15$ pF (1 card)

## 5. PAD ASSIGNMENT

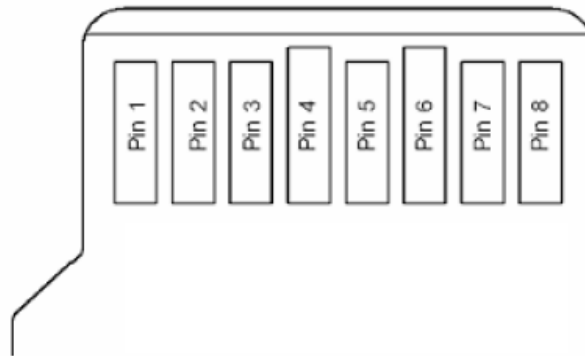


Table 5-1 microSD Memory Card Pad Assignment

pin	SD Mode			SPI Mode		
	Name	Type <sup>1</sup>	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 <sup>2</sup>	I/O/PP <sup>3</sup>	Card Detect/ Data Line[bit3]	CS	I <sup>3</sup>	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V <sub>DD</sub>	S	Supply voltage	V <sub>DD</sub>	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V <sub>SS</sub>	S	Supply voltage ground	V <sub>SS</sub>	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

- (1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
- (2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET\_BUS\_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.
- (3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET\_CLR\_CARD\_DETECT (ACMD42) command.

## 6. REGISTERS



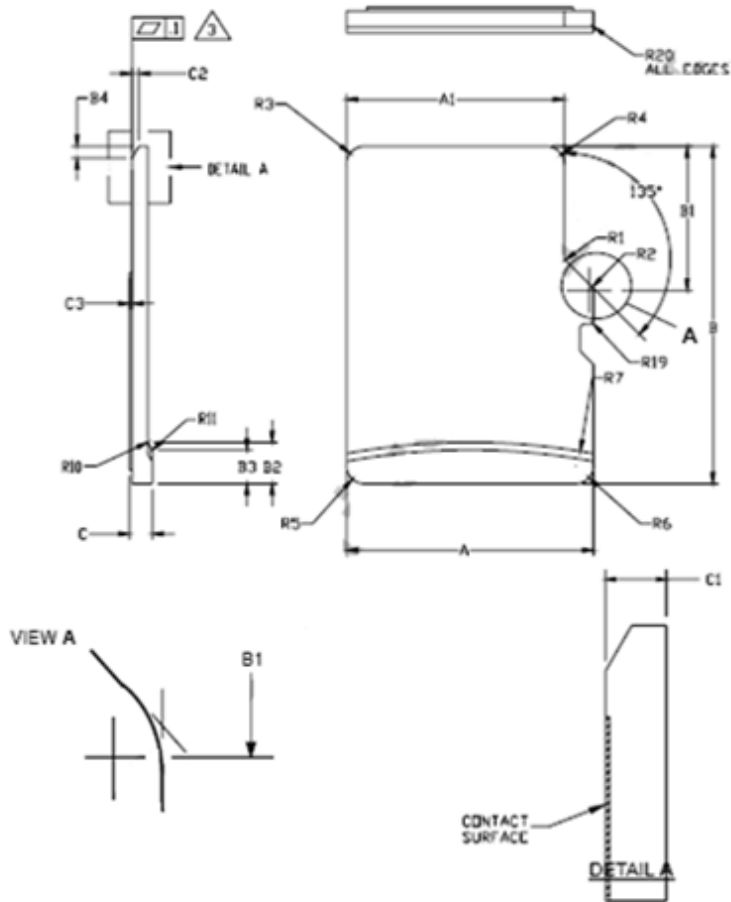
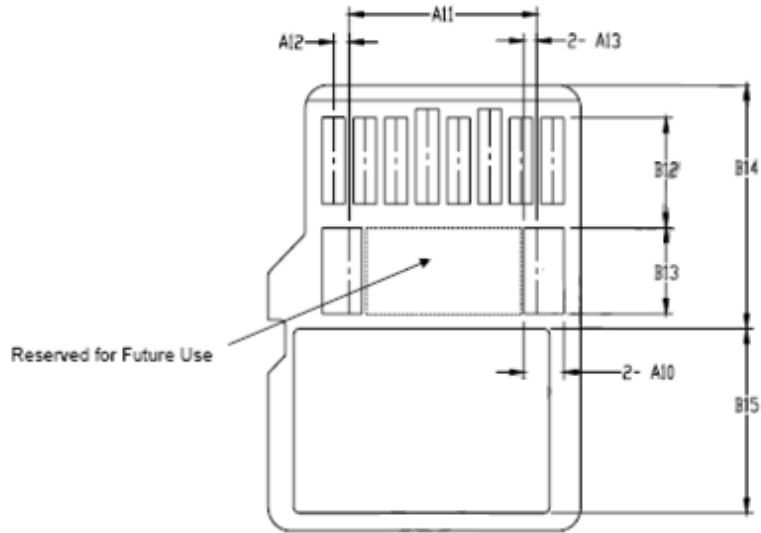
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification.
RCA	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization.
DSR	16bit	Driver Stage Register; to configure the card's output drivers.
CSD	128bit	Card Specific Data; Information about the card operation conditions.
SCR	64bit	SD Configuration Register; Information about the SD Memory Card's Special Features capabilities
OCR	32bit	Operation conditions register.
SSR	512bit	SD Status; Information about the card proprietary features.
OCR	32bit	Card Status; Information about the card status.

FLEXON CONFIDENTIAL

## 7. PHYSICAL DIMENSION



Dimension: 15mm (L) x 11mm (W) x 1mm (H)



Common Dimensions				
Symbol	Min	Nom	Max	Note
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	Basic
A3	7.60	7.70	7.80	
A4	-	1.10	-	Basic
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.60	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	-	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Dimensions are in millimeters.
3. Coplanarity is additive to C1 Max. thickness



**8. ORDERING INFORMATION**

Capacity	MPN
32GB	FDMM032GBC-320K
64GB	FDMM064GBC-320K
128GB	FDMM128GBC-320K
256GB	FDMM256GBC-320K
512GB	FDMM512GBC-320K

FLEXXON CONFIDENTIAL

## Revision History

Revision	Release Date	Description
1.0	2021/09	First release
1.1	2021/09	Update Capacity
1.2	2022/05	Add 32GB capacity
1.3	2022/09	Update Section 2.4

FLEXXON CONFIDENTIAL