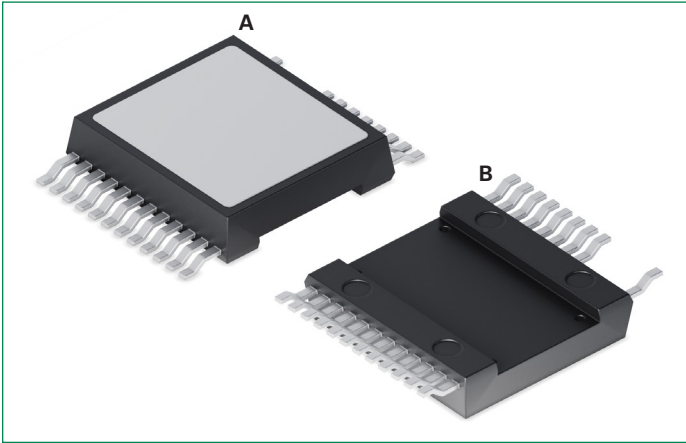


MMIX1T500N20X4

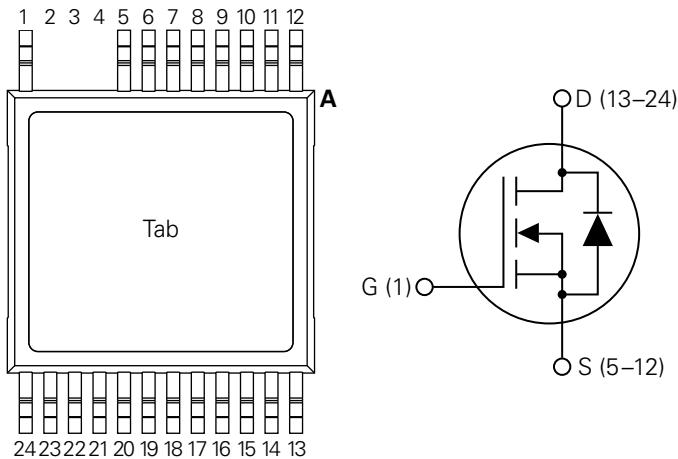
200 V, 1.99 mΩ, 480 A X4-Class Power MOSFET in SMPD-X

N-Channel Enhancement Mode



A: Top, B: Bottom

Pinout Diagram (SMPD-X)



G (Pin 1): Gate; S (Pins 5–12): Source; D (Pins 13–24): Drain; Tab: Isolated

Features

- Up to 200 V blocking voltage with low $R_{DS(on)}$ of 1.99 mΩ
- Low gate charge Q_g of 535 nC
- High current capability $I_D = 480$ A
- Compact design with high power density

Benefits

- Low conduction losses and reduced heat dissipation
- Low gate drive power requirements
- Reduced paralleling effort and decreased part count
- Cost-efficient solution with ease of assembly

SMPD Package

- High performance ceramic based isolated package improves overall thermal resistance $R_{th(j-s)}$ and power handling capability
- Isolation voltage 2500 V AC (RMS), 1 minute
- Low drain-to-tab stray capacitance
- Advanced topside cooled packaging simplifies thermal management
- RoHS compliant
- Epoxy meets UL 94V-0

Applications

- DC load switch
- Battery energy storage systems
- Industrial and process power supplies
- Industrial charging infrastructures
- Drones and VTOL

Product Summary

Characteristic	Value	Unit
V_{DSS}	200	V
$I_D @ 25^\circ\text{C}$	480	A
$R_{DS(on)}$	≤ 1.99	mΩ

Maximum Ratings

Symbol	Characteristic	Conditions	Value	Unit
V_{DSS}	Drain-source voltage	$T_{vj} = 25\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$	200	V
V_{GSS}	Gate-source voltage	Continuous	± 20	V
V_{GSM}		Transient	± 30	
I_{D25}	Drain current	$T_c = 25\text{ }^{\circ}\text{C}$	480	A
I_{DM}		$T_c = 25\text{ }^{\circ}\text{C}$, pulse width limited by $T_{vj(max)}$	1300	
I_A	Avalanche current	$T_c = 25\text{ }^{\circ}\text{C}$	250	A
E_{AS}	Avalanche energy	$T_c = 25\text{ }^{\circ}\text{C}$	5	J
dv/dt	Reverse diode dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_{vj} \leq 150\text{ }^{\circ}\text{C}$	50	V/ns
P_D	Power dissipation	$T_c = 25\text{ }^{\circ}\text{C}$	1070	W
T_{vj}	Virtual junction temperature range	–	–55 to +175	$^{\circ}\text{C}$
$T_{vj(max)}$	Maximum virtual junction temperature	–	175	
T_{stg}	Storage temperature range	–	–55 to +175	
T_{sold}	Soldering temperature	Plastic body for 10s	260	$^{\circ}\text{C}$
T_L		Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10s	300	
F_C	Mounting force	–	50..200 / 11..45	N/lb
V_{ISOL}	Isolation voltage	50/60 Hz; RMS; $I_{ISOL} < 1\text{ mA}$, $t = 1\text{ minute}$	2500	V
F_C	Mounting Force	–	50..200 / 11..45	N/lb
M	Package weight	–	8	g

Thermal Characteristics*

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$R_{th(j-c)}$	Thermal resistance, junction-to-case	–	–	0.14	$^{\circ}\text{C}/\text{W}$
$R_{th(c-s)}$	Thermal resistance, case-to-sink	–	0.05	–	$^{\circ}\text{C}/\text{W}$

*common thermal grease attached

Electrical Characteristics – Static ($T_{vj} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	200	–	–	V
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = V_{DS}$	2.5	–	4.5	V
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	–	–	± 200	nA
I_{DSS}	Drain-source leakage current	$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$	–	–	25	μA
		$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$, $T_{vj} = 150\text{ }^{\circ}\text{C}$	–	–	3	mA
$R_{DS(on)}$	Drain-source on-resistance ¹	$V_{GS} = 10\text{ V}$, $I_D = 100\text{ A}$	–	–	1.99	m Ω

Electrical Characteristics – Dynamic ($T_{vj} = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_{fs}	Transconductance ¹	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	150	200	–	S
$R_{g(int)}$	Gate input resistance	–	–	0.85	–	Ω
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	–	41.5	–	nF
C_{oss}	Output capacitance		–	4.4	–	nF
C_{rss}	Reverse transfer capacitance		–	23	–	pF
$C_{o(er)}$	Effective output capacitance – energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0.8 \times V_{DSS}$	–	2.33	–	nF
$C_{o(tr)}$	Effective output capacitance – time related		–	10.10	–	
Q_G	Total gate charge	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 250\text{ A}$	–	535	–	nC
Q_{GS}	Gate-source charge		–	220	–	
Q_{GD}	Gate-drain charge		–	110	–	
$t_{d(on)}$	Turn-on delay time	Resistive Switching $V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 250\text{ A}, R_{G(ext)} = 10\ \Omega$	–	200	–	ns
t_r	Rise time		–	560	–	
$t_{d(off)}$	Turn-off delay time		–	600	–	
t_f	Fall time		–	485	–	

Source-Drain Diode Characteristics ($T_{vj} = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
I_S	Continuous diode forward current	$V_{GS} = 0\text{ V}$	–	–	500	A
I_{SM}	Diode pulse current	Repetitive, pulse width limited by $T_{vj(max)}$	–	–	2000	A
V_{SD}	Diode forward voltage ¹	$I_F = 100\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.4	V
t_{rr}	Reverse recovery time	$I_F = 200\text{ A}, -di/dt = 200\text{ A}/\mu\text{s},$ $V_R = 100\text{ V}, V_{GS} = 0\text{ V}$	–	250	–	ns
Q_{rr}	Reverse recovery charge		–	2.8	–	μC
I_{rrm}	Reverse recovery current		–	28	–	A

Characteristic Curves

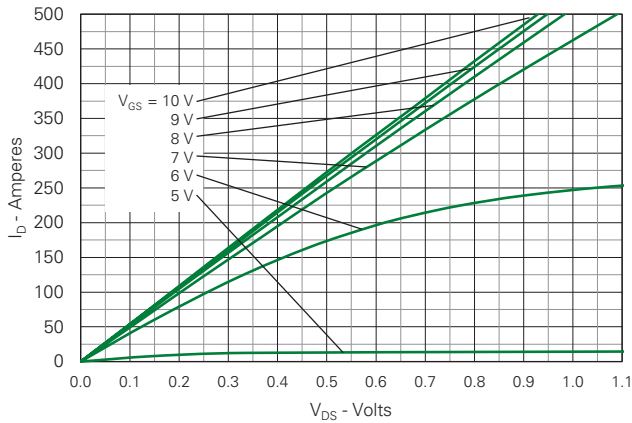
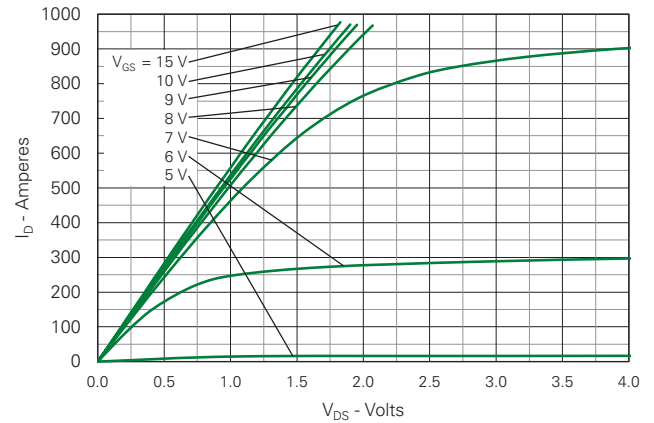
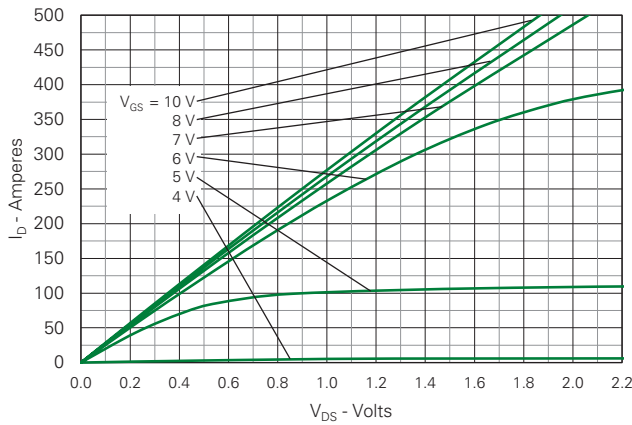
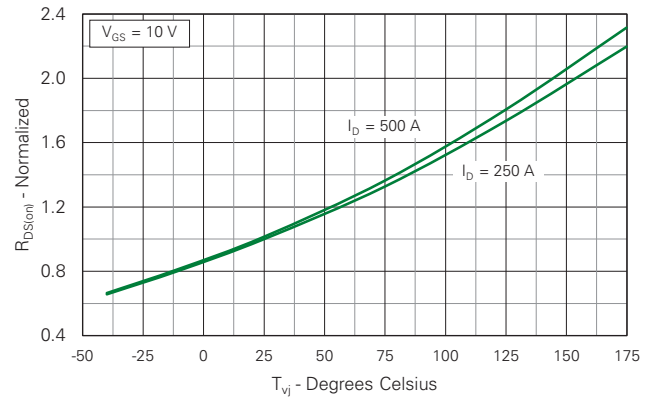
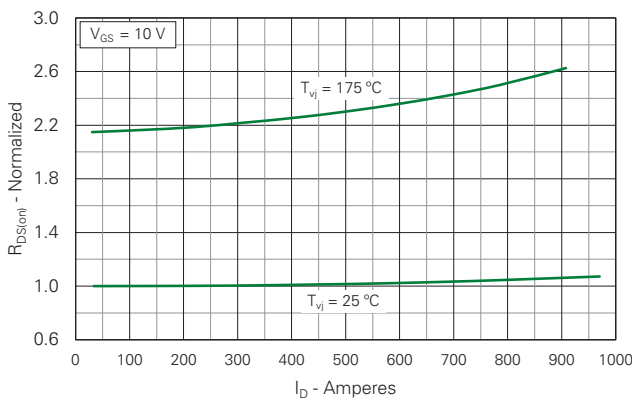
Fig. 1. Output Characteristics @ $T_{vj} = 25^\circ\text{C}$ Fig. 2. Extended Output Characteristics @ $T_{vj} = 25^\circ\text{C}$ Fig. 3. Output Characteristics @ $T_{vj} = 150^\circ\text{C}$ Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 250\text{A}$ Value vs. Junction TemperatureFig. 5. $R_{DS(on)}$ Normalized to $I_D = 250\text{A}$ vs. Drain Current

Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

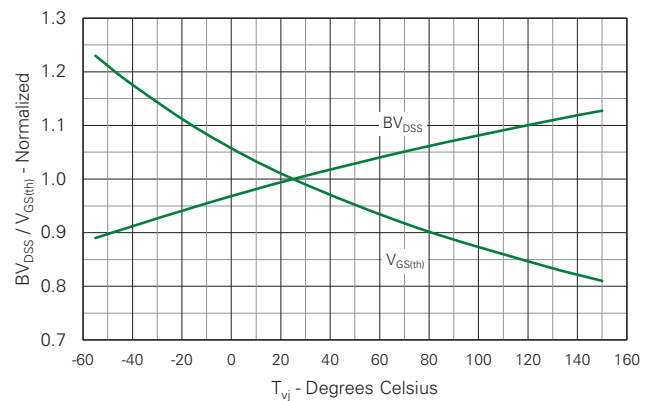


Fig. 7. Drain Current vs. Case Temperature

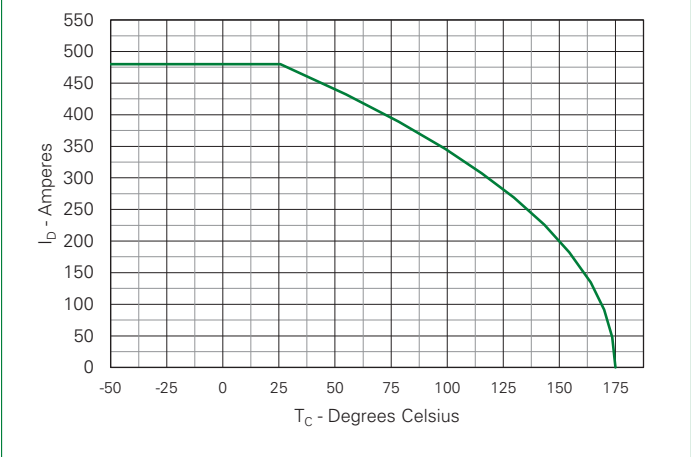


Fig. 8. Input Admittance

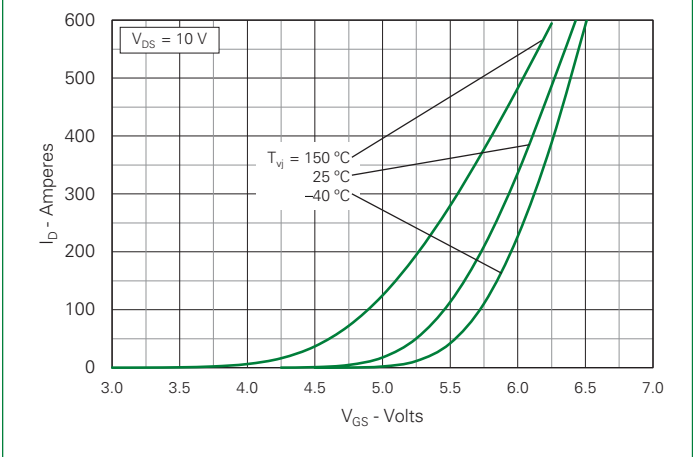


Fig. 9. Transconductance

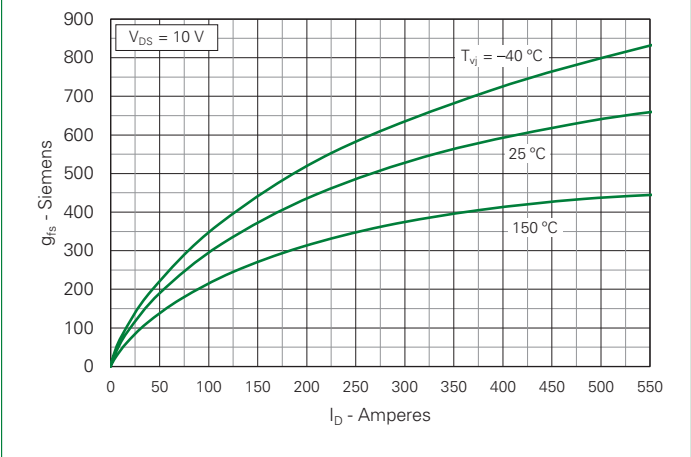


Fig. 10. Forward Voltage Drop of Intrinsic Diode

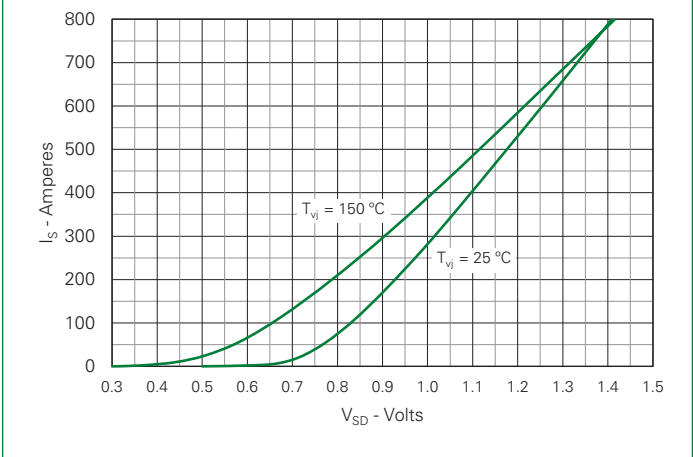


Fig. 11. Gate Charge

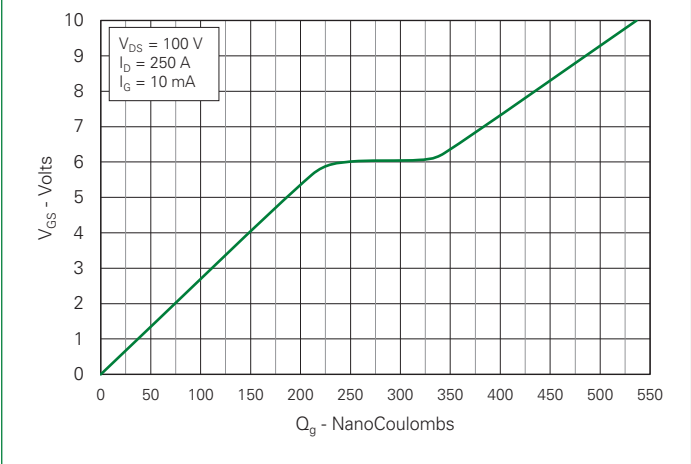


Fig. 12. Capacitance

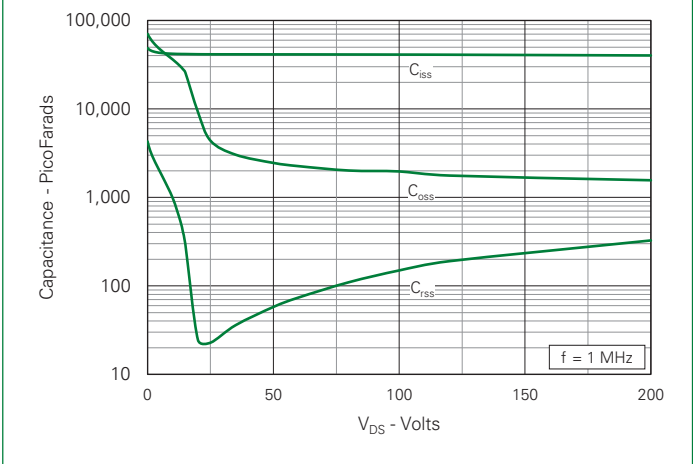


Fig. 13. Output Capacitance Stored Energy

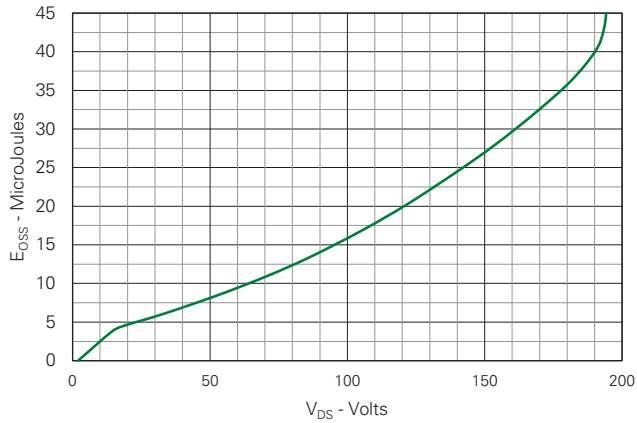


Fig. 14. Forward-Bias Safe Operating Area

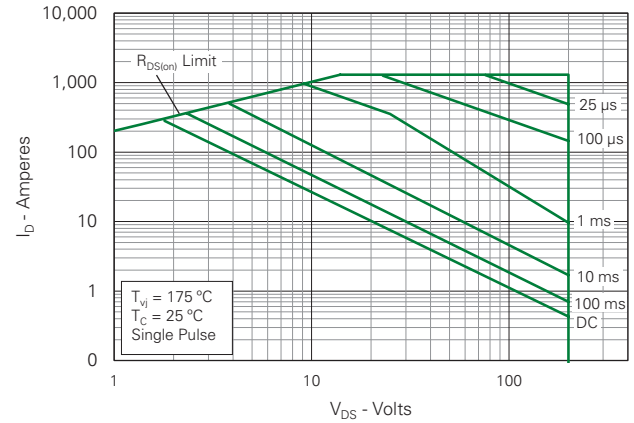
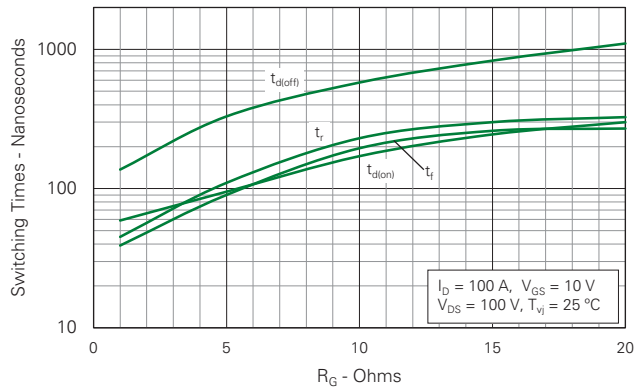
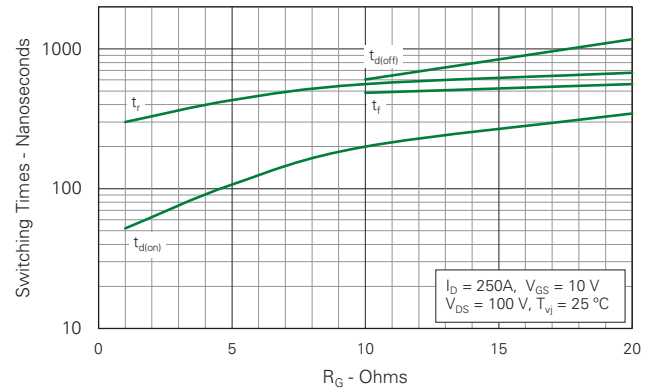
Fig. 15. Resistive Switching Times vs. Gate Resistance @ $I_D = 100$ AFig. 16. Resistive Switching Times vs. Gate Resistance @ $I_D = 250$ A

Fig. 17. Resistive Switching Times vs. Drain Current

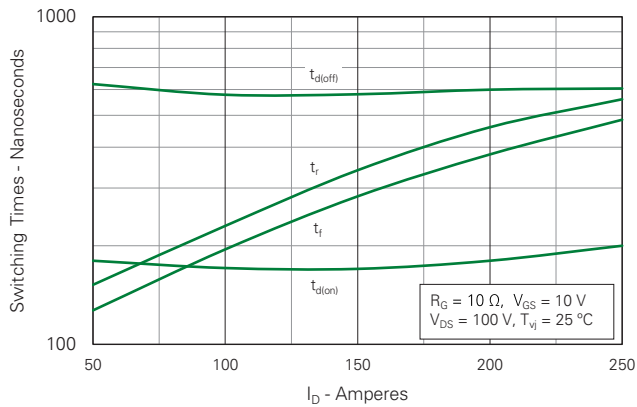
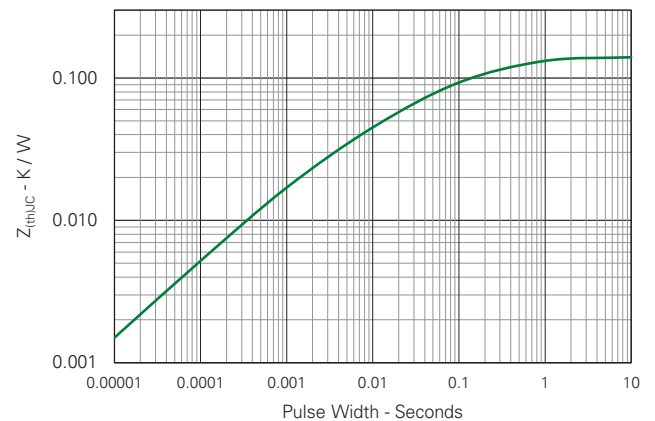
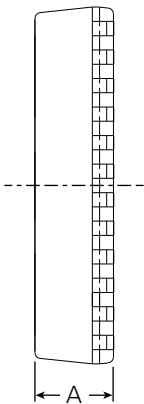
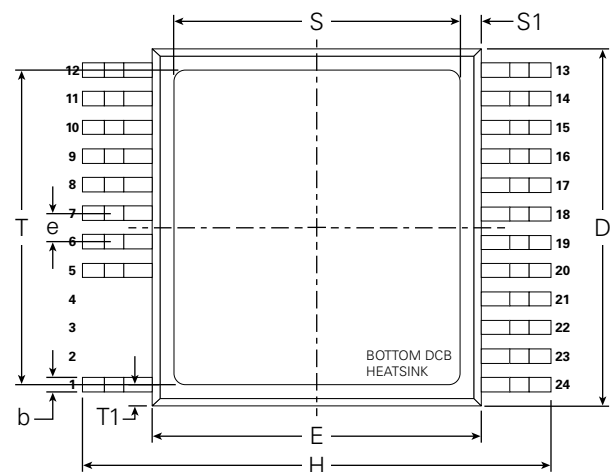


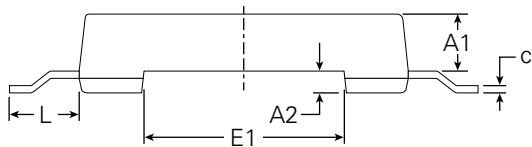
Fig. 18. Maximum Transient Thermal Impedance



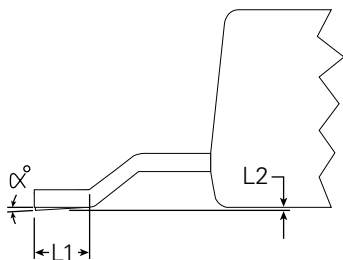
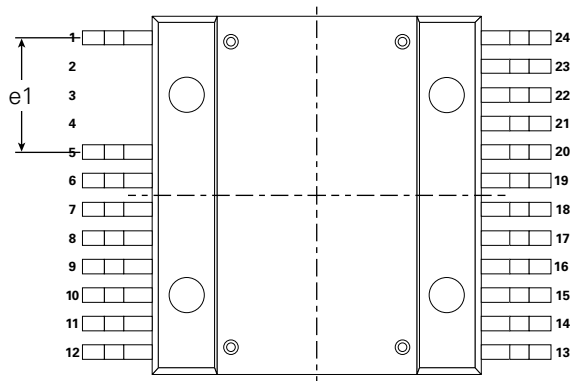
Part Outline Drawing (SMPD-X)



1 - Gate
5-12 - Source
13-24 - Drain
Tab - Isolated



Note:
1. Bottom heatsink meets 2.6 kV AC isolation to the other pins.
2. All leads are matte pure tin plated.



Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.209	–	0.224	5.30	–	5.70
A1	0.154	–	0.161	3.90	–	4.10
A2	0.055	–	0.063	1.40	–	1.60
b	0.035	–	0.045	0.90	–	1.15
c	0.018	–	0.026	0.45	–	0.65
D	0.976	–	0.994	24.80	–	25.25
E	0.898	–	0.915	22.80	–	23.25
E1	0.543	–	0.559	13.80	–	14.20
e	0.079 BSC			2.00 BSC		
e1	0.315 BSC			8.00 BSC		
H	1.272	–	1.311	32.30	–	33.30
L	0.181	–	0.209	4.60	–	5.30
L1	0.051	–	0.067	1.30	–	1.70
L2	0.000	–	0.006	0.00	–	0.15
S	0.742	–	0.792	18.85	–	20.12
S1	0.057	–	0.082	1.45	–	2.08
T	0.823	–	0.873	20.90	–	22.17
T1	0.056	–	0.080	1.42	–	2.03
a	4°	–	–	4°	–	–

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