IAUCN04S7L025AH

Automotive MOSFET

Optimos™ 7 Power-Transistor

RoHS

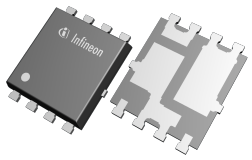
Infineon Automotive Quality

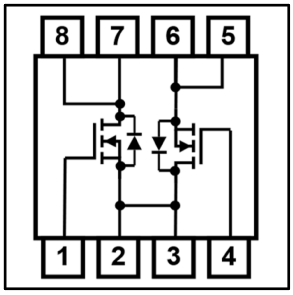
AEC Qualified

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

PG-TDSON-8-57





Potential Applications

General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	40	V
$R_{DS(on),\,M1}$	2.56	mΩ
$R_{DS(on),\,M2}$	5.04	mΩ
I_D (chip limited) M1	127	A
I_D (chip limited) M2	65	A

Pin Assignment

Function	Symbol	Pin
Gate M1	G1	1
Source M1, Drain M2	S1, D2	2, 3
Gate M2	G2	4
Source M2	S2	5, 6
Drain M1	D1	7, 8

Type	Package	Marking
IAUCN04S7L025AH	PG-TDSON-8-57	7N4L02AH

Table of Contents

Maximum Ratings

at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			M1	M2	
Continuous drain current	I_D	V_{GS} = 10 V, Chip limitation[1,2)]	127	65	A
		V_{GS} = 10 V, DC current	100	65	
		T_a = 100°C, V_{GS} = 10 V, R_{thJA} on 2s2p[2,3)]	20	14	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C = 25°C, t_p = 100 µs	349	149	
Avalanche energy, single pulse[2)]	E_{AS}	$I_{D,M1}$ = 38 A, $I_{D,M2}$ = 14 A	58	25	mJ
Avalanche current, single pulse	I_{AS}	–	75	27	A
Gate source voltage	V_{GS}	–	±16		V
		Limited to duty factor of 1%	+20		
Power dissipation	P_{tot}	T_C = 25°C	75	40	W
Operating temperature	T_j	–	-55 ... +175		°C

Thermal Characteristics[2)]

Parameter	M1/M2	Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Thermal resistance, junction - case	M1	R_{thJC}	–	–	–	2	K/W
	M2			–	–	3.7	
Thermal resistance, junction - ambient[3)]	M1	R_{thJA}	–	–	41	–	
	M2			–	43	–	

Electrical characteristics

at T_j=25 °C, unless otherwise specified

Parameter	M1/M2	Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Static characteristics							
Drain-source breakdown voltage	M1	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = 1 mA	40	–	–	V
	M2						
Gate threshold voltage	M1	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 25 µA	1.2	1.5	1.8	
	M2		V_{GS} = V_{DS}, I_D = 10 µA	1.2	1.5	1.8	
Zero gate voltage drain current	M1	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V, T_j = 25°C[2)]	–	–	1	µA
	M2						
	M1		V_{DS} = 40 V, V_{GS} = 0 V, T_j = 100°C[2)]	–	–	6	
	M2			–	–	3	
Gate-source leakage current	M1	I_{GSS}	V_{GS} = 16 V, V_{DS} = 0 V	–	–	100	nA
	M2						
Drain-source on-state resistance	M1	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 50 A	–	3.04	3.43	mΩ
	M2		V_{GS} = 4.5 V, I_D = 30 A	–	6.46	7.49	
	M1		V_{GS} = 10 V, I_D = 50 A	–	2.34	2.56	
	M2		V_{GS} = 10 V, I_D = 30 A	–	4.46	5.04	
Gate resistance[2)]	M1	R_G	–	–	1.4	–	Ω
	M2		–	–	2	–	

[1)] Practically the current is limited by the overall system design including the customer-specific PCB.

[2)] The parameter is not subject to production testing – specified by design.

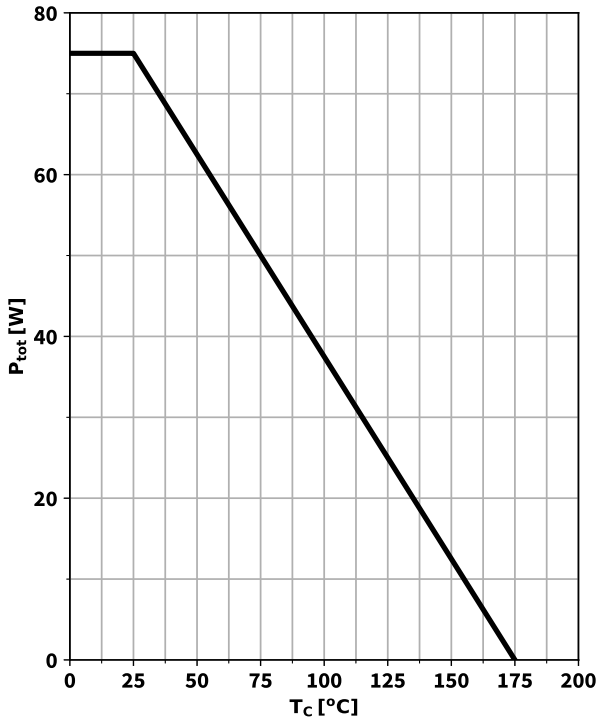
[3)] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Parameter	M1/M2	Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Dynamic Characteristics[2]							
Input capacitance	M1	C_{iss}	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz	–	1937	2518	pF
	M2			–	704	915	
Output capacitance	M1	C_{oss}		–	970	1261	
	M2			–	349	454	
Reverse transfer capacitance	M1	C_{oss}		–	35	53	
	M2			–	16	24	
Turn-on delay time	M1	$t_{d(on)}$	V_{DD} = 20 V, V_{GS} = 10 V, $I_{D,M1}$ = 50 A, $I_{D,M2}$ = 30 A, R_G = 3.5 Ω	–	4.5	–	ns
	M2			–	2.5	–	
Rise time	M1	t_r		–	10	–	
	M2			–	6	–	
Turn-off delay time	M1	$t_{d(off)}$		–	21	–	
	M2			–	9	–	
Fall time	M1	t_f		–	25	–	
	M2			–	12	–	
Gate Charge Characteristics[2]							
Gate to source charge	M1	Q_{gs}	V_{DD} = 20 V, $I_{D,M1}$ = 50 A, $I_{D,M2}$ = 30 A, V_{GS} = 0 to 10 V	–	5.5	7.2	nC
	M2			–	2.1	2.7	
Gate to drain charge	M1	Q_{gd}		–	5.1	7.7	
	M2			–	1.9	2.9	
Gate charge total	M1	Q_g		–	29	38	
	M2			–	11	14	
Gate plateau voltage	M1	$V_{plateau}$		–	2.8	–	V
	M2			–	3	–	
Reverse Diode							
Diode continuous forward current[2]	M1	I_S	T_C = 25°C	–	–	100	A
	M2			–	–	65	
Diode pulse current[2]	M1	$I_{S,pulse}$	T_C = 25°C, t_p = 100 µs	–	–	349	
	M2			–	–	149	
Diode forward voltage	M1	V_{SD}	V_{GS} = 0 V, $I_{F,M1}$ = 50 A, $I_{F,M2}$ = 30 A, T_j = 25° C	–	0.87	1.02	V
	M2			–	0.87	1.02	
Reverse recovery time[2]	M1	t_{rr}	V_R = 20 V, I_F = 50 A, di_F/dt = 100 A/µs	–	23	35	ns
Reverse recovery charge[2]		Q_{rr}		–	8	16	nC
Reverse recovery time[2]	M2	t_{rr}	V_R = 20 V, I_F = 50 A, di_F/dt = 100 A/µs	–	6	9	ns
Reverse recovery charge[2]		Q_{rr}		–	0.5	1	nC

Electrical characteristics diagrams

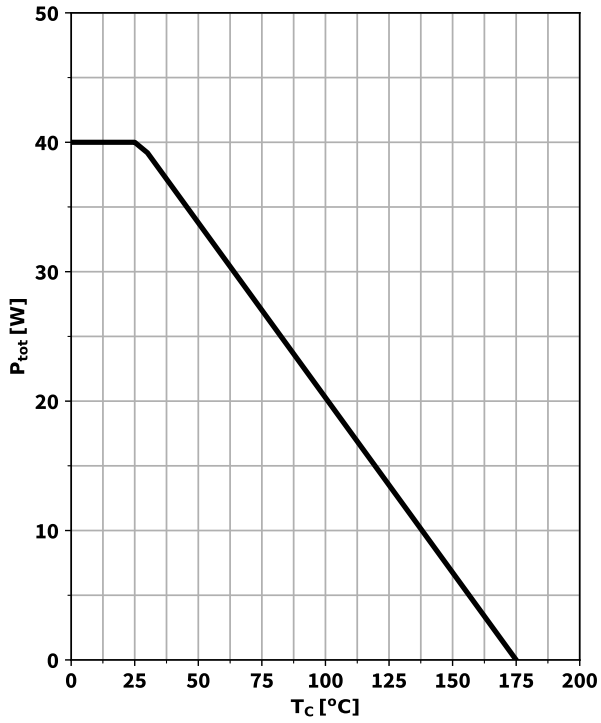
1 Power dissipation M1

$P_{tot} = f(T_C); V_{GS} \geq 6\ V$



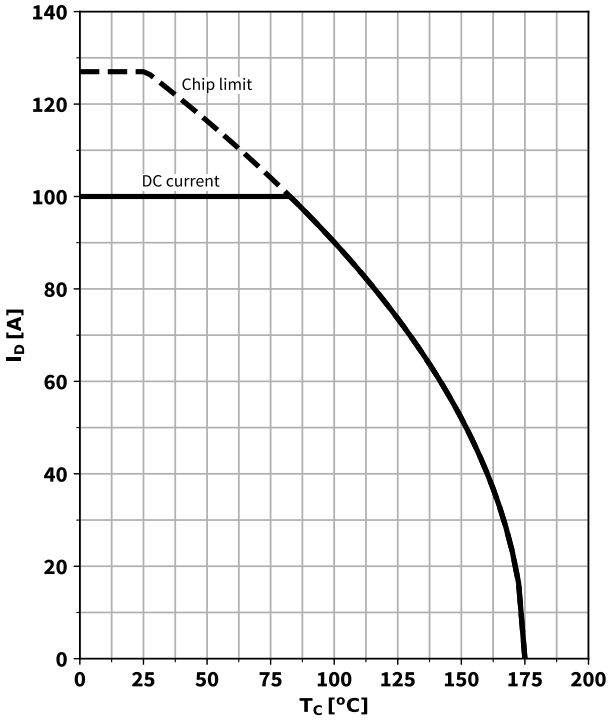
2 Power dissipation M2

$P_{tot} = f(T_C); V_{GS} \geq 6\ V$



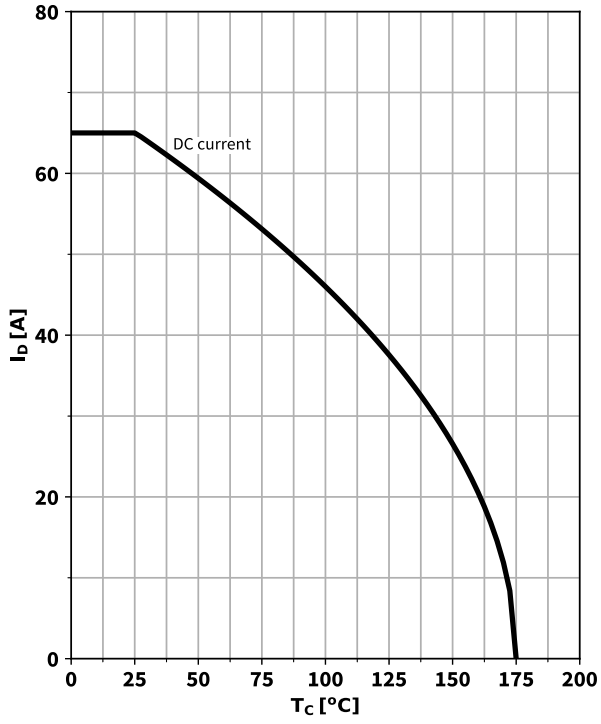
3 Drain current M1

$I_D = f(T_C); V_{GS} \geq 6\ V$



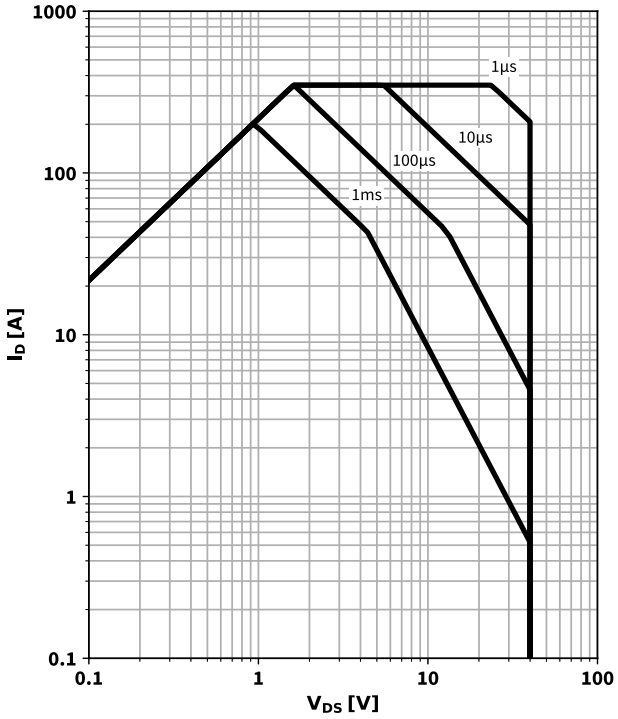
4 Drain current M2

$I_D = f(T_C); V_{GS} \geq 6\ V$



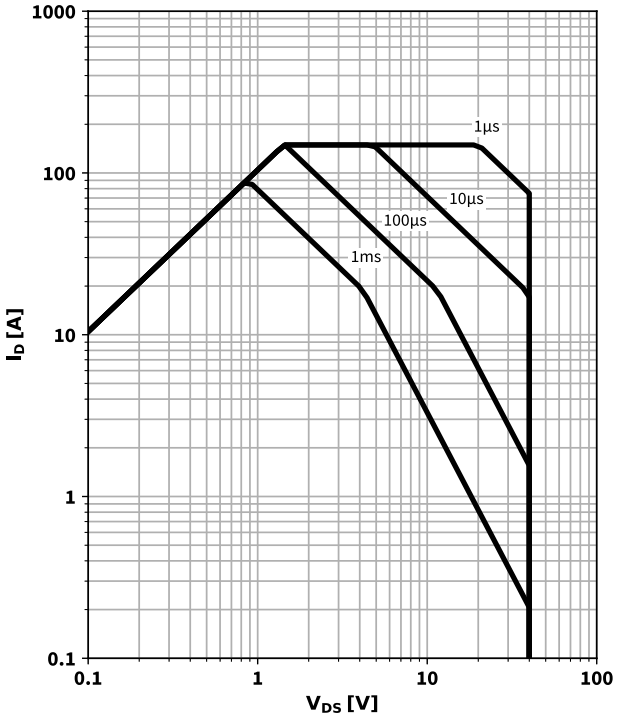
5 Safe operating area M1

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



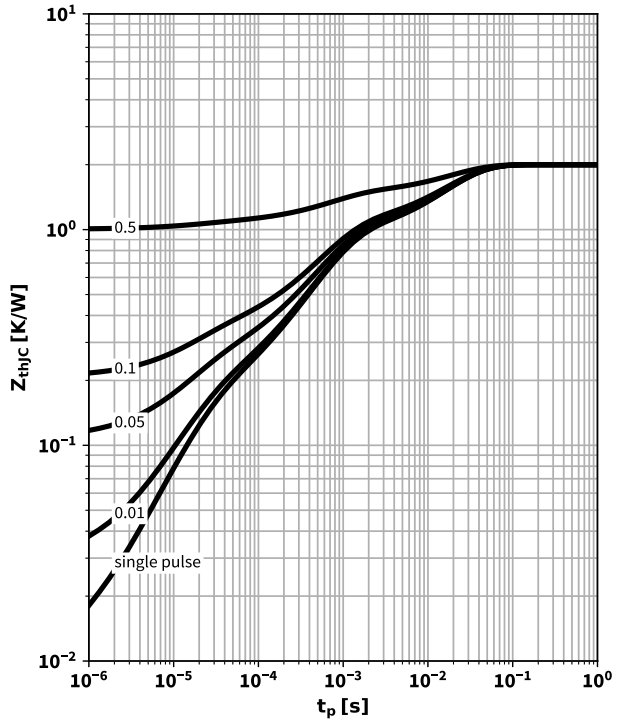
6 Safe operating area M2

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



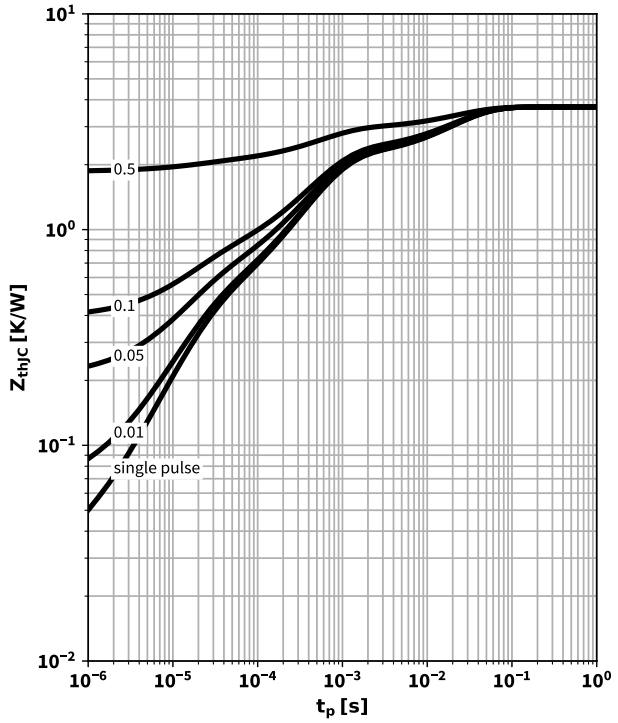
7 Max. transient thermal impedance M1

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



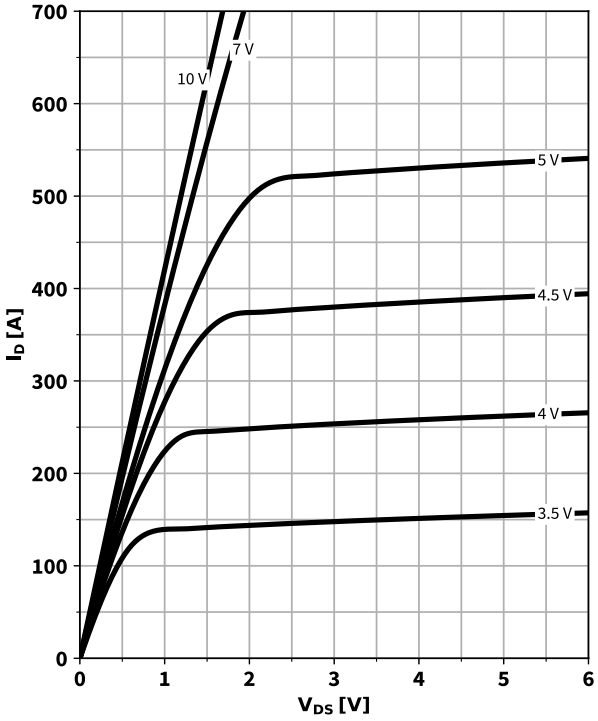
8 Max. transient thermal impedance M2

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



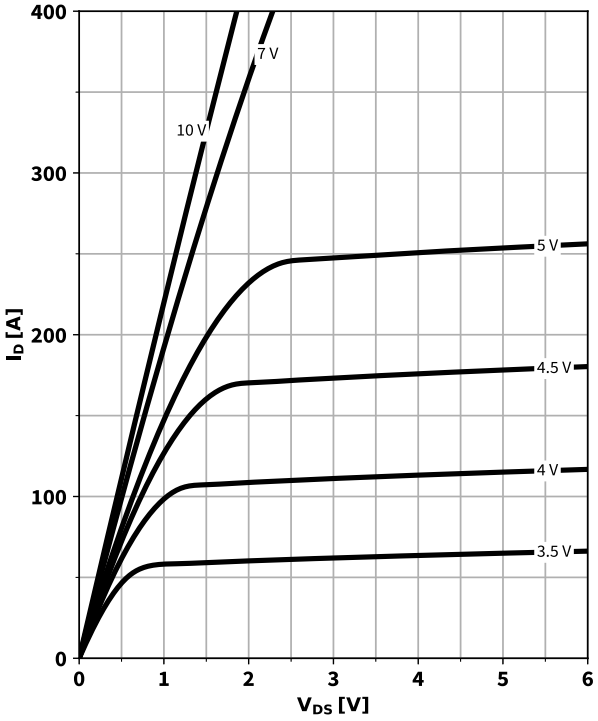
9 Typ. output characteristics M1

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



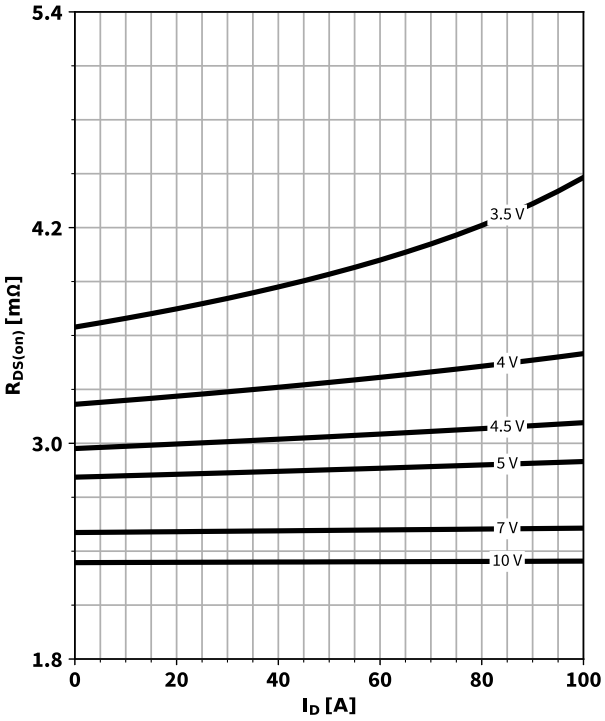
10 Typ. output characteristics M2

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



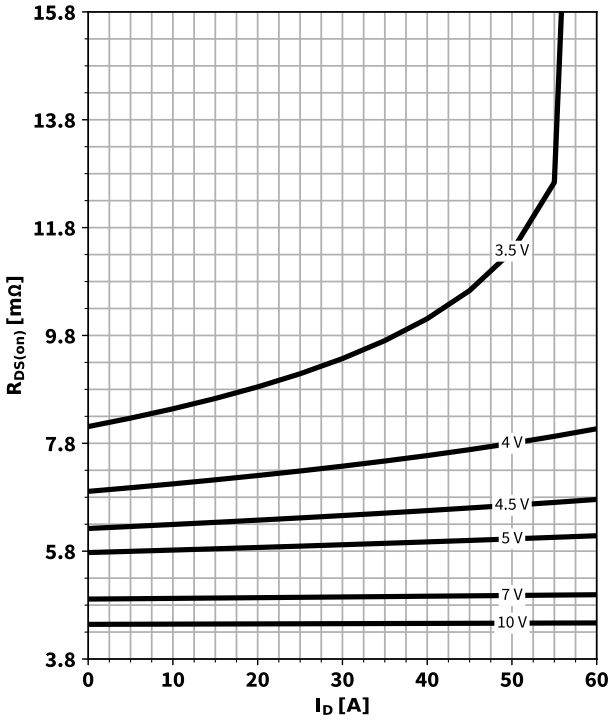
11 Typ. drain-source on-state resistance M1

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



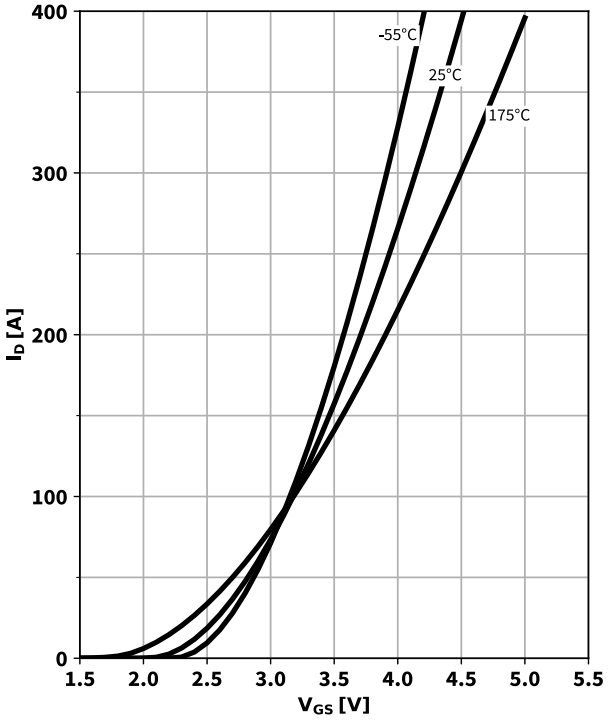
12 Typ. drain-source on-state resistance M2

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



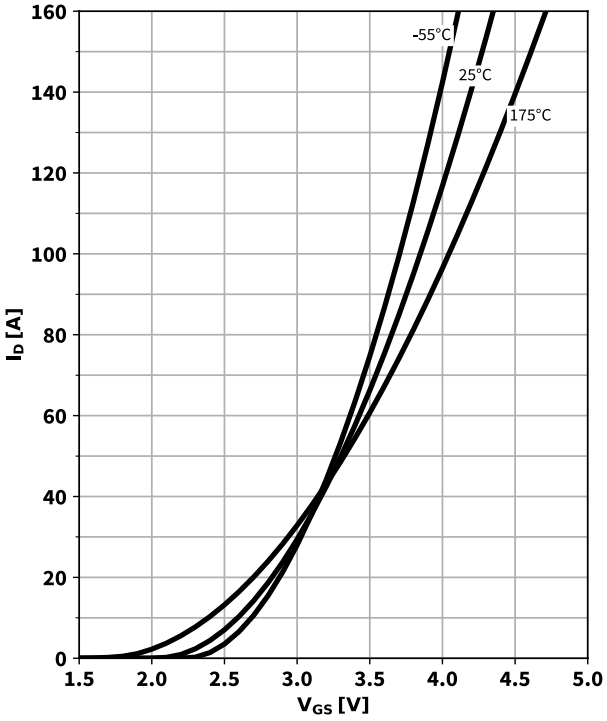
13 Typ. transfer characteristics M1

$I_D = f(V_{GS})$; V_{DS} = 6 V; parameter: T_j



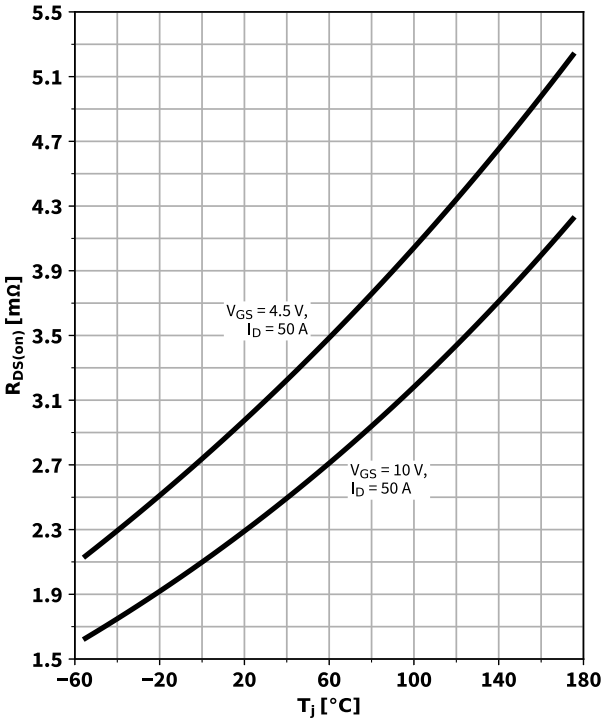
14 Typ. transfer characteristics M2

$I_D = f(V_{GS})$; V_{DS} = 6 V; parameter: T_j



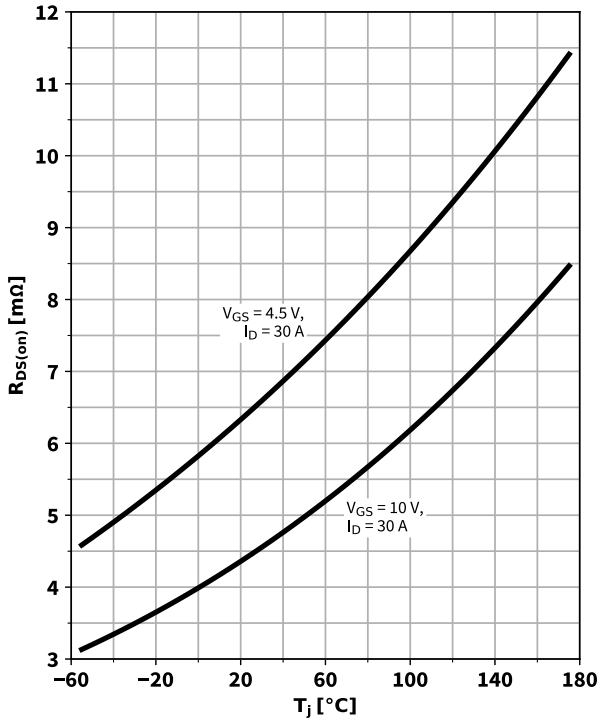
15 Typ. drain-source on-state resistance M1

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



16 Typ. drain-source on-state resistance M2

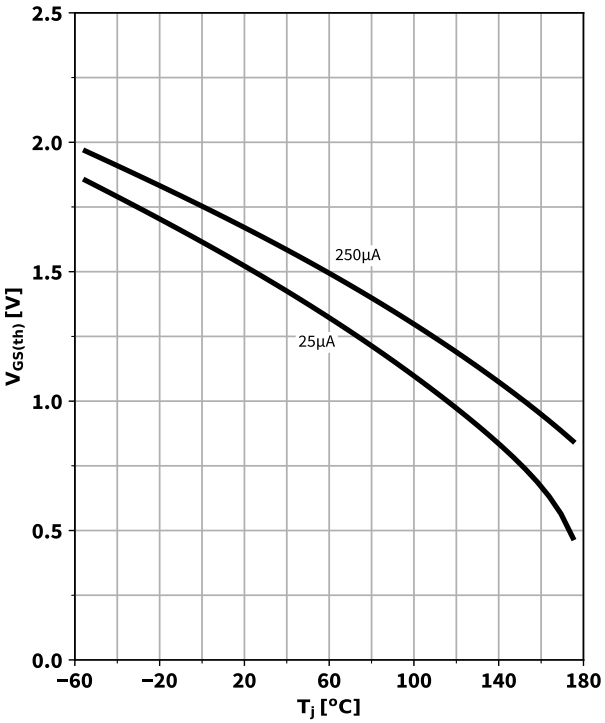
$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



Electrical characteristics diagrams

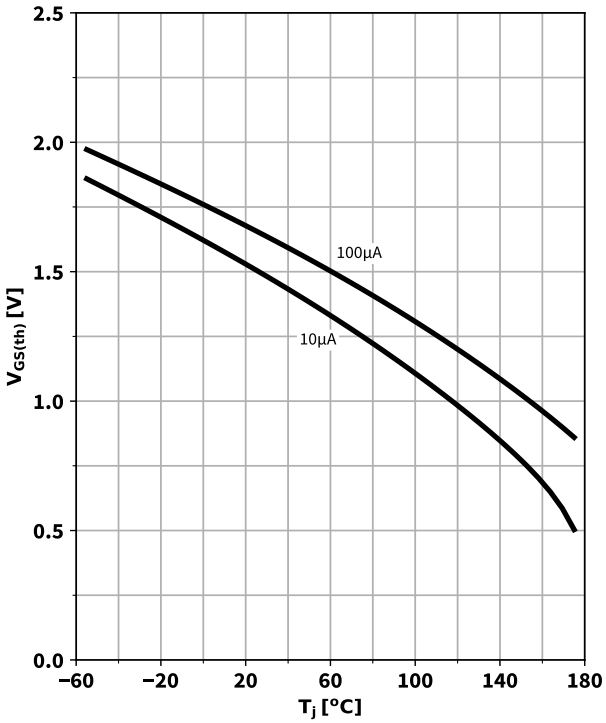
17 Typ. gate threshold voltage M1

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



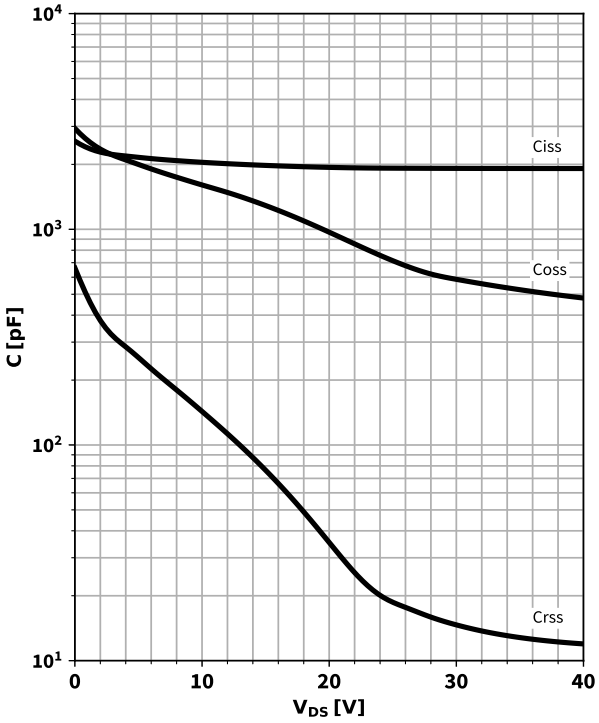
18 Typ. gate threshold voltage M2

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



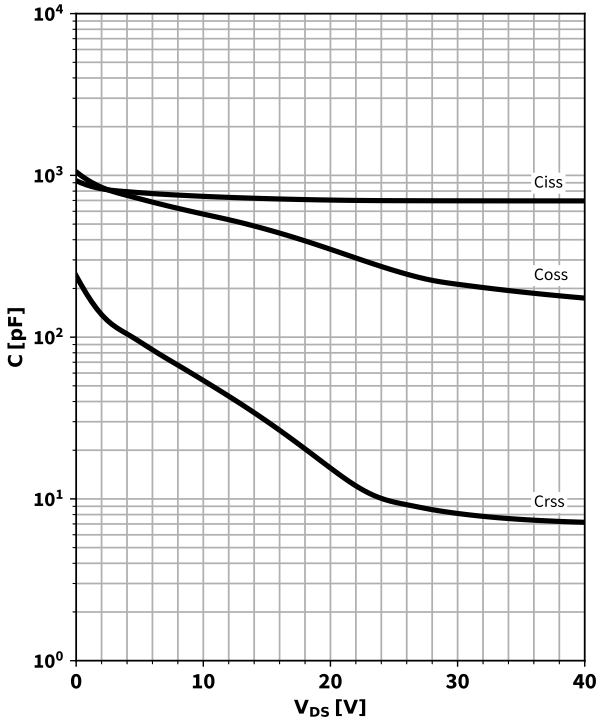
19 Typ. capacitances M1

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



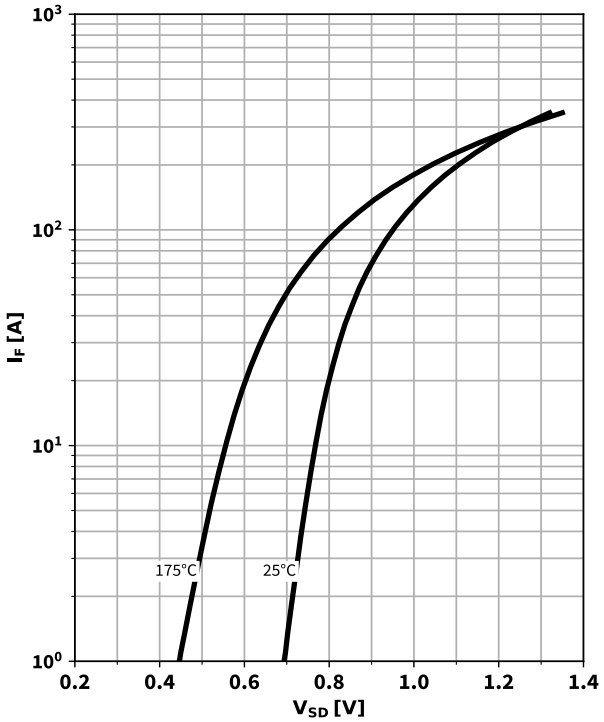
20 Typ. capacitances current M2

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



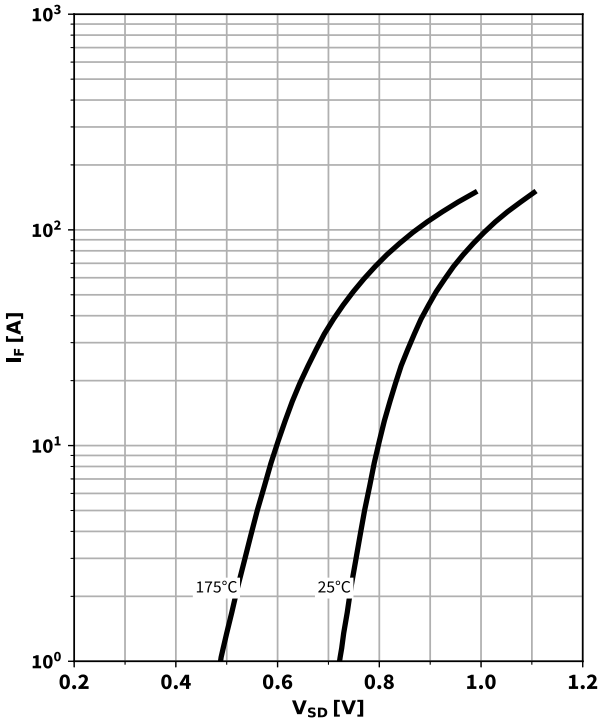
21 Typ. forward diode characteristics M1

$I_F = f(V_{SD})$; parameter: T_j



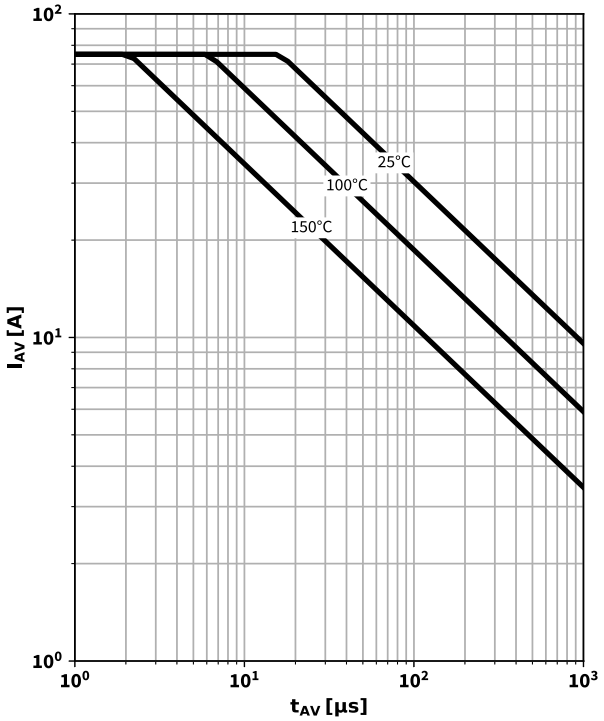
22 Typ. forward diode characteristics M2

$I_F = f(V_{SD})$; parameter: T_j



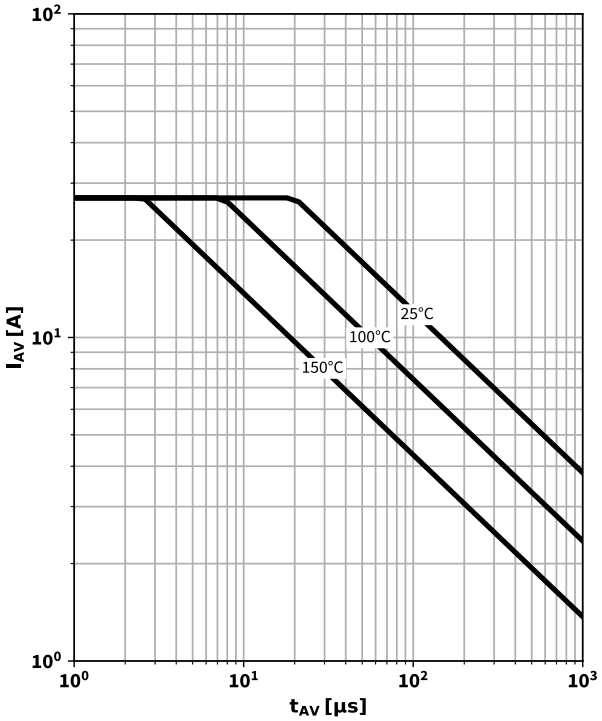
23 Typ. avalanche characteristics M1

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



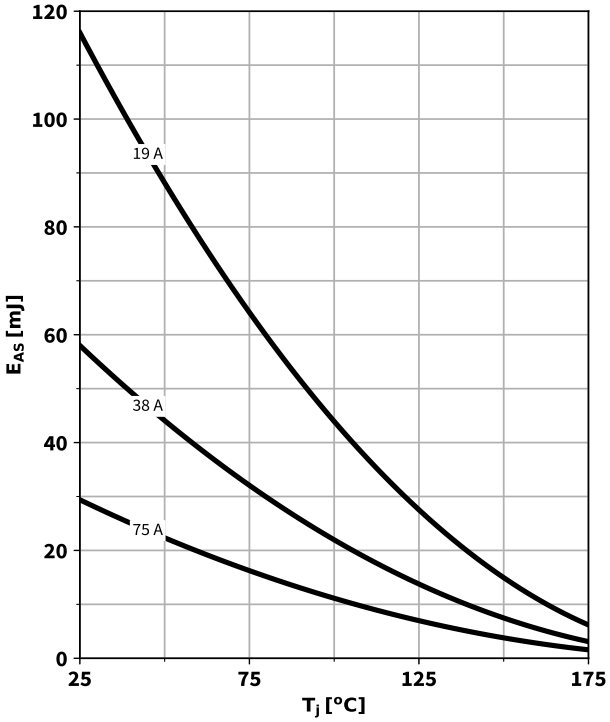
24 Typ. avalanche characteristics M2

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



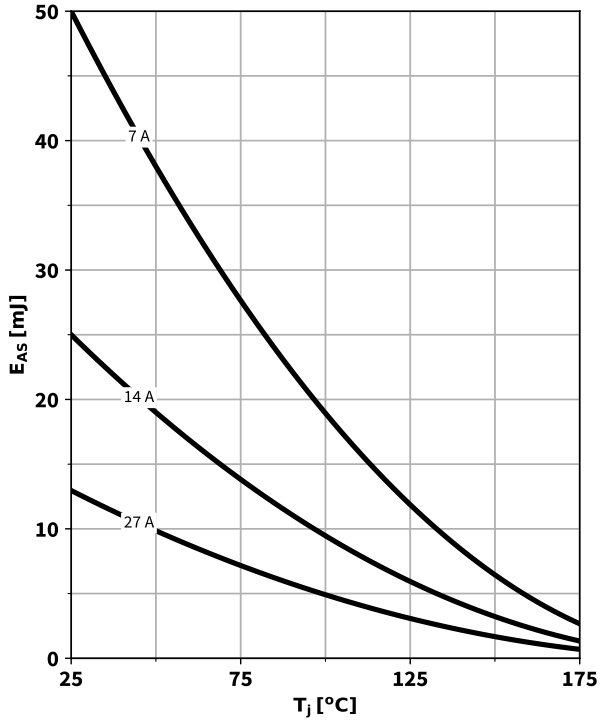
25 Typical avalanche energy M1

$E_{AS} = f(T_j)$; parameter: I_D



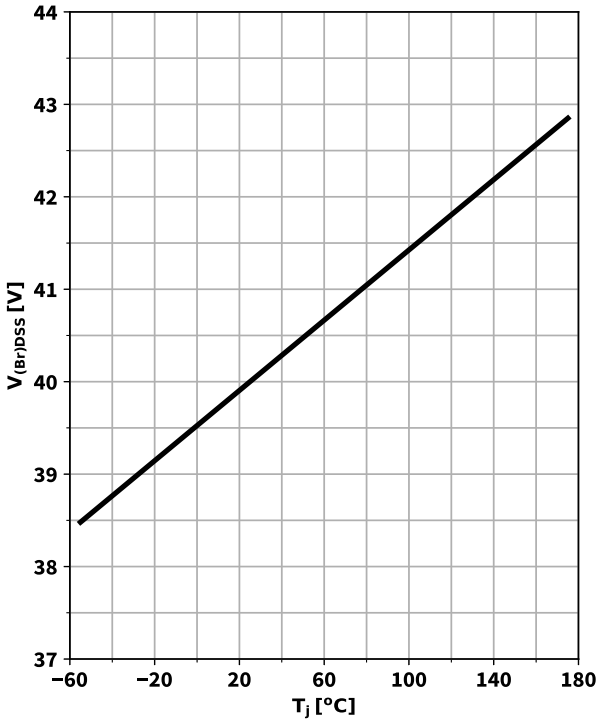
26 Typical avalanche energy M2

$E_{AS} = f(T_j)$; parameter: I_D



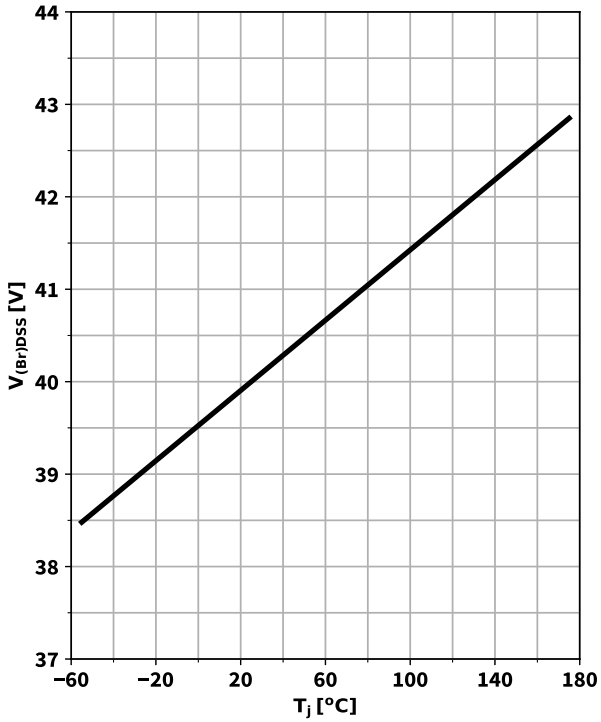
27 Drain-source breakdown voltage M1

$V_{(Br)DSS} = f(T_j)$; I_D = 1 mA



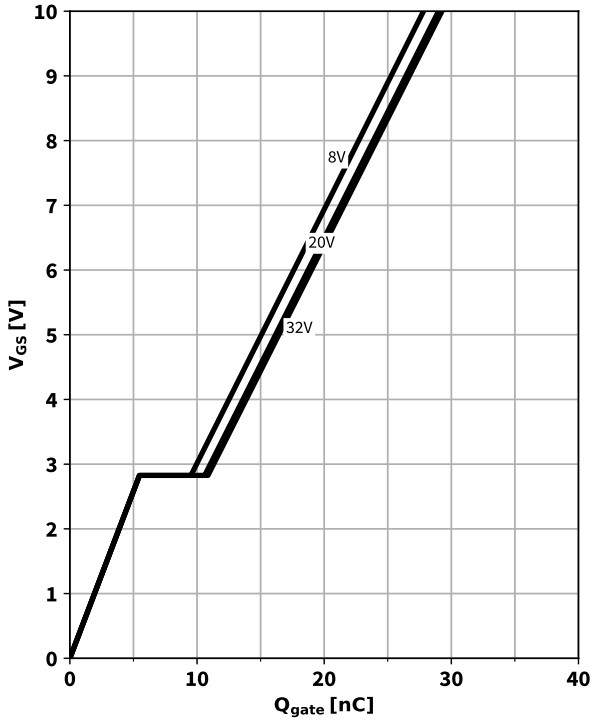
28 Drain-source breakdown voltage M2

$V_{(Br)DSS} = f(T_j)$; I_D = 1 mA



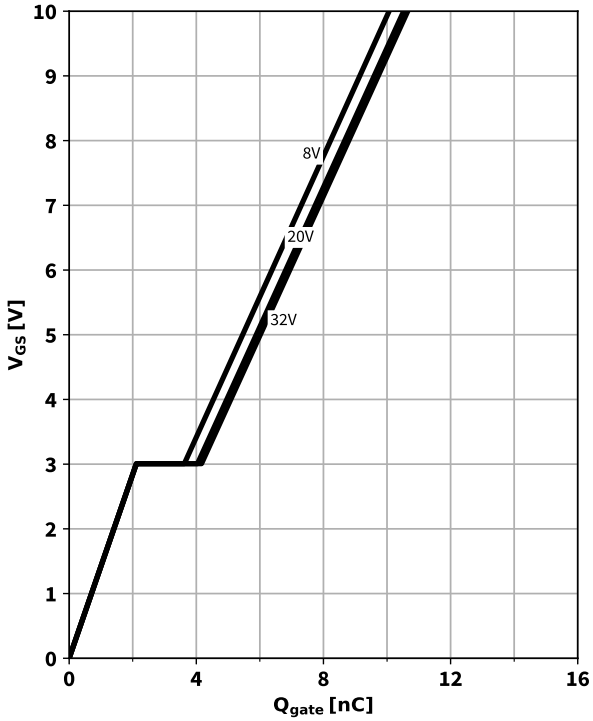
29 Typ. gate charge M1

V_{GS} = f(Q_{gate}); I_D = 50 A pulsed; parameter: V_{DD}

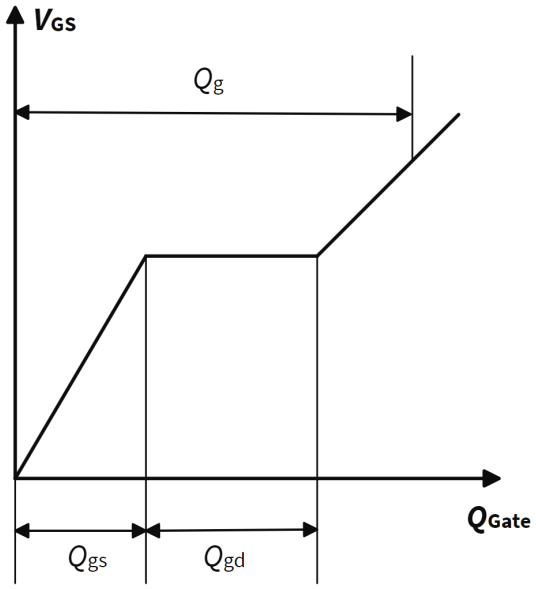


30 Typ. gate charge M2

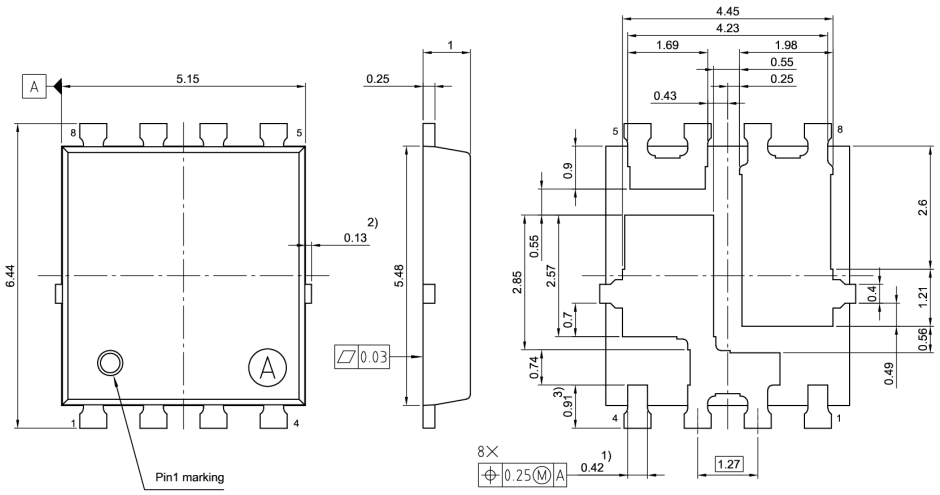
V_{GS} = f(Q_{gate}); I_D = 30 A pulsed; parameter: V_{DD}



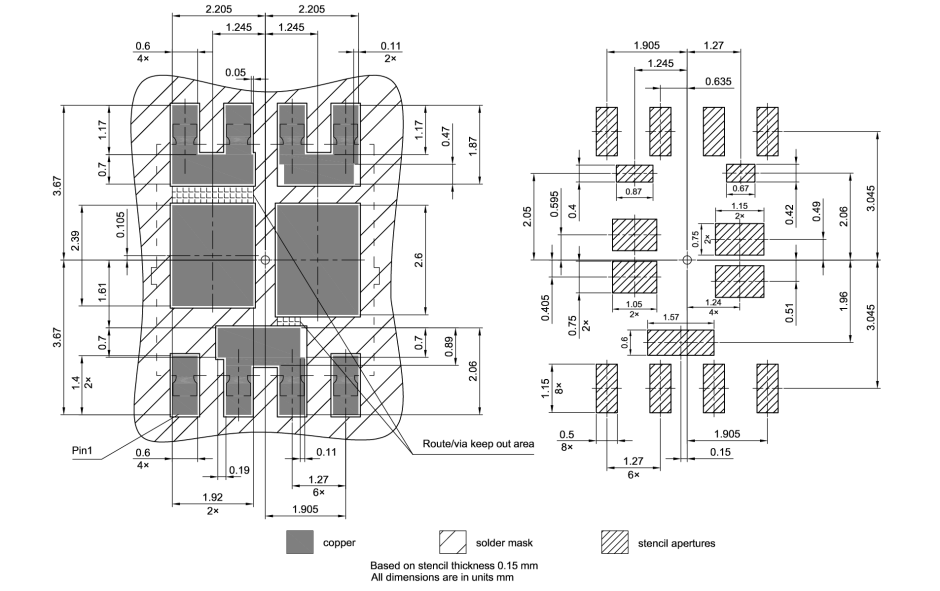
31 Gate charge waveforms M1, M2



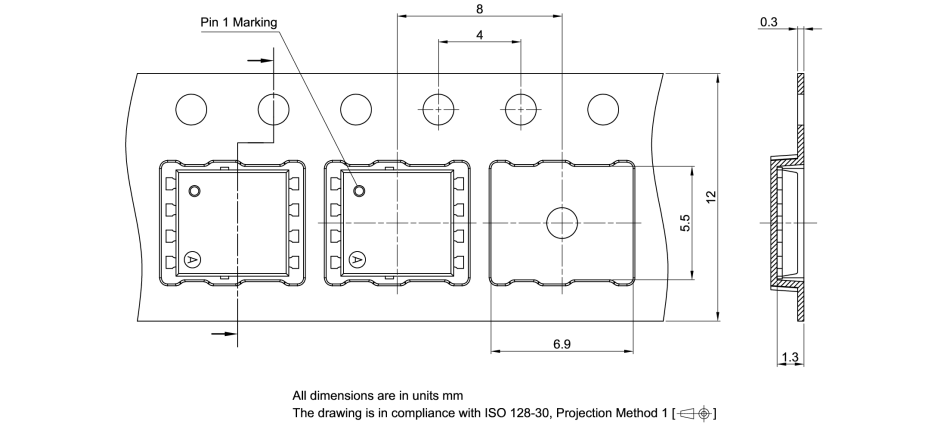
Package Outline



Footprint



Packaging



Revision History

Revision	Date	Changes
Revision 1.0	2025-04-11	Final Data Sheet

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