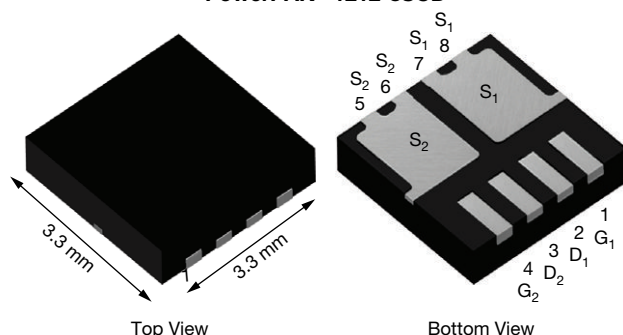


Common Drain Dual N-Channel 12 V (S1-S2) MOSFET

PowerPAK® 1212-8SCD


FEATURES

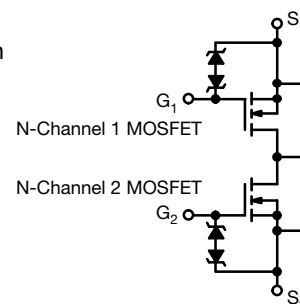
- TrenchFET® Gen IV power MOSFET
- Very low source-to-source on resistance
- Integrated common-drain n-channel MOSFETs in a compact and thermally enhanced package
- 100 % R_g and UIS tested
- Optimizes circuit layout for bi-directional current flow
- Typical ESD protection: 4500 V (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Battery protection switch
- Bi-directional switch
- Load switch



PRODUCT SUMMARY	
V_{S1S2} (V)	12
$R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0036
$R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 3.8$ V	0.0041
$R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.0050
$R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 1.8$ V	0.0074
Q_g typ. (nC) at $V_{GS} = 2.5$ V	25
I_{S1S2} (A) ^a	109
Configuration	Common drain

ORDERING INFORMATION	
Package	PowerPAK 1212-8SCD
Lead (Pb)-free and halogen-free	SiSF12EDN-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{S1S2}	12	V
Gate-source voltage	V_{GS}	± 8	
Continuous drain current ($V_{GS} = 5$ V, $T_J = 150$ °C)	$T_C = 25$ °C	109	A
	$T_C = 70$ °C	87	
	$T_A = 25$ °C	30 ^{b, c}	
	$T_A = 70$ °C	24 ^{b, c}	
Pulsed drain current ($t = 100$ μ s, $V_{GS} = 5$ V)	I_{S1S2M}	200	mJ
Single pulse avalanche current, $L = 0.1$ mH		15	
Single pulse avalanche energy, $L = 0.1$ mH		11.25	W
Maximum power dissipation	$T_C = 25$ °C	69.4	
	$T_C = 70$ °C	44.4	
	$T_A = 25$ °C	5.2 ^{b, c}	
	$T_A = 70$ °C	3.3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^a	$t \leq 10$ s	R_{thJA}	19	24	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.4	1.8	

Note

a. Surface mounted on 1" x 1" FR4 board

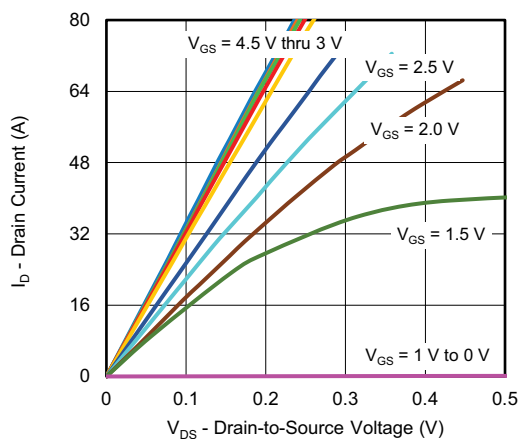
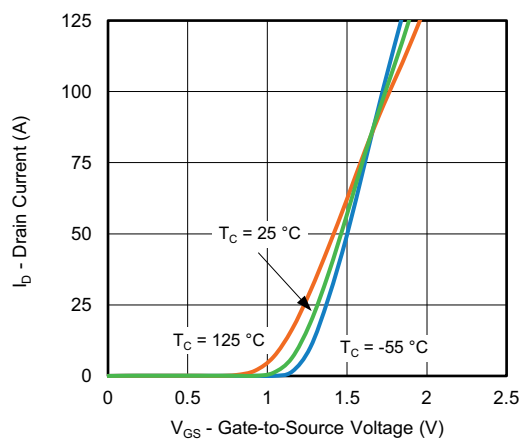
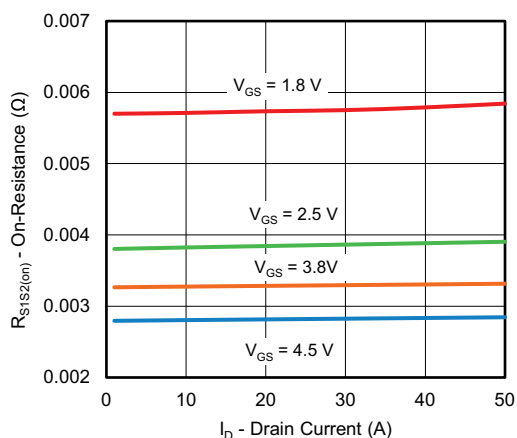
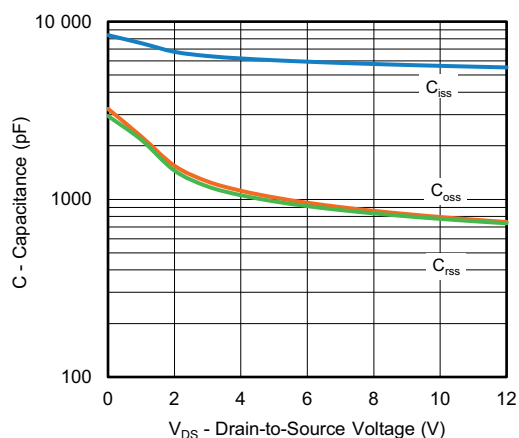
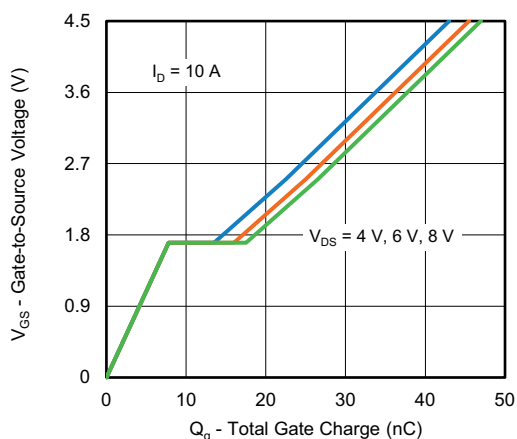
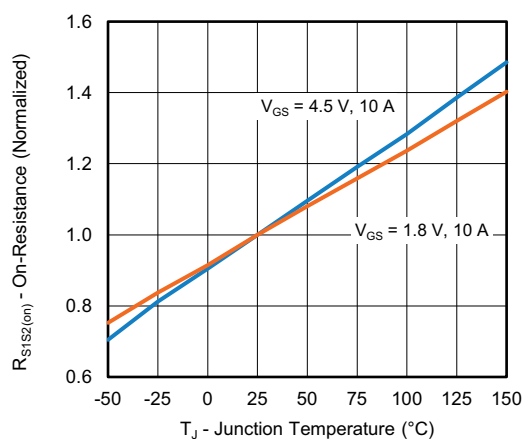
SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	12	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{S1S2} = V _{GS} , I _D = 250 μA	0.4	-	1.0		
Gate-source leakage	I _{GSS}	V _{S1S2} = 0 V, V _{GS} = ± 5 V	-	-	± 1	μA	
		V _{S1S2} = 0 V, V _{GS} = ± 8 V	-	-	± 30		
Zero gate voltage drain current	I _{DSS}	V _{S1S2} = 12 V, V _{GS} = 0 V	-	-	1		
		V _{S1S2} = 12 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15		
Drain-source on-state resistance ^a	R _{S1S2(on)}	V _{GS} = 4.5 V, I _{S1S2} = 10 A	-	0.0030	0.0036	Ω	
		V _{GS} = 3.8 V, I _{S1S2} = 10 A	-	0.0033	0.0041		
		V _{GS} = 2.5 V, I _{S1S2} = 10 A	-	0.0039	0.0050	Ω	
		V _{GS} = 1.8 V, I _{S1S2} = 10 A	-	0.0058	0.0074		
Forward transconductance ^a	g _{fs}	V _{S1S2} = 6 V, I _{S1S2} = 10 A	-	75	-	S	
Dynamic ^{b, c}							
Input capacitance	C _{iss}	V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz	-	5950	-	pF	
Output capacitance	C _{oss}		-	940	-		
Reverse transfer capacitance	C _{rss}		-	895	-		
Total gate charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 10 A	-	45.5	70	nC	
Gate-source charge	Q _{gs}	V _{DS} = 6 V, V _{GS} = 2.5 V, I _D = 10 A	-	25	38		
Gate-drain charge	Q _{gd}		-	7.8	-		
Gate resistance	R _g		-	8.2	-		
Turn-on delay time	t _{d(on)}	f = 1 MHz	0.4	1.0	1.7	Ω	
Rise time	t _r		V _{DD} = 6 V, R _L = 0.6 Ω, I _{S1S2} ≡ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	22	45	ns
Turn-off delay time	t _{d(off)}			-	197	395	
Fall time	t _f			-	50	100	
		-		45	90		
Drain-Source Body Diode Characteristics ^c							
Continuous source-drain diode current	I _{S1S2}	T _C = 25 °C	-	-	63	A	
Pulse diode forward current	I _{S1S2M}		-	-	200		
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	23	46	ns	
Body diode reverse recovery charge	Q _{rr}		-	12	25	nC	
Reverse recovery fall time	t _a		-	12	-	ns	
Reverse recovery rise time	t _b		-	11	-		

Notes

- b. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
c. Guaranteed by design, not subject to production testing
d. On single MOSFET

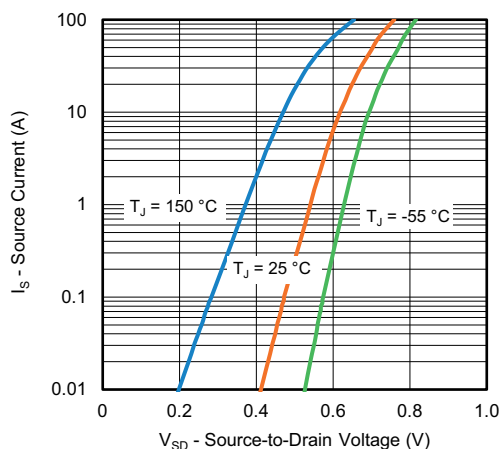
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Source Current and Gate Voltage

Capacitance ^a

Gate Charge ^a

On-Resistance vs. Junction Temperature
Note

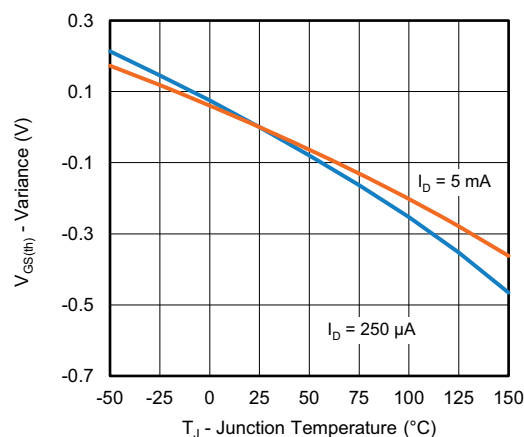
a. For one channel only



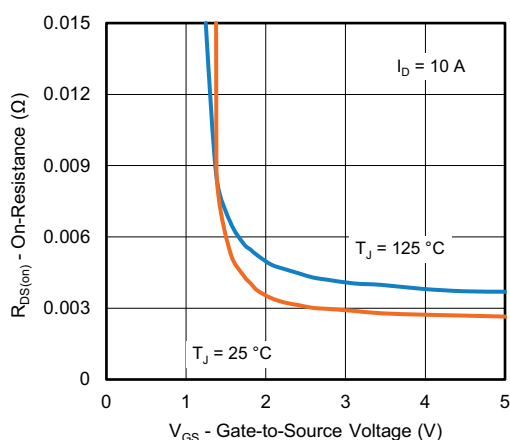
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



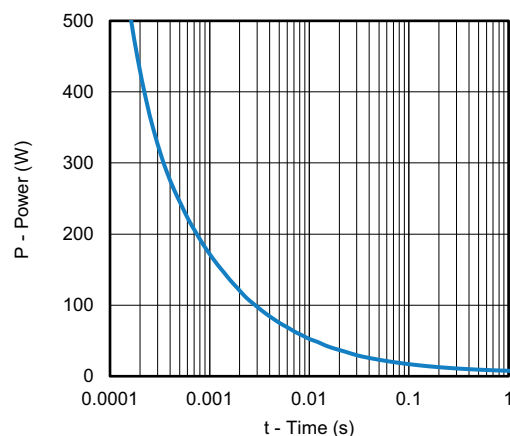
Source-Drain Diode Forward Voltage



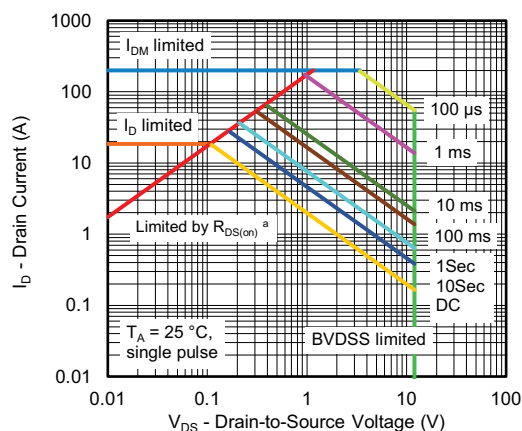
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



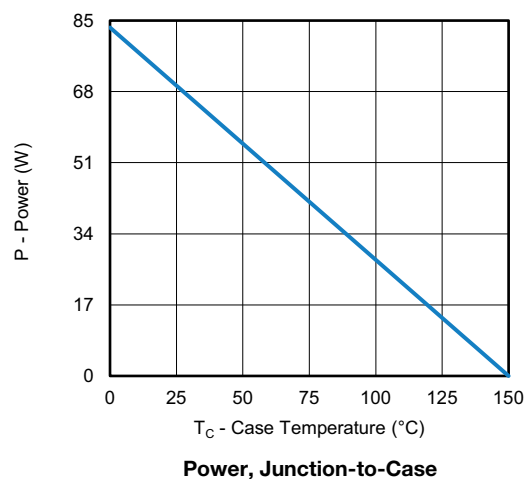
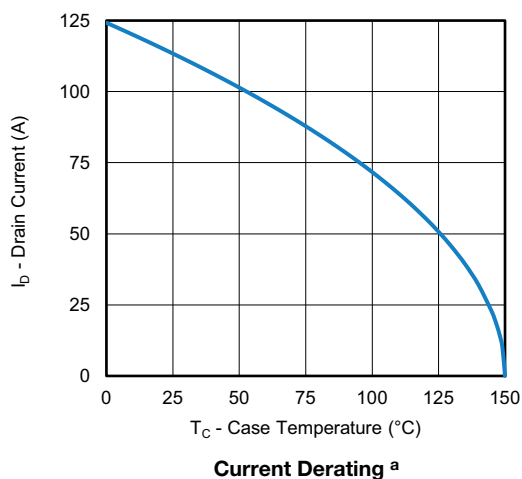
Safe Operating Area, Junction-to-Ambient

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

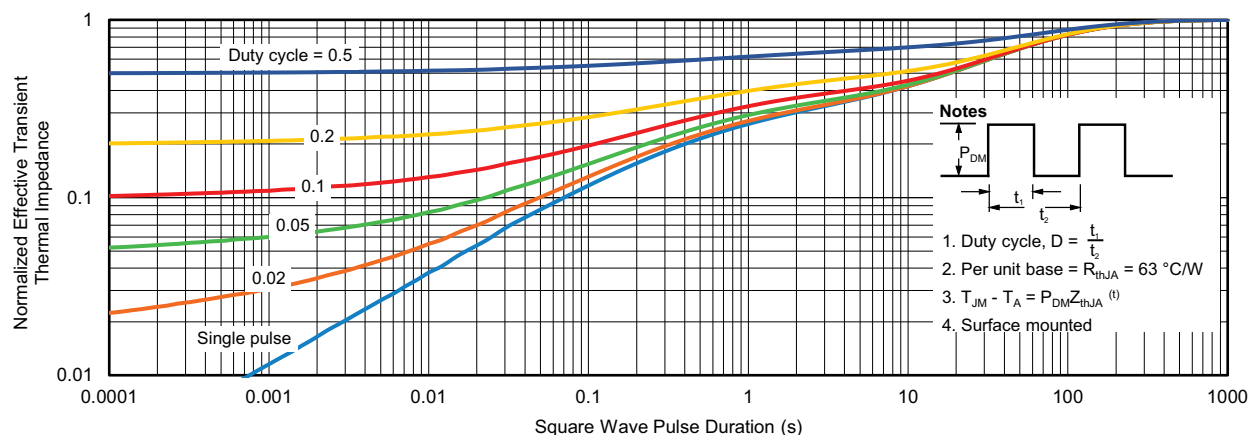


Notes

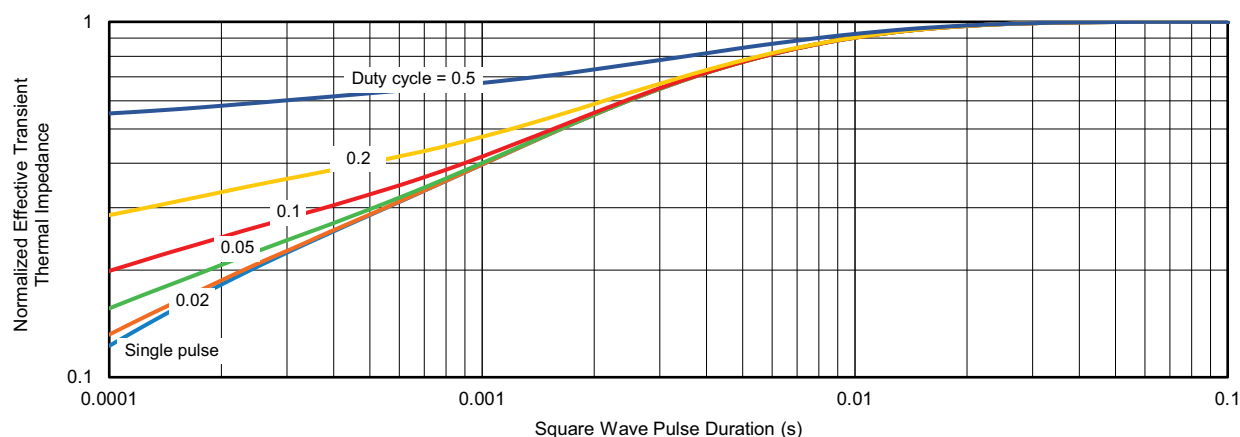
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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