




晶采光電科技股份有限公司  
**AMPIRE CO., LTD.**

# Specifications for LCD module

<b>Customer</b>	<b>Avnet USA</b>
<b>Customer part no.</b>	<b>AES-ACC-DISP-5INCH</b>
<b>Ampire part no.</b>	<b>AM-7201280KTZQW-T02H</b>
<b>Approved by</b>	
<b>Date</b>	November 18, 2024

- Preliminary Specification  
 Formal Specification

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This Specification is subject to change without notice.

## RECORD OF REVISION

Revision Date	Page	Contents	Editor
2023/03/27	-	New Release	Mantle
2023/06/21	3,33	Add Type-C cable	Mantle
	31	Bridge board add more function	
2023/07/28	3.33	Cancel Type-C Cable	Mantle
	31	Bridge board add more function	
		Bridge board reduces some functions	
2024/01/08		TFT-7201280-12-2 rename to AM-7201280KTZQW-T02H	Lawlite
2024/03/19	32	Update PCB drawing	Lawlite
2024/07/30	32	Update PCB drawing	Lawlite
2024/11/13	32	Update PCB drawing	Jessica

# 1. General Descriptions

## 1.1 Introduction

This is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) single chip and sub sheet that use amorphous silicon TFT as a switching device. This TFT LCD panel has a 4.99 inch diagonally measured active display area with HD resolution (720 horizontal by 1280 vertical pixels array).

## 1.2 Features

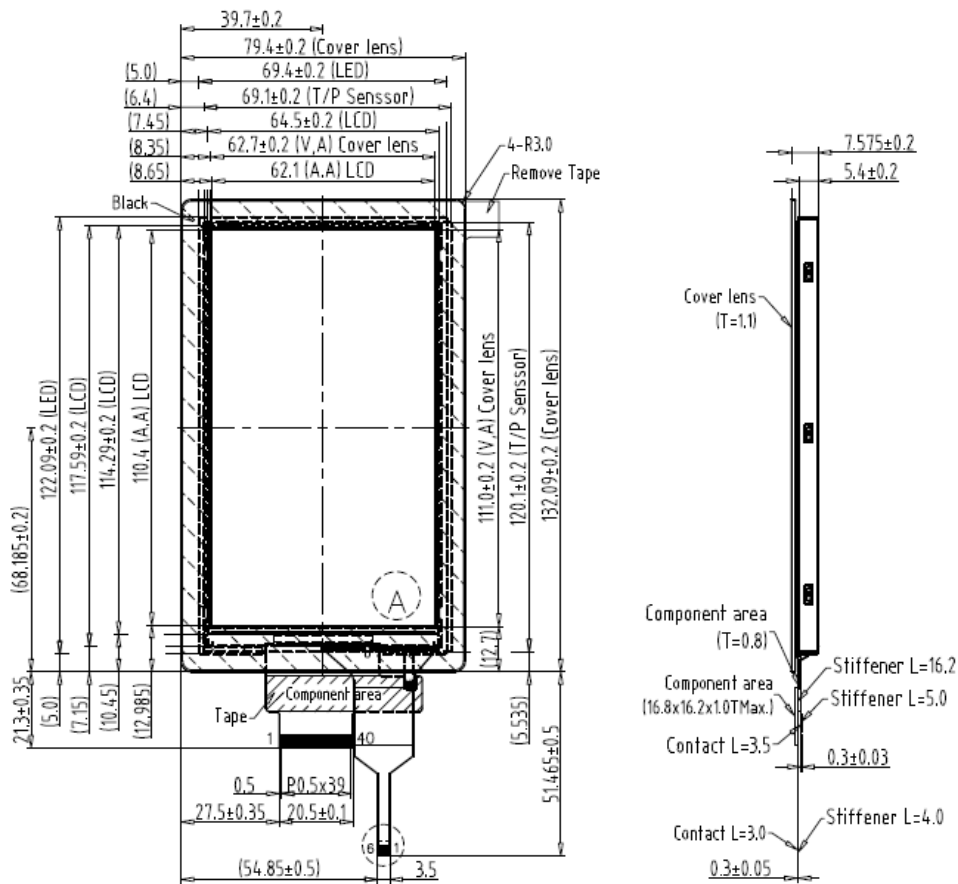
- (1) 4.99 Inch TFT-LCD Panel
- (2) MIPI Interface
- (3) Touch panel
  - ✧ IC controller: ST1633i-N48
  - ✧ Interface: I2C
- (4) Cover glass
  - ✧ Thickness:1.1mm

## 1.3 Customize

- (1) Bridge board
- (2) 30 Pin FFC

### 1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	5.0	Inch
Number of pixel	720 x 1280	-
Pixel Pitch (H x V)	0.08625 x 0.08625	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black, IPS	-
White Luminance	<b>360</b> (Typ.)	cd /m2
Electrical Interface (Logic)	MIPI	-



## 2. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Conditions
System power supply Voltage	IOVCC	-0.3	3.8	V	(1),(2)
Power supply VSP	VSP	-0.3	7.0	V	(1),(2)
Power supply VSN	VSN	-7.0	0.3	V	(1),(2)
Operating Temperature	TOP	<b>-20</b>	<b>70</b>	°C	(3),(4),(5),(6)
Storage Temperature	TST	<b>-30</b>	<b>80</b>	°C	

Note(1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note(2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. Normal conditions are defined as: Temperature: 25°C, Humidity: 55± 10%RH.

Note(3) Unpredictable results may occur when it was used in extreme conditions. Ta= Ambient Temperature, Tgs= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note(4) Wet bulb temperature should be lower than 58°C, and no condensation of water. Besides, protect the module from static electricity.

### 3. Electrical Characteristics

#### 3.1 TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply voltage	IOVCC	1.65	2.8	3.6	V	
Supply Voltage	VSP	4.5	--	6.6	V	
Supply Voltage	VSN	-4.5	--	-6.6	V	

Note(1)  $f_V = 60\text{Hz}$  ,  $T_a = 25^\circ\text{C}$  , Display pattern : All White.

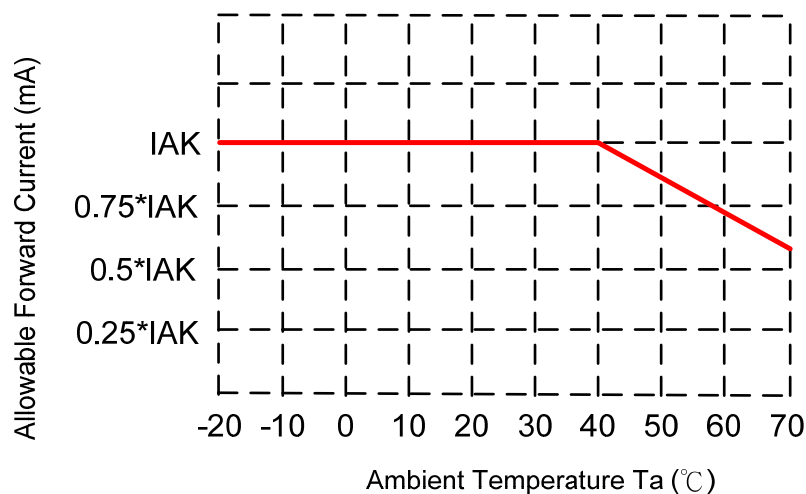
Note(2) \*:Will be reference only

#### 3.2 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED Voltage	VAK	16.8	18.0	19.2	V	
LED current	IAK	--	40	--	mA	(2)
Life time	Hrs.	50K	--	--	Hours	(1)(2)

Note(1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a = 25 \pm 3^\circ\text{C}$  , typical IAK value indicated in the above table until the brightness becomes less than 50%.

Note(2) When LCM is operated over  $40^\circ\text{C}$  ambient temperature, the **IAK** should be follow :



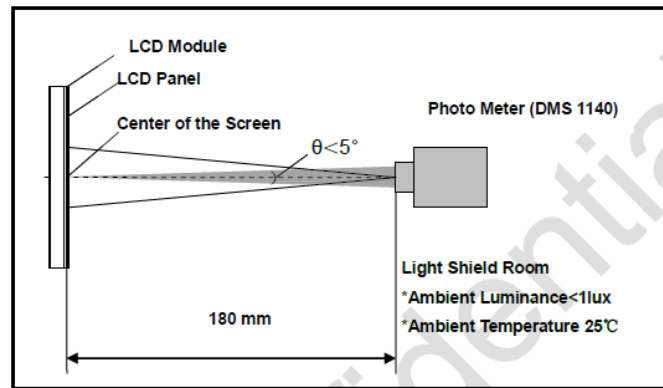
## 4. Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

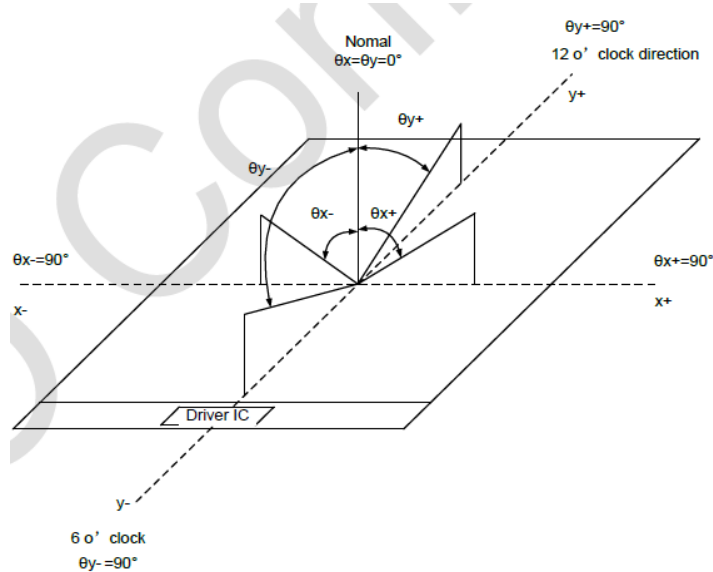
Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	$\theta_{x+}$	80	85	-	degree	(1),(2)
		$\theta_{x-}$	80	85	-		
	Vertical	$\theta_{y+}$	80	85	-		
		$\theta_{y-}$	80	85	-		
Contrast Ratio	Center		900	1200	-	-	(1),(3) $\theta_x=\theta_y=0^\circ$
Response Time	Rising + Falling		-	35	40	ms	(1),(4),(6),(7),(8) $\theta_x=\theta_y=0^\circ$
NTSC	CIE1931		65	70	-	%	Under C-light (1),(5) $\theta_x=\theta_y=0^\circ$
Color Chromaticity (CIE1931)	Red	x	Typ. -0.05	TBD	Typ. +0.05	-	
	Red	y		TBD		-	
	Green	x		TBD		-	
	Green	y		TBD		-	
	Blue	x		TBD		-	
	Blue	y		TBD		-	
	White	x		TBD		-	
	White	y		TBD		-	
White Luminance	Center		<b>288</b>	<b>360</b>	-	cd/m <sup>2</sup>	(1),(2) $\theta_x=\theta_y=0^\circ$
Luminance Uniformity	9Points		-	TBD	-	%	(1),(2),(6) $\theta_x=\theta_y=0^\circ$

Note(1) Measurement Setup:

The LCD module should be stabilized at given temperature (25°C) for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in a windless room.



Note(2) Definition of Viewing Angle



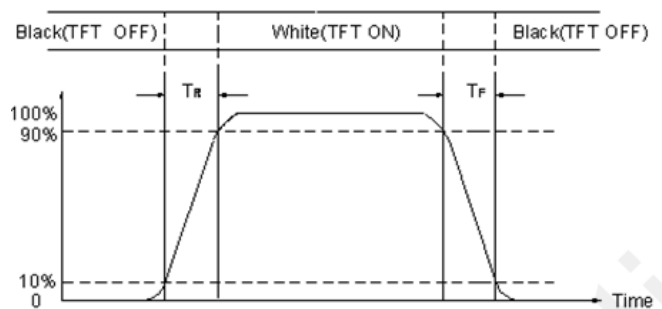
Note(3) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

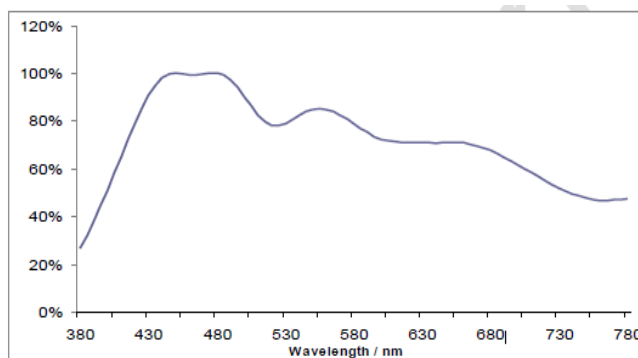
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note(4) Definition Of Response Time (TR, TF)



Note(5) Definition of Brightness Luminance

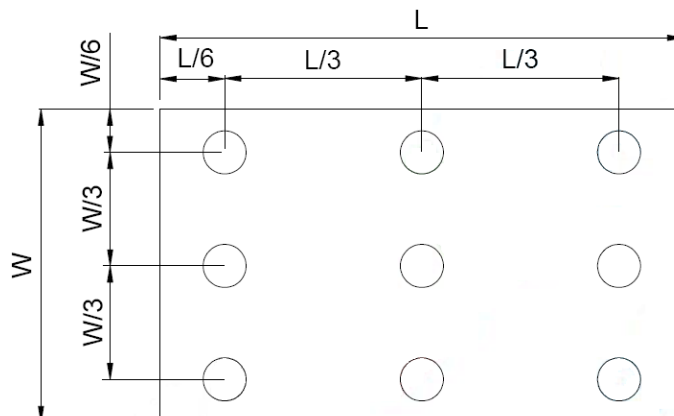


Note(6) Definition of Brightness Luminance

Active area is divided into 9 measuring areas (Refer to bellow figure).  
 Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (Yu)} = \frac{B_{\min}}{B_{\max}}$$

L ----- Active area length      W ----- Active area width



Bmax: The measured maximum luminance of all measurement position.  
 Bmin: The measured minimum luminance of all measurement position.

## 5. Interface

No.	Symbol	Functions
1	IOVCC(1.8V)	Power input 1.8V for logic power
2	IOVCC(1.8V)	Power input 1.8V for logic power
3	IOVCC(1.8V)	Power input 1.8V for logic power
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	GND	Ground
10	DATA2_P (D2_P)	MIPI SDI differential data pair
11	DATA2_N (D2_N)	MIPI SDI differential data pair
12	GND	Ground
13	DATA1_P (D1_P)	MIPI SDI differential data pair
14	DATA1_N (D1_N)	MIPI SDI differential data pair
15	GND	Ground
16	STB_P (CLK_P)	MIPI SDI differential CLK pair
17	STB_N (CLK_N)	MIPI SDI differential CLK pair
18	GND	Ground
19	DATA0_P (D0_P)	MIPI DSI differential data pair
20	DATA0_N (D0_N)	MIPI DSI differential data pair
21	GND	Ground
22	DATA3_P (D3_P)	MIPI SDI differential data pair
23	DATA3_N (D3_N)	MIPI SDI differential data pair
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	TE	Tearing effect output
29	RESET	Reset signal, low active
30	NC	No Connection
31	LEDK	Power for LED backlight cathode

32	LEDK	Power for LED backlight cathode
33	LEDA	Power for LED backlight anode
34	LEDA	Power for LED backlight anode
35	GND	Ground
36	VSN	Power Supply; connect an external power
37	VSN	Power Supply; connect an external power
38	VSP	Power Supply; connect an external power
39	VSP	Power Supply; connect an external power
40	GND	Ground

## 6. AC Characteristics

### High Speed Mode – Clock Channel Timing

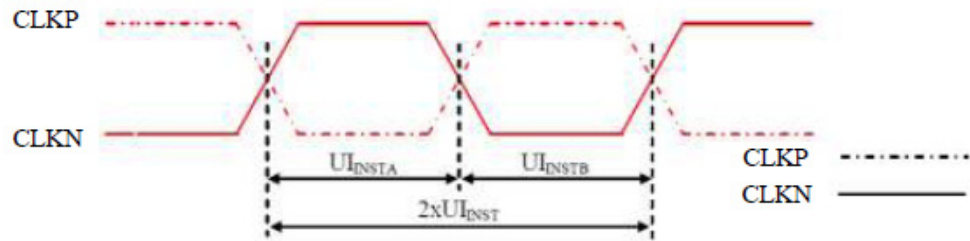


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	$UI_{INSTA}, UI_{INSTB}$ (Note 1)	UI instantaneous Half	Note 2	12.5	ns

**Notes:**

1.  $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

### High Speed Mode – Data Clock Channel Timing

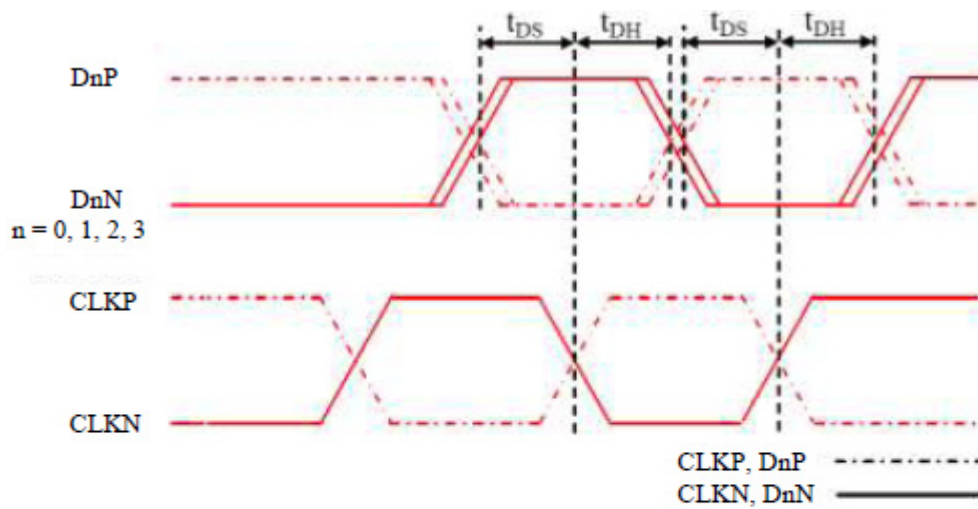


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	$t_{DS}$	Data to Clock Setup time	0.15xUI	-
	$t_{DH}$	Clock to Data Hold Time	0.15xUI	-

## High Speed Mode – Rising and Falling Timings

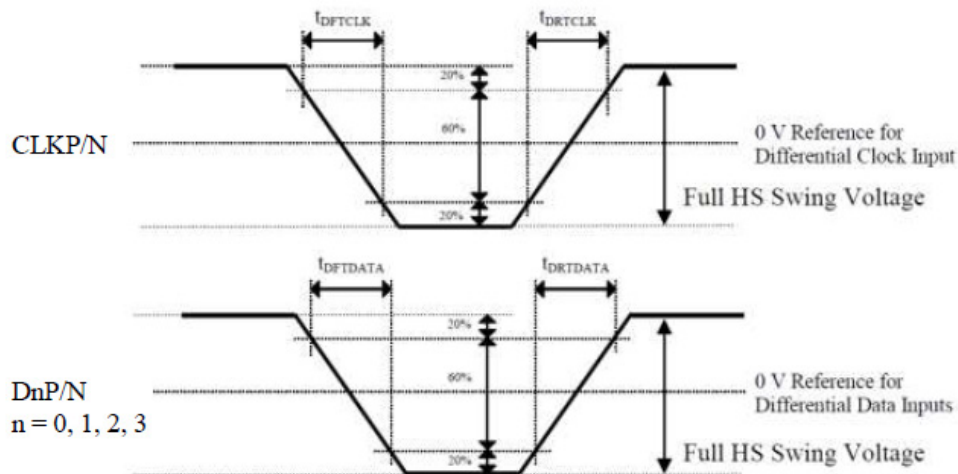


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	$t_{DRTCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	$t_{DFTCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

**Note:** The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

## Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module

(ILI9881C-04) are illustrated for reference purposes below

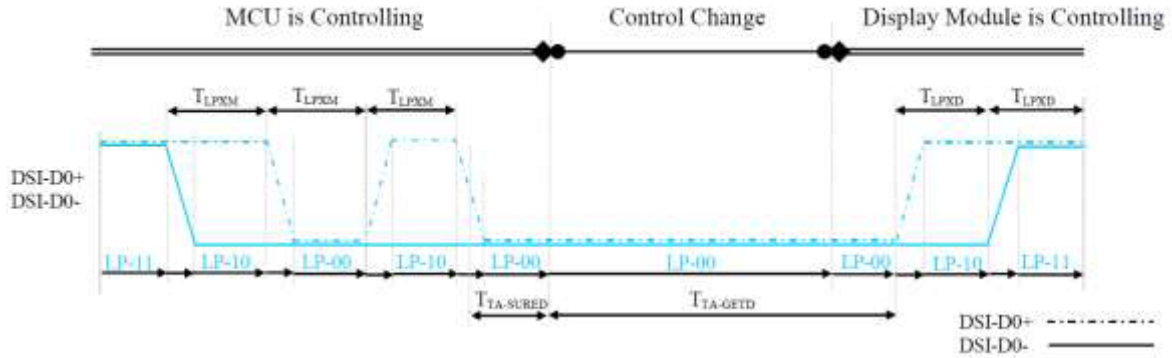


Figure 108: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-04) to the MCU are illustrated for reference purposes below.

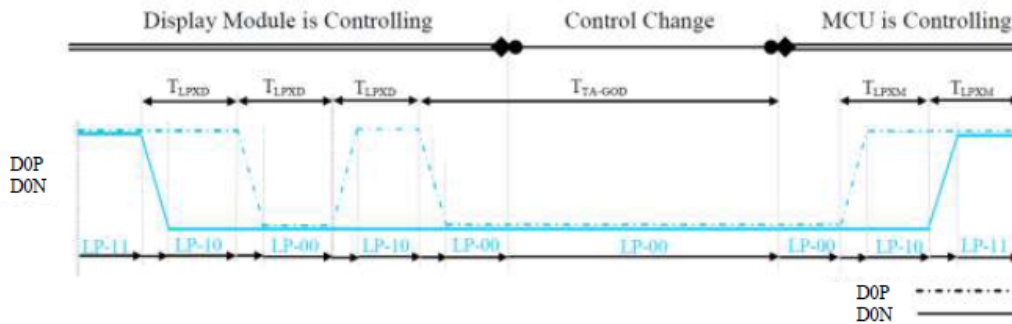


Figure 109: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	$T_{LPXM}$	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C-04)	50	75	ns
D0P/N	$T_{LPXD}$	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-04) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-04) starts driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-04)	$5 \times T_{LPXD}$	ns
D0P/N	$T_{TA-GOOD}$	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

## Data Lanes from Low Power Mode to High Speed Mode

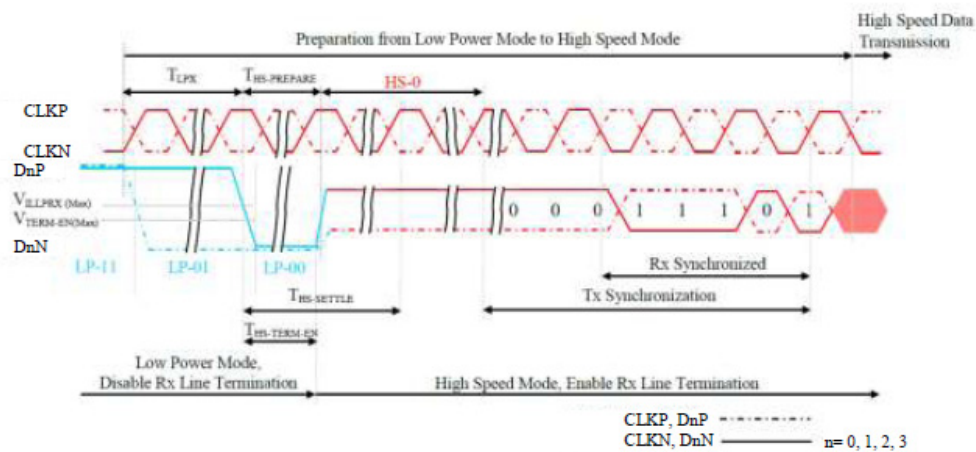


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{LPK}$	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses $V_{ILLMAX}$	-	$35+4xUI$	ns

## Data Lanes from High Speed Mode to Low Power Mode

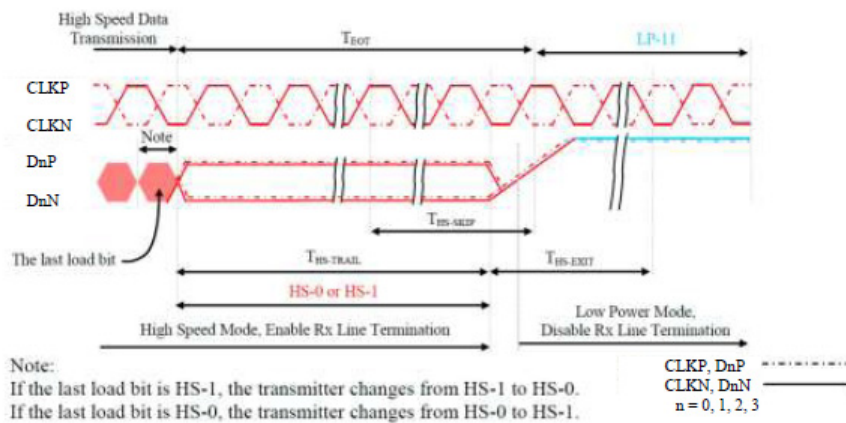


Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	$55+4 \times UI$	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

## DSI Clock Burst – High Speed Mode to/from Low Power Mode

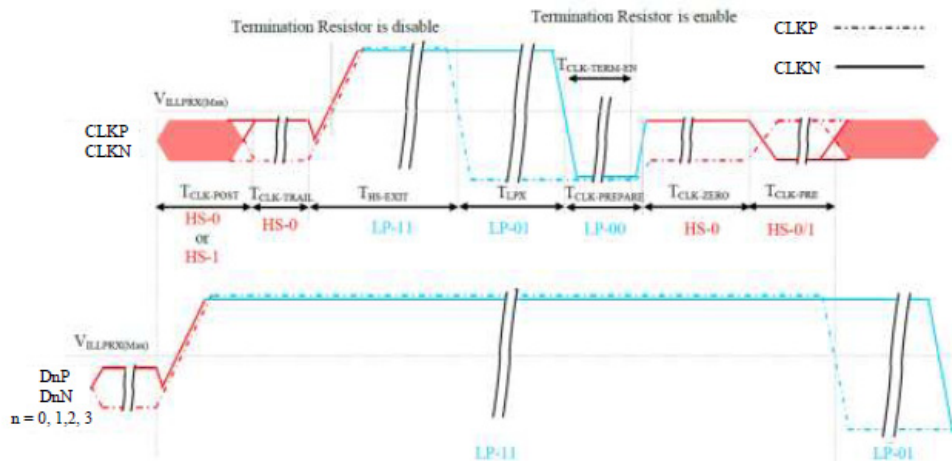
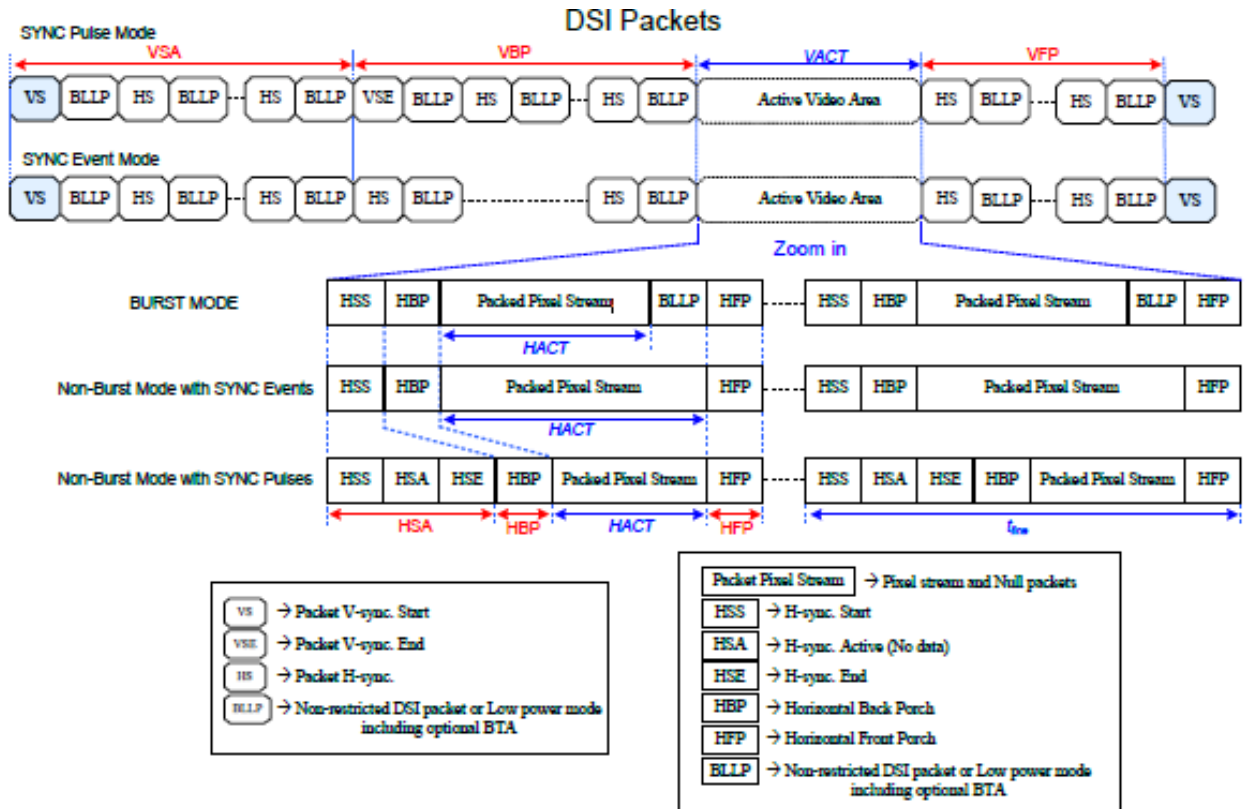


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52xUI$	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8xUI$	-	ns

## Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 <small>(Note 6)</small>	-	-	Line
Vertical Back Porch	VBP	14 <small>(Note 6)</small>	-	-	Line
Vertical Front Porch	VFP	8 <small>(Note 6)</small>	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.8	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR <sub>bps</sub>	385		Note 5	Mbps/lane

1 UI=1/Bit rate

$$HSA(\text{pixel}) = (tHSA \times \text{lane number}) / (UI \times \text{pixel format})$$

$$HBP(\text{pixel}) = (tHBP \times \text{lane number}) / (UI \times \text{pixel format})$$

$$HFP(\text{pixel}) = (tHFP \times \text{lane number}) / (UI \times \text{pixel format})$$

$$\text{Frame Rate} = \frac{BR_{\text{bps}} \times \text{Lane}_{\text{num}}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR<sub>bps</sub> = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, Lane<sub>num</sub>=4(lane), Pixel Format=24(bit).

Note:

1. Lanenum: Data lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1 DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

## 7. Touch Panel Specification

### 7.1 Basic Characteristic

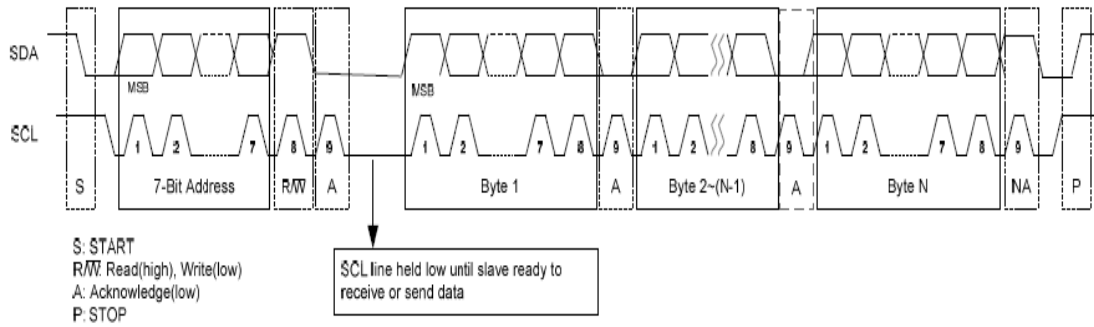
Item	Specification
Type	Projective Capacitive Touch Panel
Activation	5-fingers or Single-finger
X/Y Position Reporting	Absolute Position
Touch Force	No contact pressure required
Calibration	No need for calibration
Report Rate	Approx. 60 points/sec
Control IC	<a href="#">ST1633i-N48</a>

### 7.2 Capacitive Touch Panel FPC Descriptions

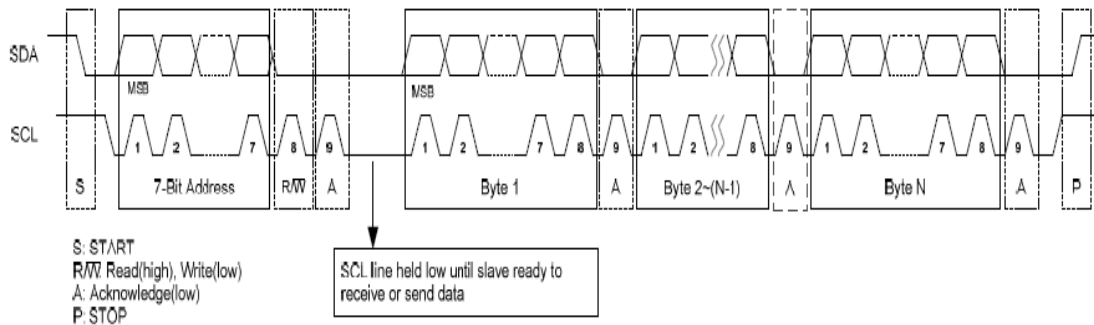
No.	Symbol	Description
1	GND	Ground.
2	SDA	I2C Interface.
3	SCL	
4	VDD	Power Supply for TP controller.
5	INT	IRQ Terminal.
6	XRES	Terminal of Reset TP controller.

### 7.3 I2C Slave Interface

#### Read



#### Write



### 7.4 Default I2C Address

I2C address is default to **0x55** (7-bits address) for Sitronix Touch IC. If the I2C address is conflict with another I2C device’s address on same bus, user can change I2C address by TTK PC Utility.

### 7.5 Register Read

For reading register value from I2C device, host has to tell I2C device the *Start Register Address* before reading corresponding register value.

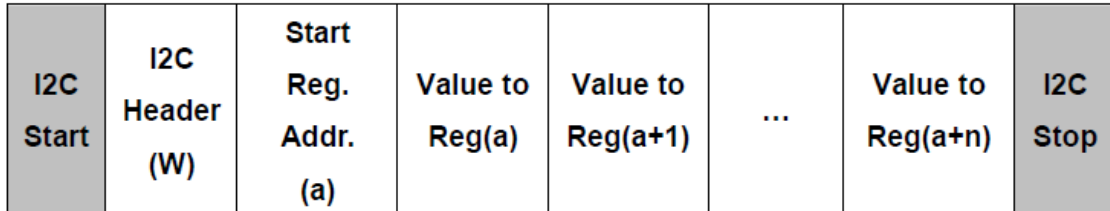
I2C Start	I2C Header (W)	Start Reg. Addr. (a)	I2C Stop	I2C Start	I2C Header (R)	Value of Reg(a)	Value of Reg(a+1)	...	Value of Reg(a+n)	I2C Stop
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Sitronix Touch IC I2C host interface protocol supports Repeated Register Read. That is, once the Start Register Address has been set by host, consequent I2C Read(R) transactions will directly read register values starting from the Start Register Address without setting address first, as shown in Figure

I2C Start	I2C Header (R)	Value of Reg(a)	Value of Reg(a+1)	...	Value of Reg(a+n)	I2C Stop	I2C Start	I2C Header (R)	Value of Reg(a)	Value of Reg(a+1)	...	Value of Reg(a+n)	I2C Stop
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## 7.6 Register Write

For writing register to I2C device, host has to tell I2C device the Start Register Address in each I2C Register Write transaction. Register values to the I2C device will be written to the address starting from the Start Register Address described in Register Write I2C transaction as shown in Figure



## 7.7 Sample Codes

```
typedef struct {  
    u8 y_h: 3,  
    reserved: 1,  
    x_h: 3,  
    valid: 1;  
    u8 x_l;  
    u8 y_l;  
    u8 z;  
} xyz_data_t;
```

```
typedef struct {  
    u8 fingers: 4,  
    reserved: 4;  
    u8 keys;  
    xyz_data_t xyz_data[10];  
} stx_report_data_t;
```

// I2C Master sends *count* bytes data stored in *buf* to I2C Slave.

// I2C package: | S | I2C Addr | W | Data (buf) | P |

**extern int i2c\_master\_send(const char \*buf, int count);**

// I2C Master reads *count* bytes data to *buf* from I2C Slave.

// I2C package: | S | I2C Addr | R | Data (buf) | Nak | P |

**extern int i2c\_master\_recv(char \*buf, int count);**

#### 4-4-8 Read XY Coordinates

The function, `get_coordinates()`, reads XY Coordinate registers from I2C Slave, extracts XY information from data buffer and returns to upper layer. This function shall be called from ISR each time when host receives and INT from device.

```
static int get_coordinates(u8 *count, u32 *x0, u32 *y0, u32 *x1, u32 *y1)
{
    u8 buf[42];
    stx_report_data_t *pdata;
    int ret = 0;
    *count = 0; // Set point detected count to 0.
    if (i2c_master_recv(buf, sizeof(buf))) // Read Coordinates from default Reg. address 0x10.
        goto err;
    pdata = (stx_report_data_t *) buf;
    if (pdata->fingers) {
        if (pdata->xy_data[0].valid) {
            *x0 = pdata->xy_data[0].x_h << 8 | pdata->xy_data[0].x_l;
            *y0 = pdata->xy_data[0].y_h << 8 | pdata->xy_data[0].y_l;
            (*count)++;
        }
        if (pdata->xy_data[1].valid) {
            *x1 = pdata->xy_data[1].x_h << 8 | pdata->xy_data[1].x_l;
            *y1 = pdata->xy_data[1].y_h << 8 | pdata->xy_data[1].y_l;
            (*count)++;
        }
    }
err:
    return ret;
}
```

## 8. Reliability Conditions

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , Dry t=240 hrs	
Low Temperature Operation	-20±3°C , Dry t=240 hrs	
High Temperature Storage	80±3°C , Dry t=240 hrs	1,2
Low Temperature Storage	-30±3°C , Dry t=240 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note(1) Condensation of water is not permitted on the module.

Note(2) The module should be inspected after 1 hour storage in normal conditions (15-35°C, 45-65%RH).

Note(3) The module shouldn't be tested more than one condition, and all the test conditions are independent.

Note(4) All the reliability tests should be done without protective film on the module.

Definitions of life end point:

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

## **9. Use Precautions**

### **9.1 Handling precautions**

- (1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- (2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- (3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- (4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

### **9.2 Installing precautions**

- (1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx.  $1M\Omega$  and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- (2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- (3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- (4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

### 9.3 Storage precautions

- (1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- (2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- (3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

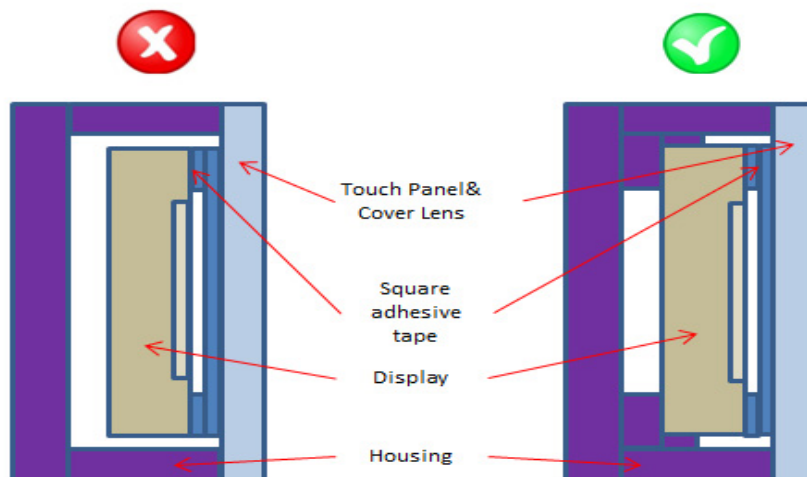
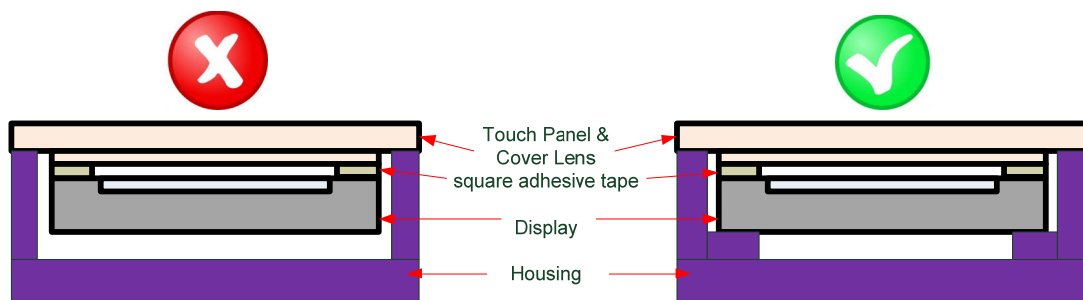
### 9.4 Operating precautions

- (1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- (2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- (3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- (4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- (5) Make certain that each signal noise level is within the standard (L level: 0.2 IOVCC or less and H level: 0.8 IOVCC or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- (6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- (7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

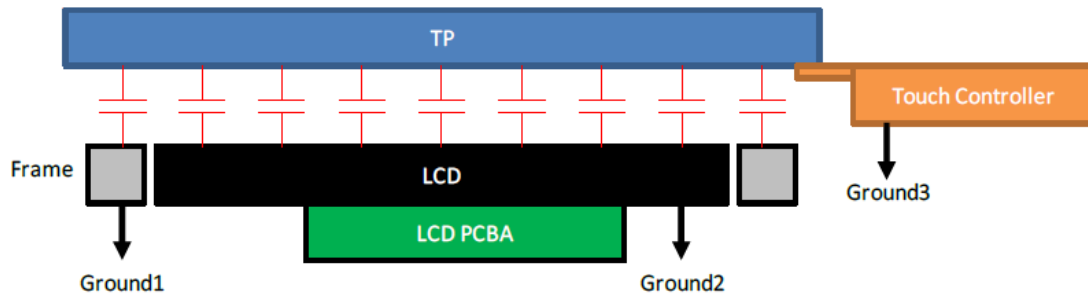
(8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

## 9.5 Mechanism

- (1) Please mount LCD module by using mounting holes arranged in four corners tightly.
- (2) Please hold the LCD module properly when you use or store it.
- (3) The square adhesive tape which is between the touch panel and display can't provide well supporting in the long term and high ambient temperature condition. Whether upright or horizontal position the support holder which is in the back side of the display is needed. Do not let the display floating.



- (4) TP needs to work in environment with stable stray capacitance. In order to minimize the variation in stray capacitance, all conductive mechanical parts must not be floating. Intermittent floating any conductive part around the touch sensor may cause significant stray capacitance change and abnormal touch function. It is recommended to keep all conductive parts having same electrical potential as the GND of the touch controller module.

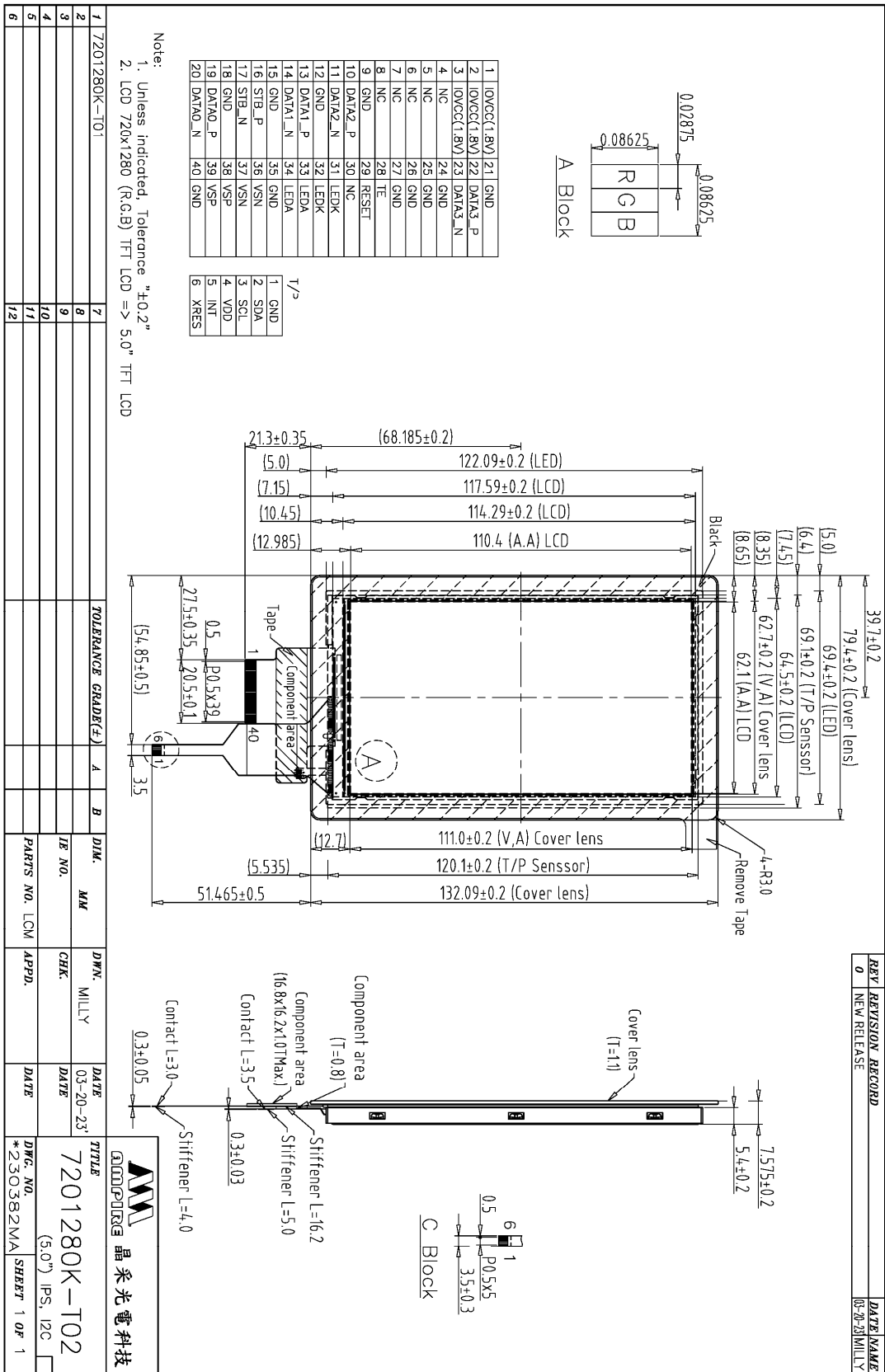


GND1, GND2 and GND3 should be connected together to have the same ground

## 9.6 Other

- (1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- (2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver
- (3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

# 10. Outline Dimension







## 11.2 Interface

- (1). CN1: Connect to LCM FPC(MIPI interface)
- (2). CN2: Connect to LCM TP FPC(I2C)
- (3). CN3: CSF-2481-301R/P0.5 30PIN or equivalent.

Pin	Signal name	Description
1	GND	Ground
2	DSI_DP3	MIPI DSI transmit differential signal 3 pair positive
3	DSI_DN3	MIPI DSI transmit differential signal 3 pair negative
4	GND	Ground
5	DSI_DP2	MIPI DSI transmit differential signal 2 pair positive
6	DSI_DN2	MIPI DSI transmit differential signal 2 pair negative
7	GND	Ground
8	DSI_DP1	MIPI DSI transmit differential signal 1 pair positive
9	DSI_DN1	MIPI DSI transmit differential signal 1 pair negative
10	GND	Ground
11	DSI_DP0	MIPI DSI transmit differential signal 0 pair positive
12	DSI_DN0	MIPI DSI transmit differential signal 0 pair negative
13	GND	Ground
14	DSI_CKP	MIPI DSI clock differential signal pair positive
15	DSI_CKN	MIPI DSI clock differential signal pair negative
16	GND	Ground
17	DSI_TS_RST	Touch screen reset output
18	DSI_TS_nINT	Touch screen interrupt input
19	I2C4_SDA	I2C port 4 data
20	I2C4_SCL	I2C port 4 clock
21	DSI_EN	MIPI DSI backlight enable output
22	DSI_BL_PWM	MIPI DSI backlight PWM output
23	GND	Ground
24	NC	No connection
25	NC	No connection
26	GND	Ground
27	NC	No connection
28	VSYS	5V power output
29	VSYS	5V power output
30	VSYS	5V power output

## **12. FFC**

**P0.5xL 150mm 30pin**

Connect bridge board CN3 and customer board mipi connector.