



BUK9Q34-80L

80 V, 34 mOhm logic level N-channel MOSFET in MLPak33

5 June 2025

Product data sheet

1. General description

Logic level N-channel MOSFET in a small MLPak33-WF package using Trench12 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Logic-level compatible
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175°C
- Side-wettable flanks for robust solder joints and automatic optical inspection

3. Applications

- LED lighting
- DC-to-DC conversion
- Solenoid, motor and other load switching
- Circuit protection

4. Quick reference data

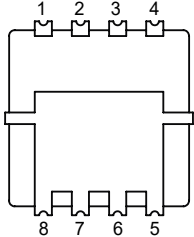
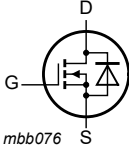
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	[1]	-	21	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	32	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5.5\text{ A}; T_j = 25\text{ °C};$ Fig. 11	-	26	34	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 5.5\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ °C};$ Fig. 13 ; Fig. 14	-	1.5	-	nC

[1] 21 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>MLPAK33 (SOT8002-3)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Q34-80L	MLPAK33	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Q34-80L	7AH

8. Limiting values

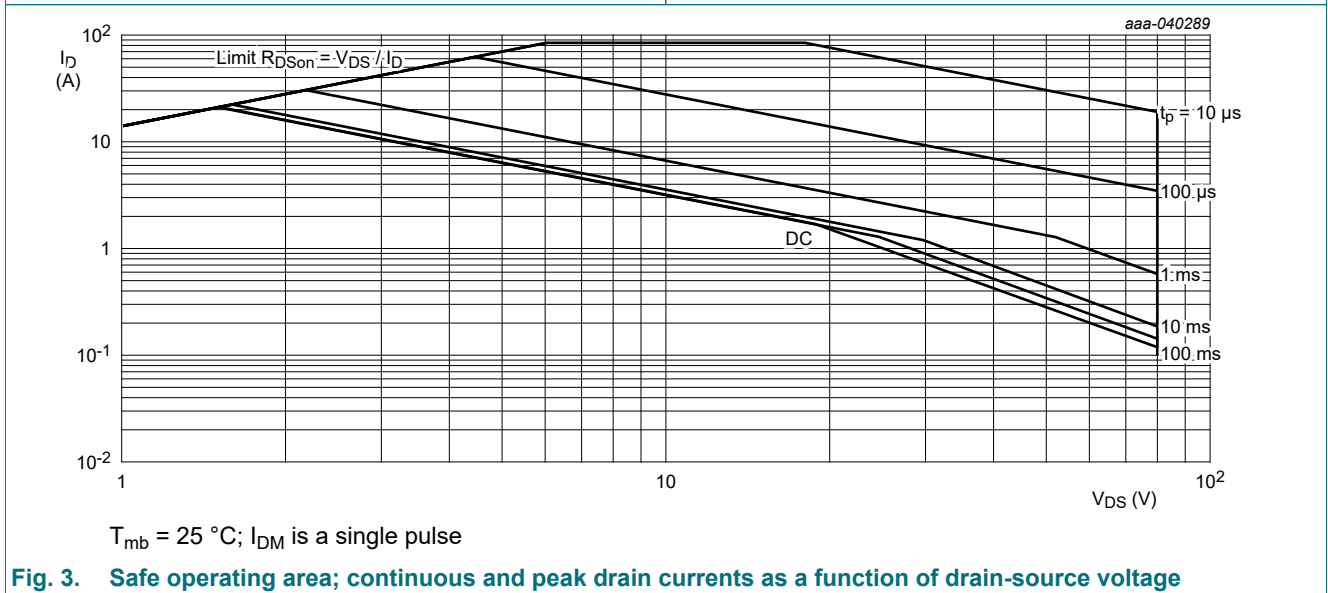
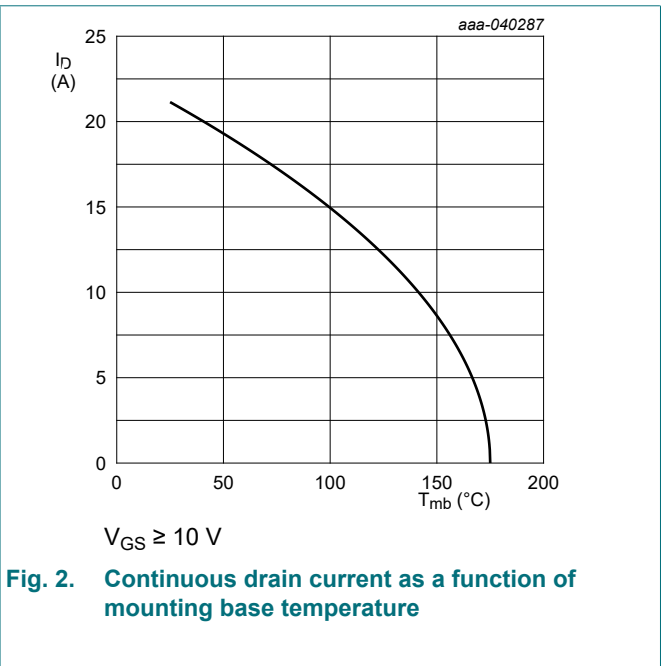
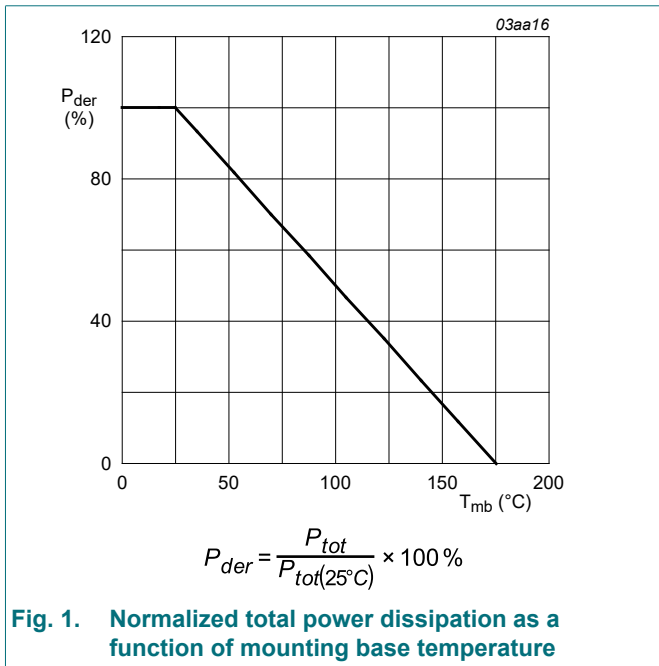
Table 5. Limiting values

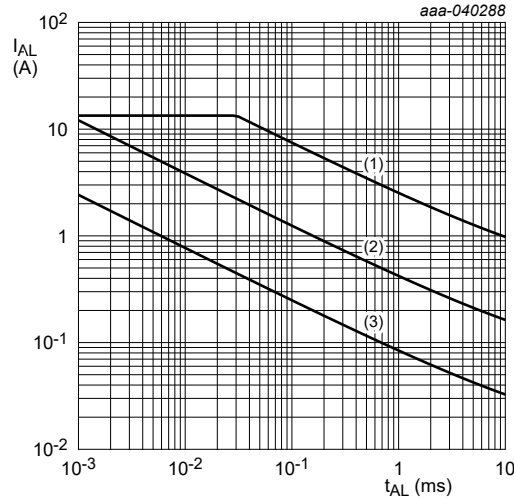
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V	
V_{GS}	gate-source voltage		-20	20	V	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	32	W	
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	21	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	15	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	85	A	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	-	21	A	
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	85	A	

Symbol	Parameter	Conditions	Min	Max	Unit	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 13.4 \text{ A}$; $V_{sup} \leq 80 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_p = 30 \mu\text{s}$; Fig. 4	[2] [3]	-	21.1	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 80 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \Omega$; Fig. 4	[2] [3]	-	13.4	A

- [1] 21 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.





(1) $T_{j\text{ (init)}} = 25\text{ °C}$; (2) $T_{j\text{ (init)}} = 150\text{ °C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3.1	4.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	40	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

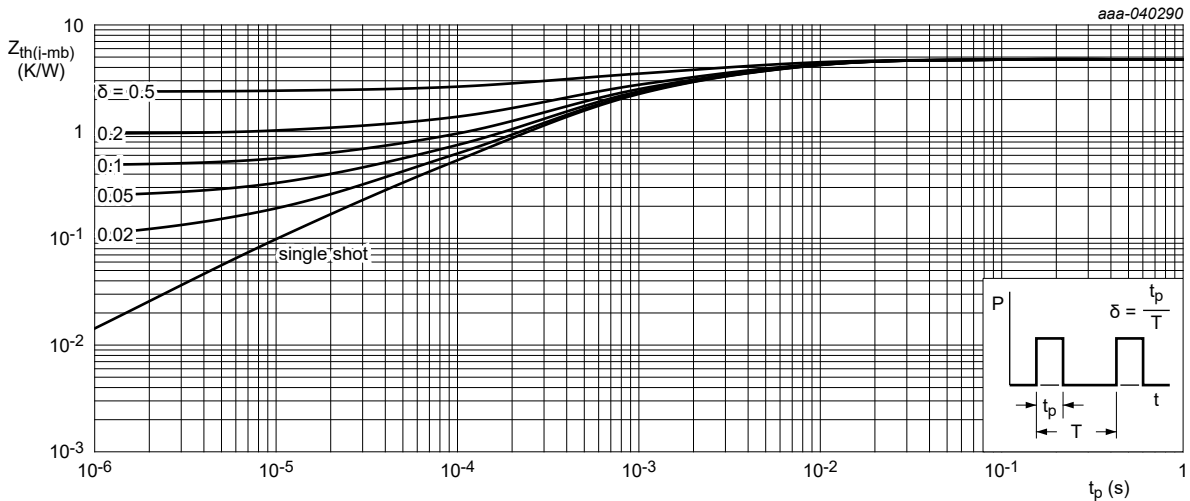


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	89	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	77	86	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	76	85	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 9 ; Fig. 10	1.45	1.7	2.15	V
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	20	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	200	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5.5 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11	-	26	34	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5.5 \text{ A}; T_j = 105 \text{ }^\circ C$; Fig. 12	-	40	52	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5.5 \text{ A}; T_j = 125 \text{ }^\circ C$; Fig. 12	-	44	58	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5.5 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 12	-	55	71	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 4.5 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11	-	35	45	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 4.5 \text{ A}; T_j = 105 \text{ }^\circ C$; Fig. 12	-	54	76	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 4.5 \text{ A}; T_j = 125 \text{ }^\circ C$; Fig. 12	-	56	79	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 4.5 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 12	-	70	95	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	1.6	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5.5 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13 ; Fig. 14	-	15	23	nC
		$I_D = 5.5 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13 ; Fig. 14	-	7.5	-	nC
Q_{GS}	gate-source charge	$I_D = 5.5 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13 ; Fig. 14	-	2.9	-	nC
Q_{GD}	gate-drain charge	$I_D = 5.5 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13 ; Fig. 14	-	1.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 15	-	1074	-	pF
C_{oss}	output capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 15	-	174	-	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 15	-	6	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 8 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	4	-	ns
t_r	rise time	$V_{DS} = 40 \text{ V}; R_L = 8 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	3	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 40 \text{ V}; R_L = 8 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	15	-	ns
t_f	fall time	$V_{DS} = 40 \text{ V}; R_L = 8 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	3	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.7\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.78	1	V
t_{rr}	reverse recovery time	$I_S = 2.5\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	21	-	ns
Q_r	recovered charge		-	13	-	nC

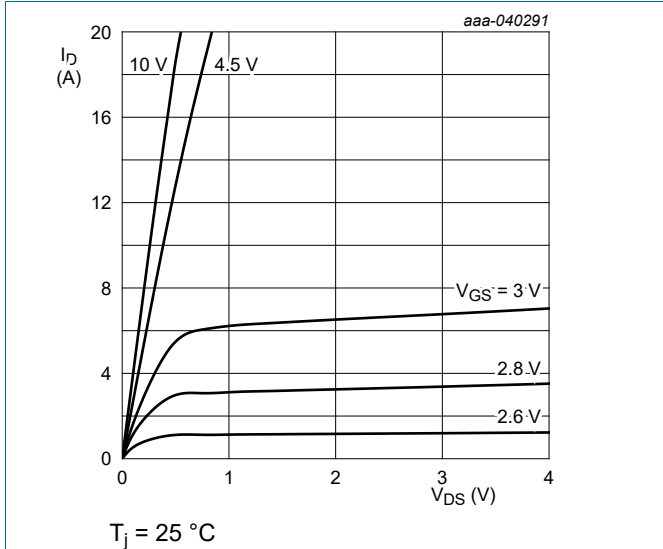


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

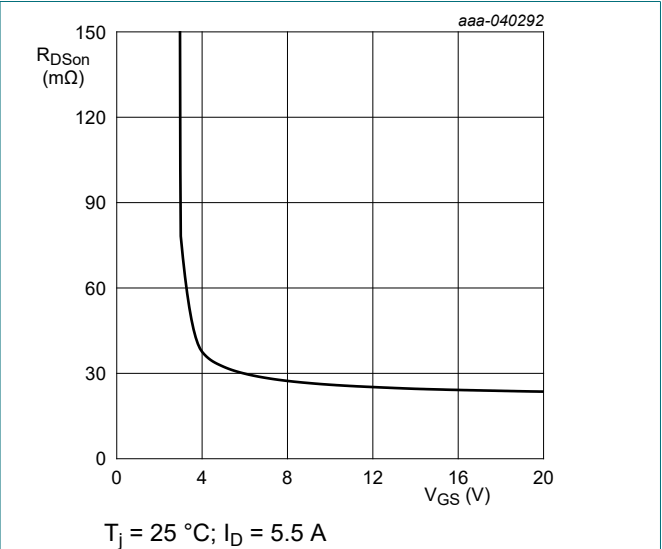


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

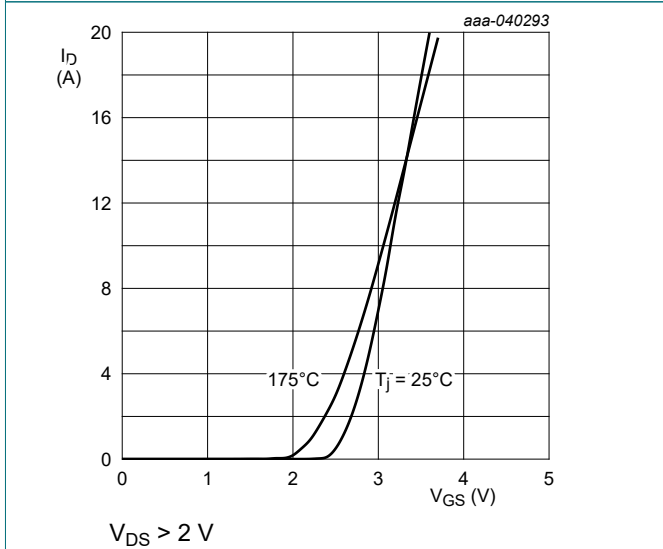


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

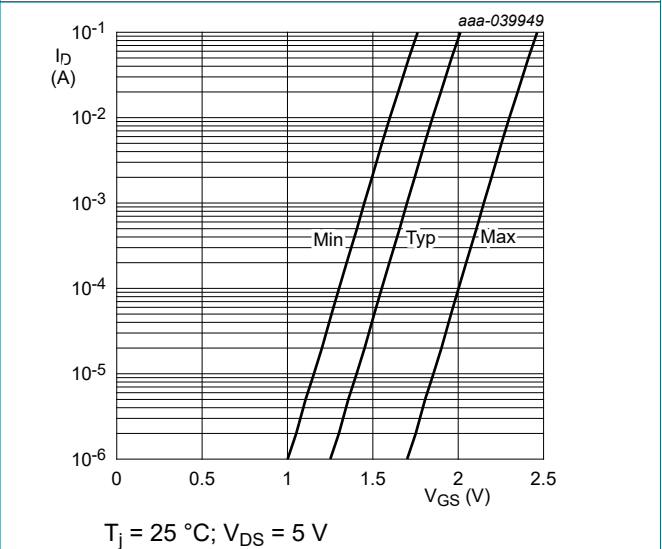
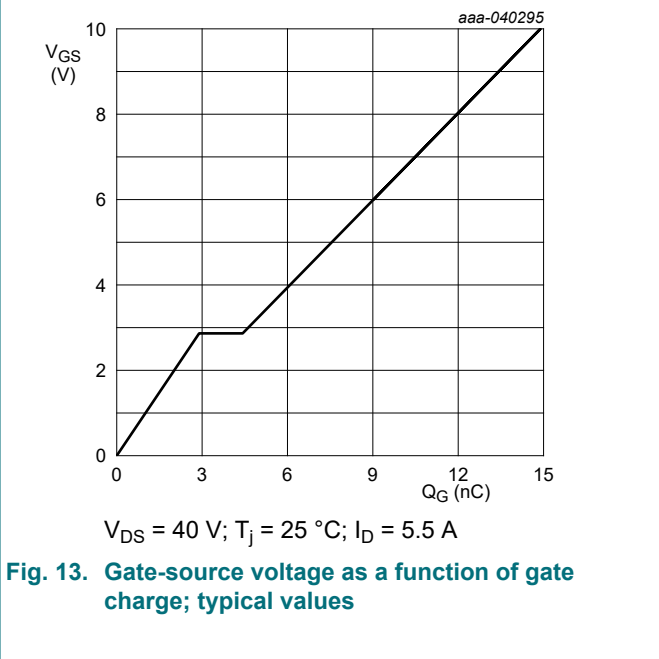
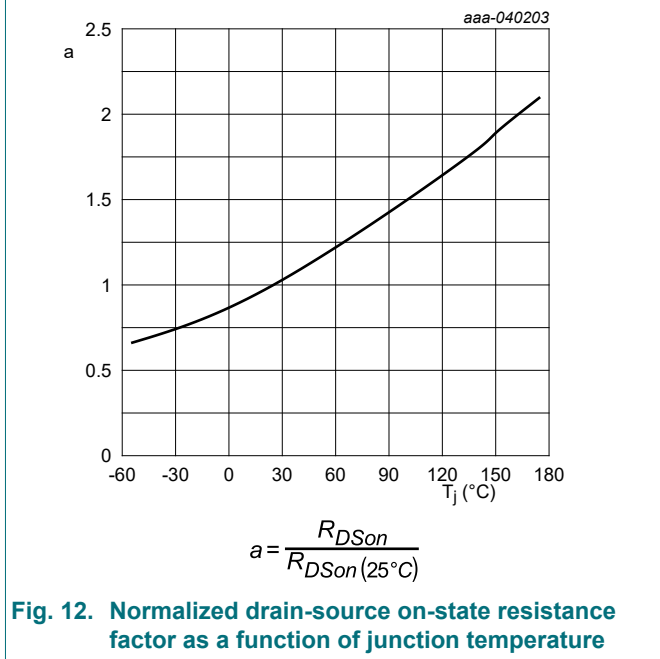
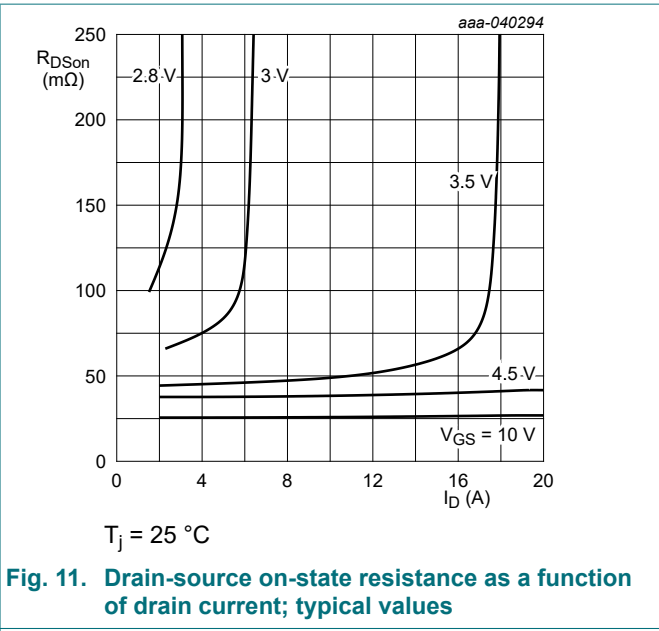
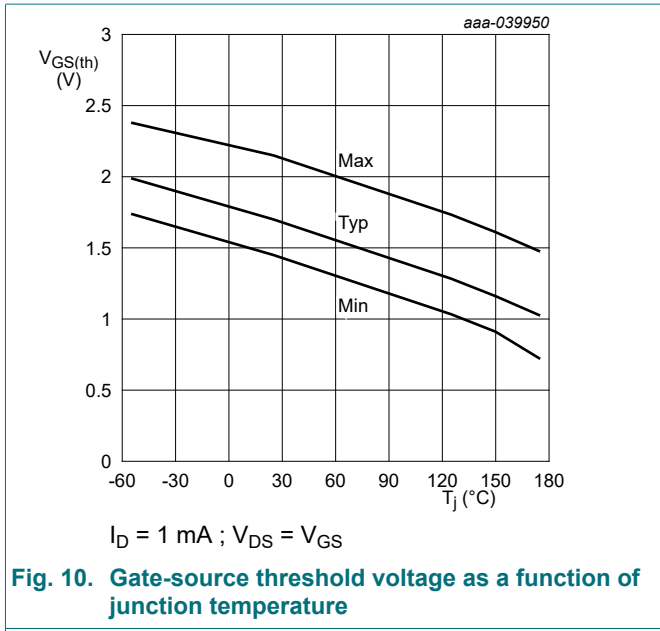


Fig. 9. Sub-threshold drain current as a function of gate-source voltage



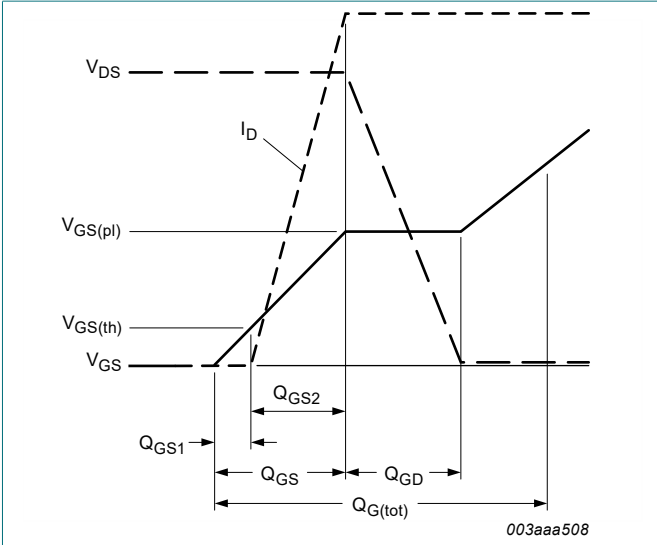


Fig. 14. Gate charge waveform definitions

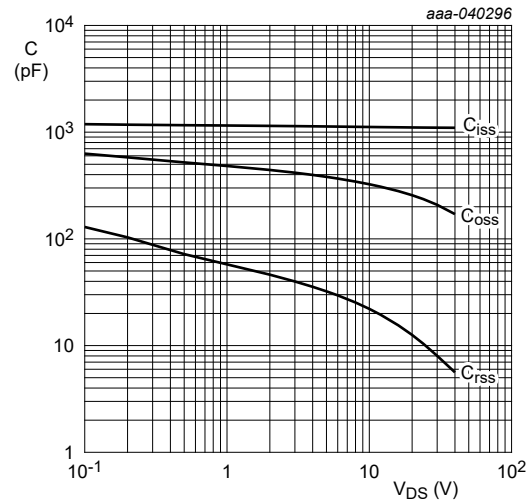
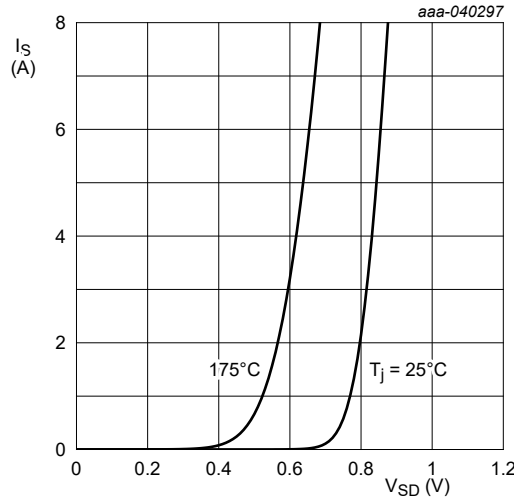


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values
 $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

MLPAK33: plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-3

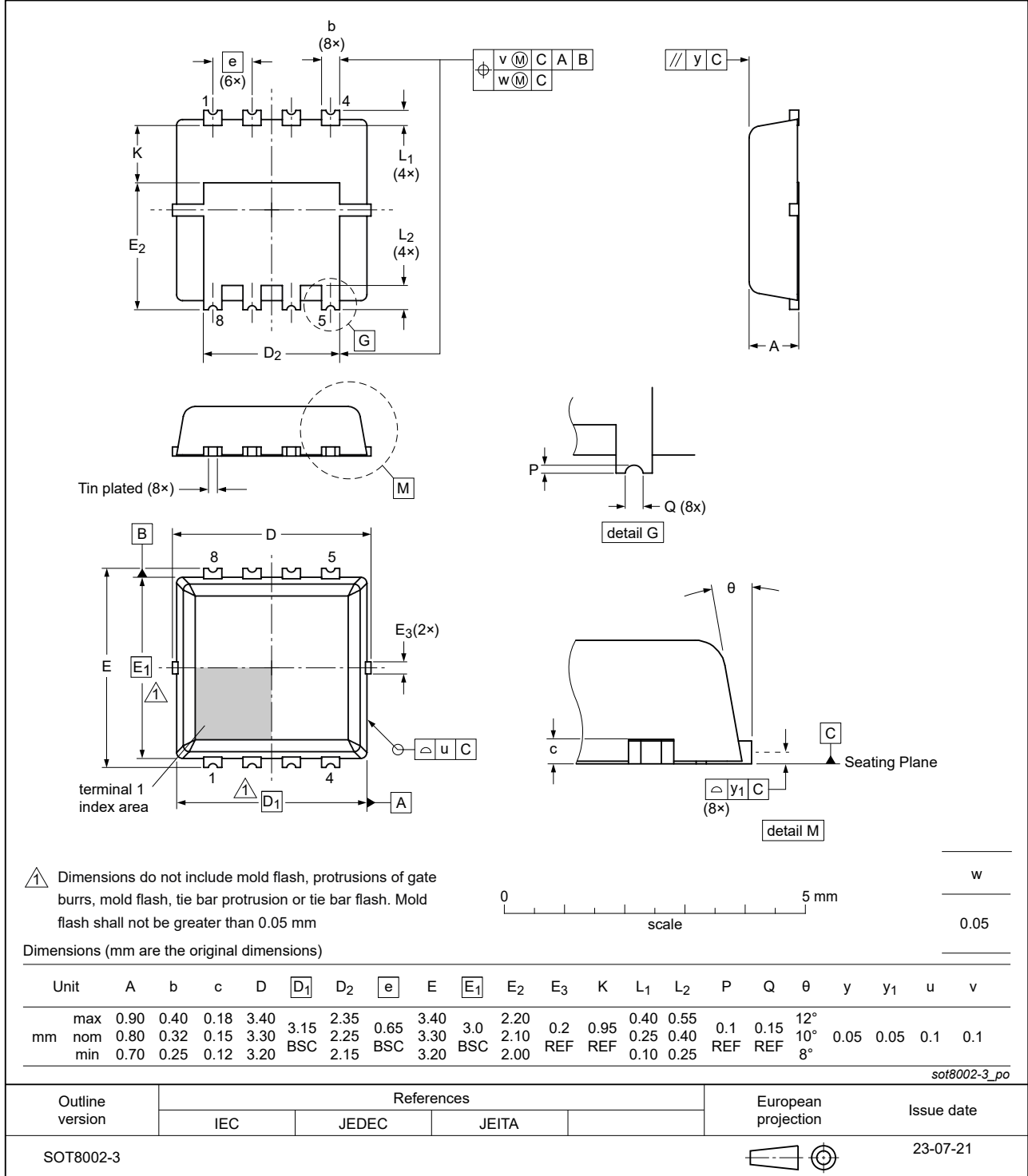


Fig. 17. Package outline MLPAK33 (SOT8002-3)

12. Soldering

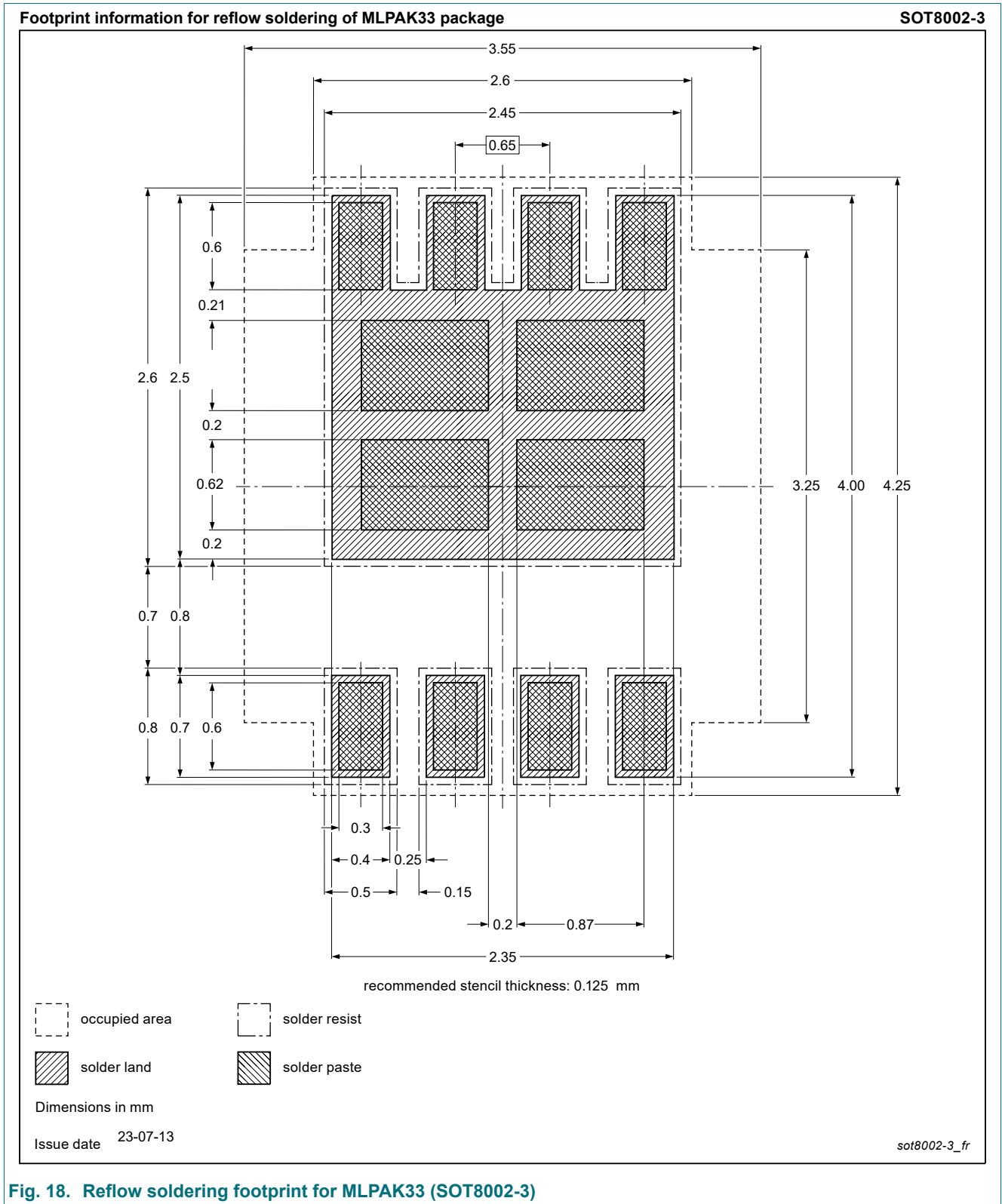


Fig. 18. Reflow soldering footprint for MLPAK33 (SOT8002-3)

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Document status [1][2]	Product status [3]	Definition
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