



BUK9Q28-80L

80 V, 28 mOhm logic level N-channel MOSFET in MLPAK33

5 June 2025

Product data sheet

1. General description

Logic level N-channel MOSFET in a small MLPAK33-WF package using Trench12 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Logic-level compatible
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175°C
- Side-wettable flanks for robust solder joints and automatic optical inspection

3. Applications

- LED lighting
- DC-to-DC conversion
- Solenoid, motor and other load switching
- Circuit protection

4. Quick reference data

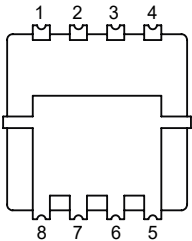
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	25	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	35.7	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 6\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	22	28	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 6\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	1.5	-	nC

[1] 25 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-3)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Marking

Table 3. Marking codes

Type number	Marking code
BUK9Q28-80L	7AG

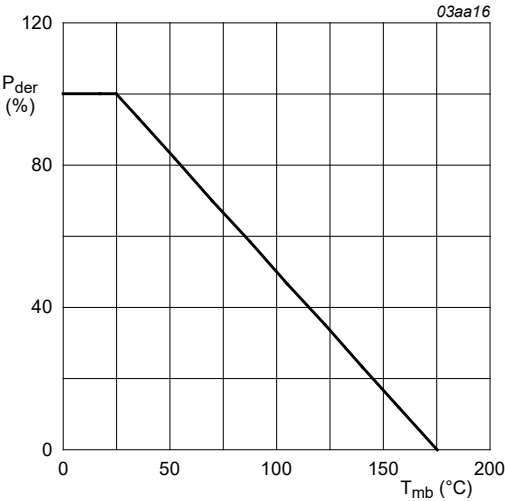
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

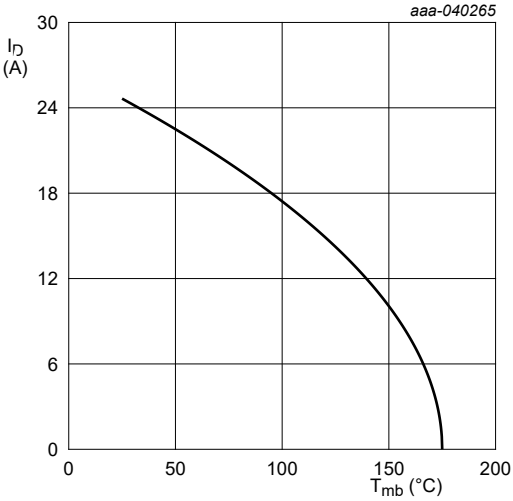
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1		-	35.7	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2	[1]	-	25	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; Fig. 2		-	17	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 3		-	99	A
T_{stg}	storage temperature			-55	175	$^{\circ}\text{C}$
T_j	junction temperature			-55	175	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$		-	25	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$		-	99	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 15.3\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; unclamped; $t_p = 35\text{ }\mu\text{s}$; Fig. 4	[2] [3]	-	27.6	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[2] [3]	-	15.3	A

- [1] 25 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}$.
- [3] Refer to application note AN10273 for further information.



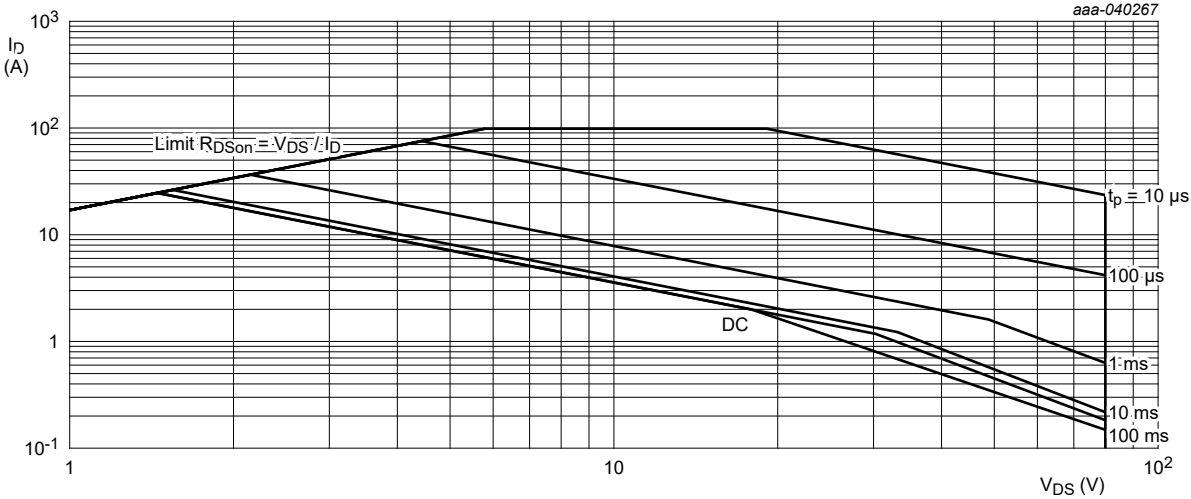
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



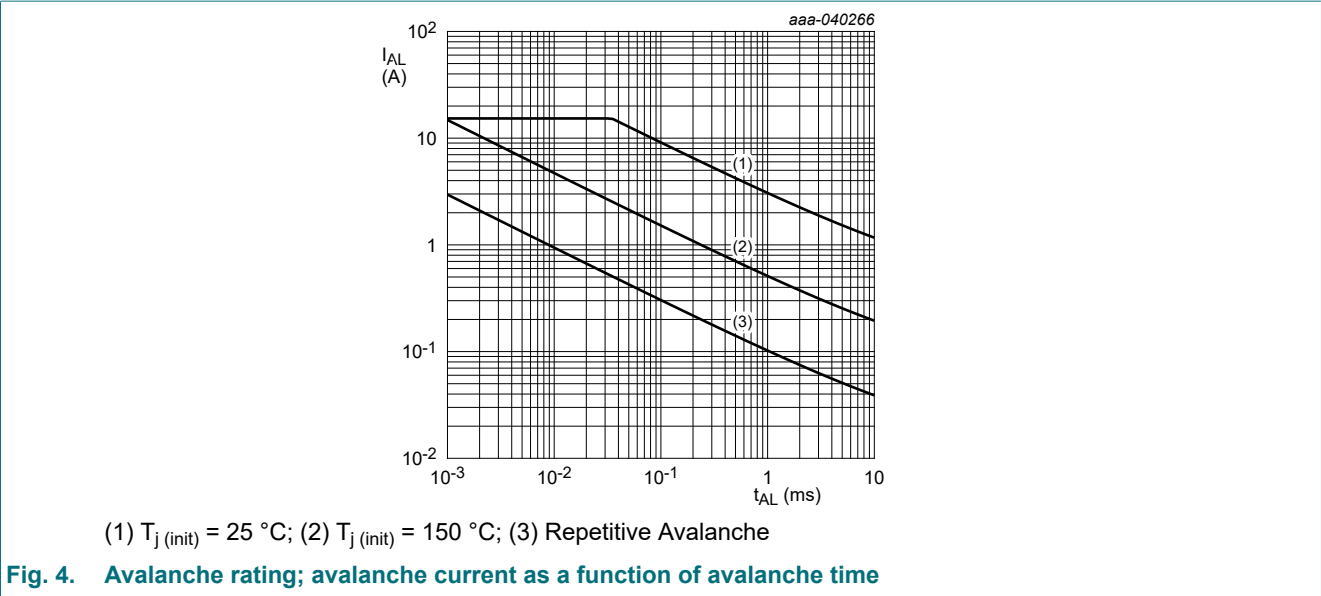
$$V_{GS} \geq 10\text{ V}$$

Fig. 2. Continuous drain current as a function of mounting base temperature



$$T_{mb} = 25\text{ }^{\circ}\text{C}; I_{DM} \text{ is a single pulse}$$

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

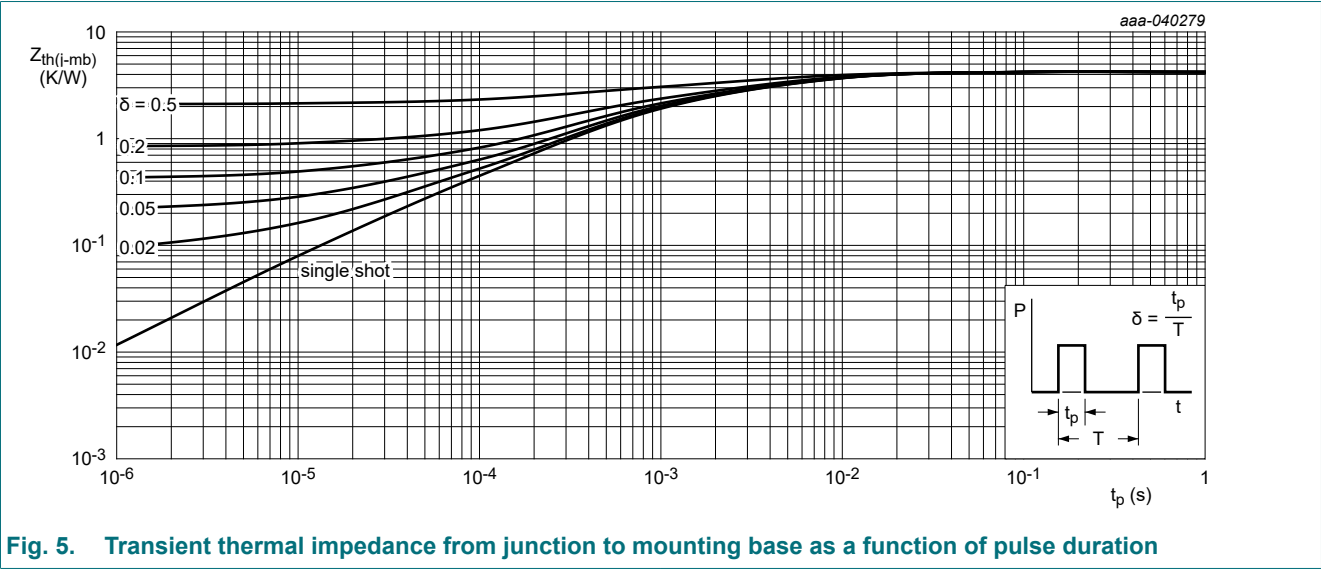


8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	2.8	4.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	40	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		80	89	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -40 °C		77	86	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		76	85	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 9 ; Fig. 10		1.45	1.7	2.15	V
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _J = 25 °C		-	-	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _J = 125 °C		-	-	20	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _J = 175 °C		-	-	200	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 6 A; T _J = 25 °C; Fig. 11		-	22	28	mΩ
		V _{GS} = 10 V; I _D = 6 A; T _J = 105 °C; Fig. 12		-	34	44	mΩ
		V _{GS} = 10 V; I _D = 6 A; T _J = 125 °C; Fig. 12		-	37	48	mΩ
		V _{GS} = 10 V; I _D = 6 A; T _J = 175 °C; Fig. 12		-	46	59	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 25 °C; Fig. 11		-	28	37	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 105 °C; Fig. 12		-	43	60	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 125 °C; Fig. 12		-	47	66	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 175 °C; Fig. 12		-	58	78	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		-	1.8	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 6 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	17	25	nC
		I _D = 6 A; V _{DS} = 40 V; V _{GS} = 5 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	8.5	-	nC
Q _{GS}	gate-source charge	I _D = 6 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	3.1	-	nC
Q _{GD}	gate-drain charge			-	1.5	-	nC
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15		-	1225	-	pF
C _{oss}	output capacitance			-	207	-	pF
C _{rss}	reverse transfer capacitance			-	6	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; R _L = 6.9 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	4	-	ns
t _r	rise time			-	3	-	ns
t _{d(off)}	turn-off delay time			-	18	-	ns
t _f	fall time			-	4	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 1.7 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.77	1	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 2.5\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;		-	24	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	14	-	nC

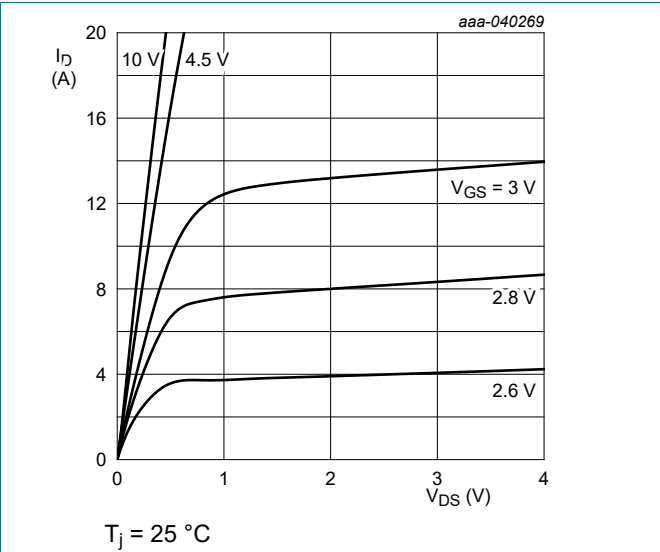


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

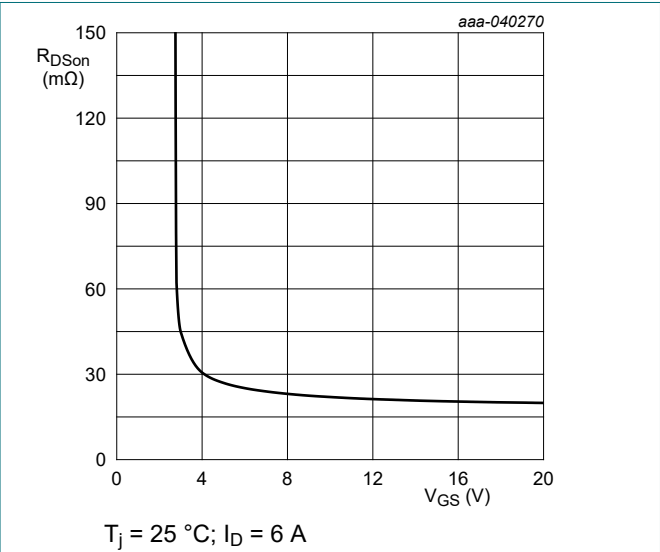


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

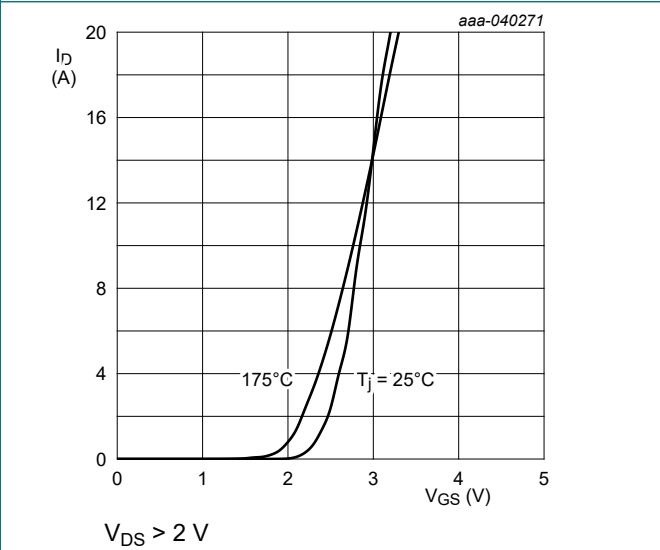


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

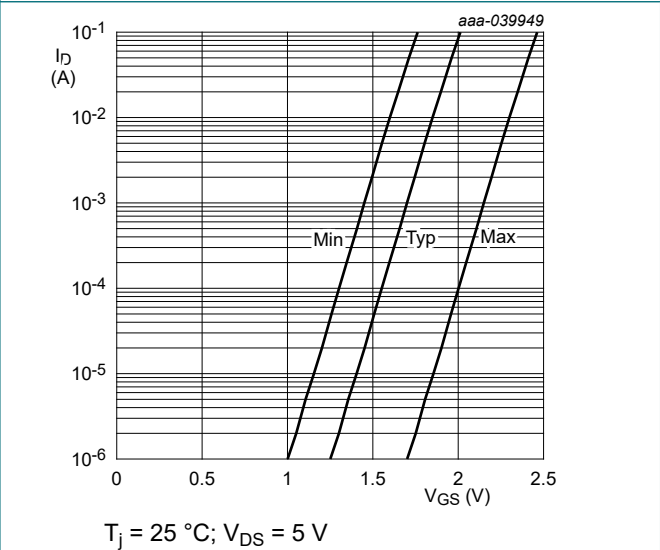


Fig. 9. Sub-threshold drain current as a function of gate-source voltage



Fig. 10. Gate-source threshold voltage as a function of junction temperature

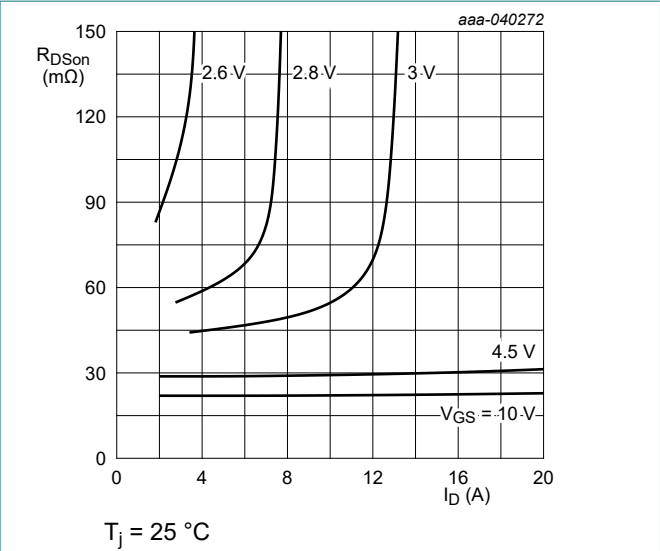


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

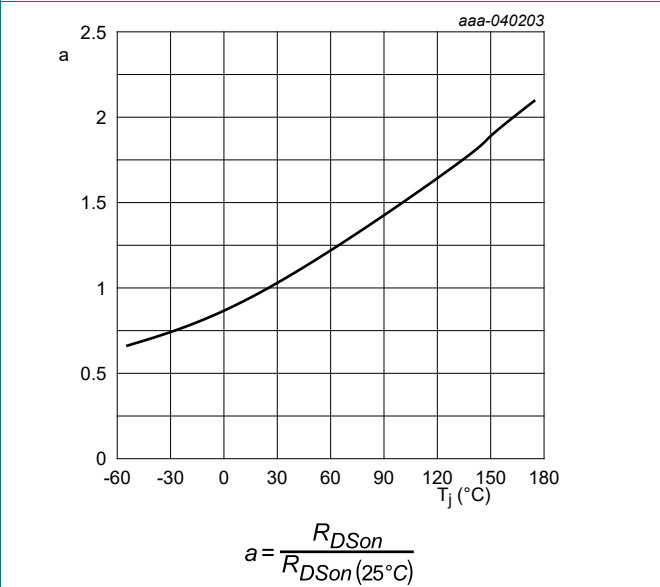


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

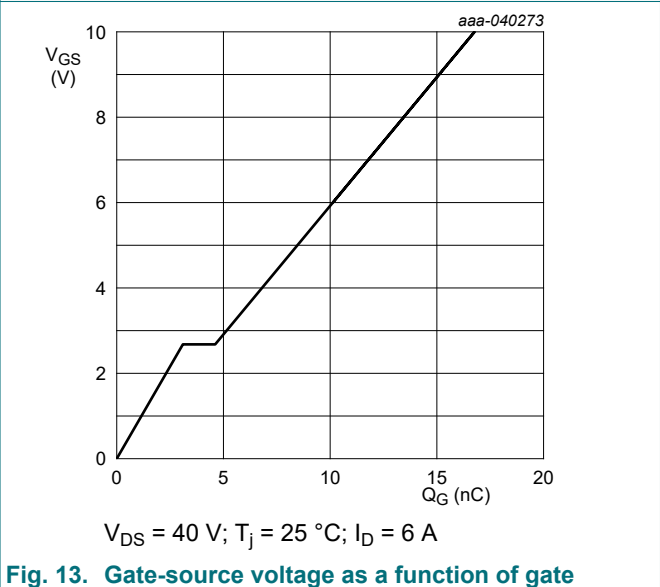


Fig. 13. Gate-source voltage as a function of gate charge; typical values



Fig. 14. Gate charge waveform definitions

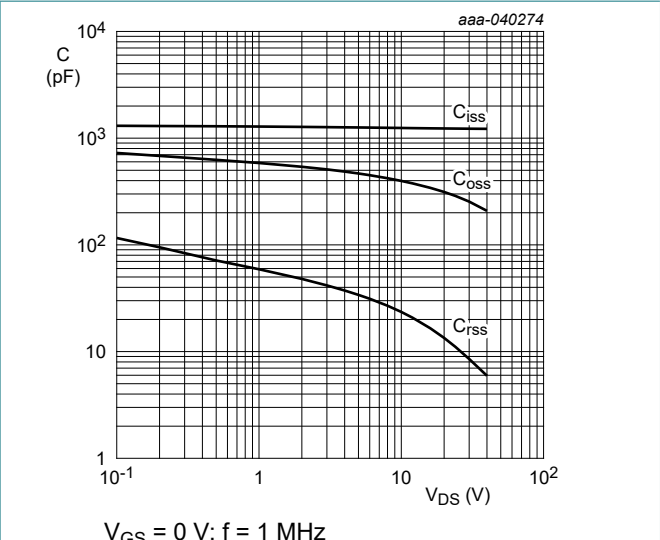


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

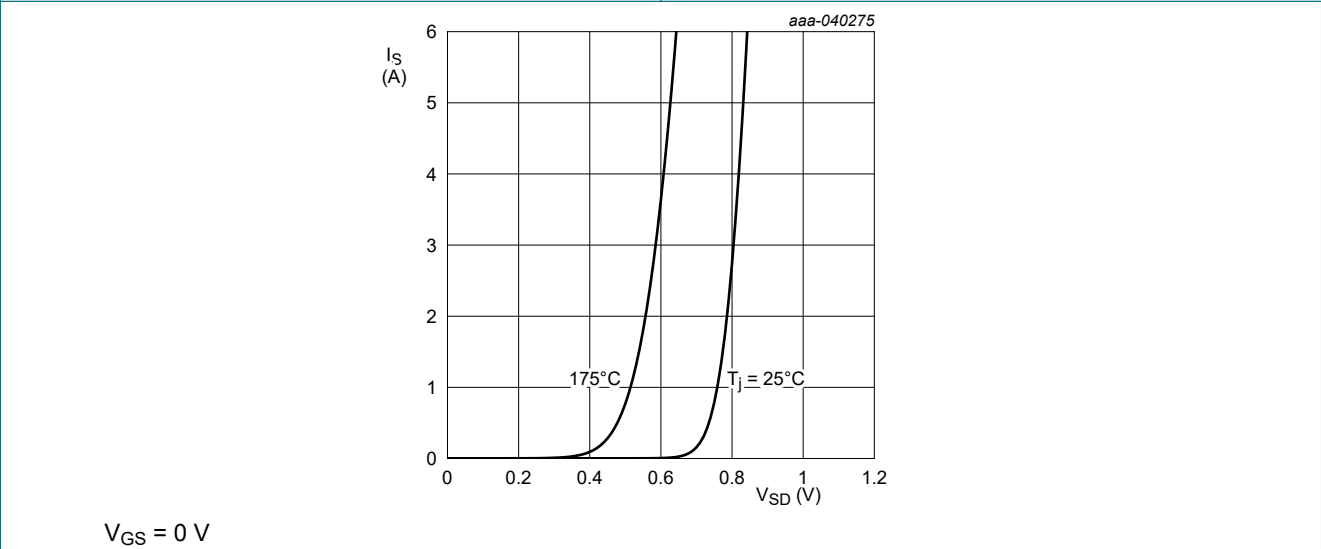


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

10. Package outline

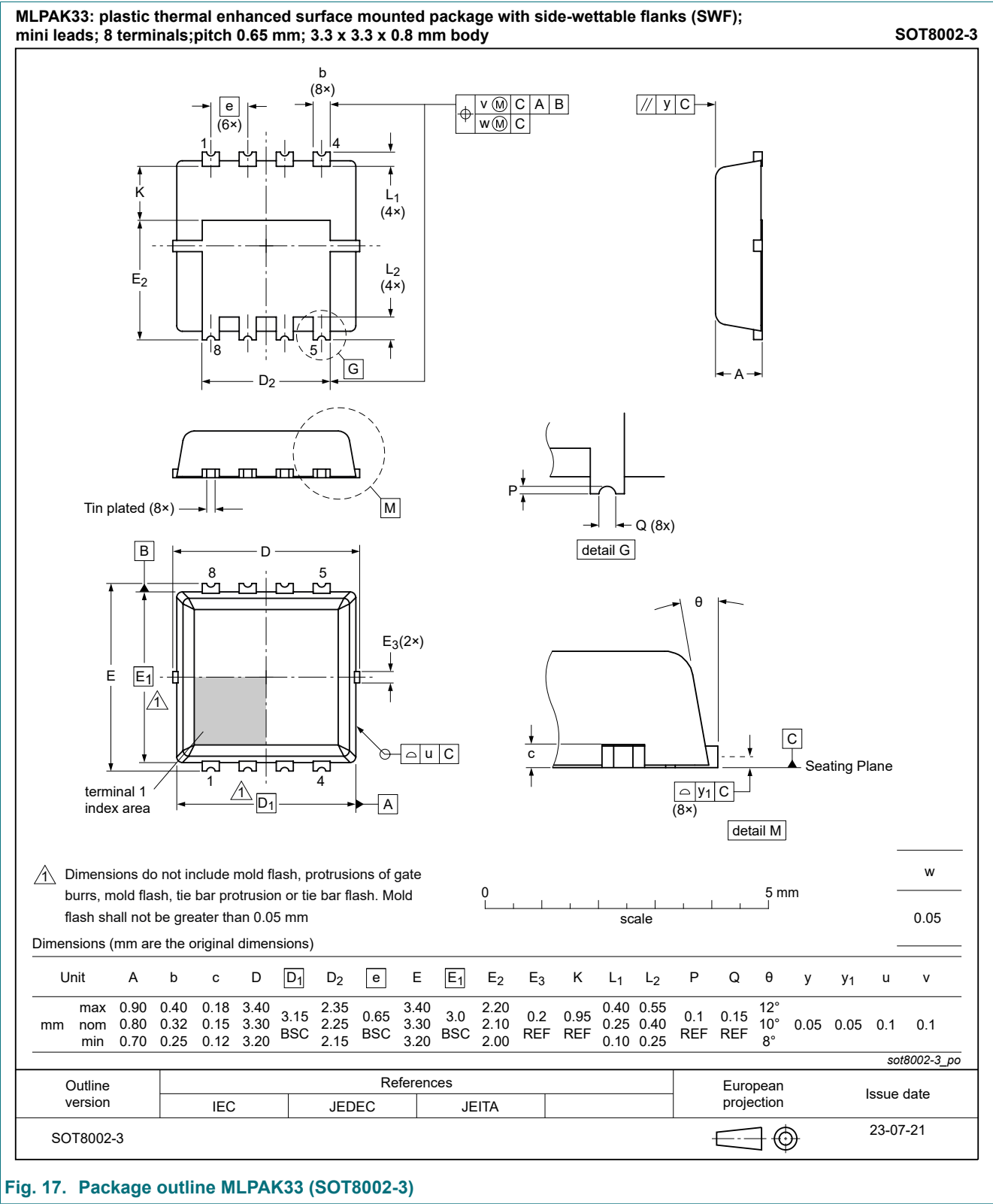


Fig. 17. Package outline MLPAK33 (SOT8002-3)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 5 June 2025