# uPOL Module

## 3A, High Efficiency uPOL Module

**MUN20AD03-SM**

## FEATURES:

- High Density uPOL Module
- 3A Output Current
- Input Voltage Range from 9V to 24V
- Output Voltage Range from 0.6V to 5.5V
- 93% Peak Efficiency(@Vin=20V)
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (OCP, OTP, SCP, OVP: Non-latching )
- Internal Soft Start
- Compact Size: 6mm*6mm*3.5mm(Max)
- Pb-free for RoHS compliant
- MSL 2, 250C Reflow

## APPLICATIONS:

- Distributed Power Supply
- Server, Workstation, and Storage
- Networking and Datacom

## GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converters that can deliver up to 3A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package.

The module has automatic operation with PWM mode and power saving mode according to loading. Instant PWM architecture to achieve fast transient responses. Other features include remote enable function, internal soft-start, non-latching over current protection and power good.

The low profile and compact size package (6.0mm × 6.0mm x 3.5mm) is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliance.

## TYPICAL APPLICATION CIRCUIT:

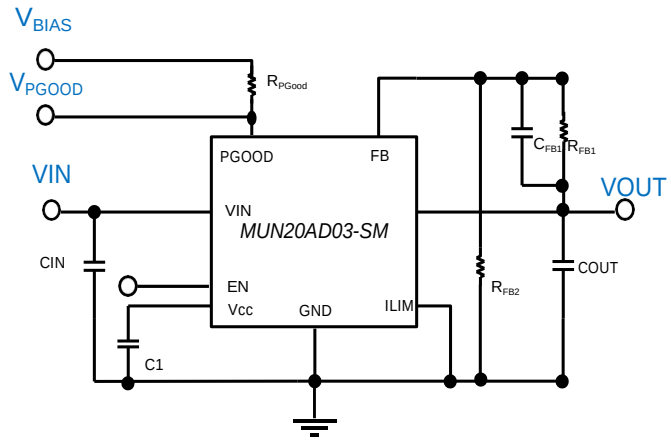



**FIGURE. 1 TYPICAL APPLICATION CIRCUIT**

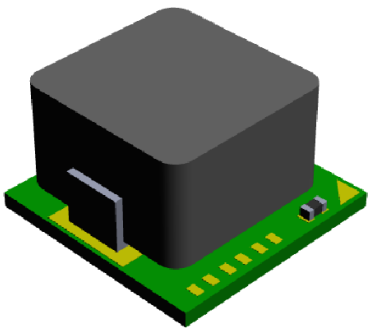


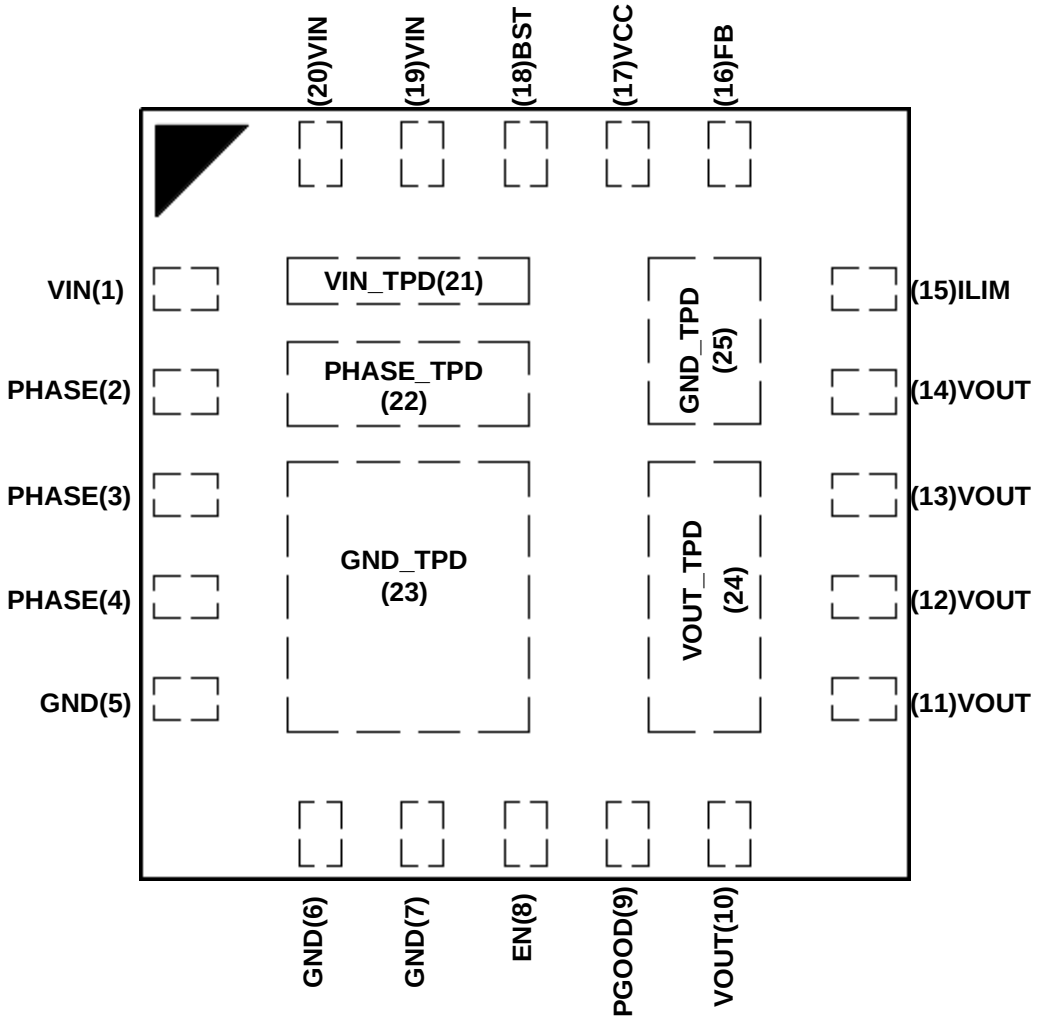
**FIGURE. 2 HIGH DENSITY uPOL MODULE**

## ORDER INFORMATION:

| Part Number | Ambient Temp. Range (°C) | Package (Pb-Free) | MSL | Note |
|---|---|---|---|---|
| MUN20AD03-SM | -40 ~ +85 | QFN | Level 2 | - |

| Order Code | Packing | Quantity |
|---|---|---|
| MUN20AD03-SM | Tape and reel | 1000 |

## PIN CONFIGURATION:




**TOP VIEW**

## PIN DESCRIPTION:

| Symbol | Pin No. | Description |
|---|---|---|
| VIN | 1, 19, 20 | Power input pin. It needs to connect input rail and thermal exposed pad of VIN_TPD(21) for heat transferring. Place the input ceramic type capacitor as closely as possible to this pin. One capacitor of 10uF at least for input capacitance. |
| PHASE | 2, 3, 4 | Switch output. Connect to thermal exposed pad of PHASE_TPD(22) for heat transferring. |
| GND | 5, 6, 7 | Power ground pin for signal, input, and output return path. This pin needs to connect one or more ground plane directly. Connect to thermal exposed pad of GND_TPD(23, 25) for heat transferring. |
| EN | 8 | On/Off control pin for module. |
| PGOOD | 9 | Power good signal pin. Open drain output when the output voltage is within 90% to 120% of regulation point. |
| VOUT | 10, 11, 12, 13, 14 | Power output pin. Connect to output and thermal exposed pad of VOUT_TPD(24) for heat transferring. Place the output capacitors as closely as possible to this pin. |
| ILIM | 15 | Current limit setting pin. Connect to GND for current limit setting. |
| FB | 16 | Feedback input. Connect an external resistor divider from the VOUT to FB to program the output voltage. |
| VCC | 17 | Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Connect a 2.2uF for Bypass capacitor. |
| BST | 18 | Boot-Strap Pin. No need connect. |
| VIN_TPD | 21 | Power input pin. Connect input rail and using for heat transferring to heat dissipation layer by Vias connection. |
| PHASE_TPD | 22 | Phase node pin. Using for heat transferring to heat dissipation layer by Vias connection. |
| GND_TPD | 23, 25 | Power ground pin. It needs to connect one or more ground plane directly and using for heat transferring to heat dissipation layer by Vias connection. |
| VOUT_TPD | 24 | Power output pin. Connect to output and using for heat transferring to heat dissipation layer by Vias connection. |

## ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| ■ Absolute Maximum Ratings | | | | | |
| VIN to GND | | - | - | +30.0 | V |
| VOUT to GND | | - | - | +6.0 | V |
| PHASE to GND | | | | +30.0 | V |
| PGOOD to GND | | | | +30.0 | V |
| ILIM to GND | | | | +4.0 | V |
| VCC to GND | | | | +4.0 | V |
| FB to GND | | | | +4.0 | V |
| EN to GND | | - | - | +30.0 | V |
| Tc | Case Temperature of Inductor | - | - | +110 | ˚C |
| Tstg | Storage Temperature | -40 | - | +125 | ˚C |
| ■ Recommendation Operating Ratings | | | | | |
| VIN | Input Supply Voltage | +9 | - | +24 | V |
| VOUT | Adjusted Output Voltage | +0.6 | | +5.5 | V |
| Ta | Ambient Temperature | -40 | - | +85 | ˚C |
| ■ Thermal Information | | | | | |
| Rth($j_{choke}$-a) | Thermal resistance from junction to ambient (Note 1) | - | 21.7 | - | °C/W |

NOTES:

1. Rth($j_{choke}$-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

## ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: $T_A$ = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 Oz. The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited. Vin=20V Vout= 5V Cin = 10uF/25V 1206x2, Cout = 47uF/6.3V/ 1206x3

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ■ Input Characteristics | | | | | | |
| $I_{SD(IN)}$ | Input shutdown current | Vin =20V, EN = GND | - | 10 | - | uA |
| $I_{(IN)}$ | Input supply current | Vin = 20V, Iout = 0A<br>Vout = 5V, EN = 5V | - | 100 | - | uA |
| $I_{S(IN)}$ | Input supply current | Vin = 20V, EN = Vin | | | | |
| | | Iout = 5mA,Vout =5V | - | 2 | - | mA |
| | | Iout = 3A,Vout =5V | - | 1 | - | A |
| ■ Output Characteristics | | | | | | |
| $I_{OUT(DC)}$ | Output continuous current range | | 0 | - | 3 | A |
| $V_{O(SET)}$ | Ouput Voltage Set Point | With 0.1% tolerance for external resistor used to set output voltage | -3 | | +3 | % $V_{O(SET)}$ |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation accuracy | Vin = 12 to 20V<br>Vout = 5V, Iout = 0A<br>Vout = 5V, Iout = 3A | - | 2 | | % $V_{O(SET)}$ |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation accuracy | Iout = 0A to 3A<br>Vin = 20V, Vout = 5V | -4 | | +3 | % $V_{O(SET)}$ |
| $V_{OUT(AC)}$ | Output ripple voltage | Vin = 20V, Vout = 5V<br>EN = Vin,20MHz Bandwidth | - | - | - | - |
| | | IOUT = 5mA | | 50 | | mVp-p |
| | | IOUT = 3A | | 20 | | mVp-p |
| ■ Dynamic Characteristics | | | | | | |
| $\Delta V_{OUT-DP}$ | Voltage change for positive load step | Iout = 1.5A to 3A<br>Current slew rate = 0.15A/uS<br>Vin = 20V, Vout = 5V | - | 30 | - | mVp-p |
| $\Delta V_{OUT-DN}$ | Voltage change for negative load step | Iout = 3A to 1.5A<br>Current slew rate = 0.15A/uS<br>Vin = 20V, Vout = 5V | - | 30 | - | mVp-p |
| ■ Control Characteristics | | | | | | |
| $F_{OSC}$ | Oscillator frequency | PWM Mode | | 0.8 | | MHz |
| $V_{REF}$ | Referance voltage | PWM Mode | 0.594 | 0.600 | 0.606 | V |
| $V_{PG}$ | Power good threshold | $V_{FB}$ Rising | 88 | 90 | 92 | % $V_{REF}$ |
| $V_{PGL}$ | Power good Low | $I_{POOD}$=4mA | 0.04 | 0.15 | 0.3 | V |
| $I_{ILIM}$ | Over current limit | ILIM=GND | 4 | | 8 | A |
| $V_{ENL}$ | EN Low threshold | | - | - | 0.3 | V |
| $V_{ENH}$ | EN High Threshold | | 0.85 | - | VIN | V |
| $T_{SS}$ | Soft Start Time | | | 600 | | uS |
| $E_{ff}$ | Efficinecy | VIN=20V ,VOUT=5V<br>IOUT=3A | | 93 | | % |

## TYPICAL PERFORMANCE CHARACTERISTICS: (5.0VOUT)

Conditions: $T_A$ = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 Oz.
The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.
Cin = 10uF/25V 1206x2, Cout = 47uF/6.3V/ 1206x3
The following figures provide the typical characteristic curves at 5.0Vout.

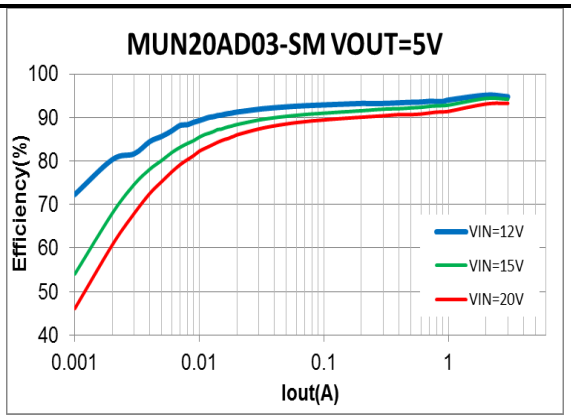



FIG.3 EFFICIENCY V.S. LOAD CURRENT

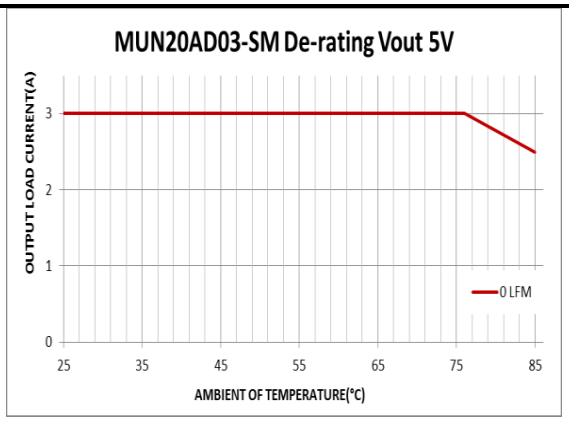



FIG.4 24VIN DE-RATING CURVE

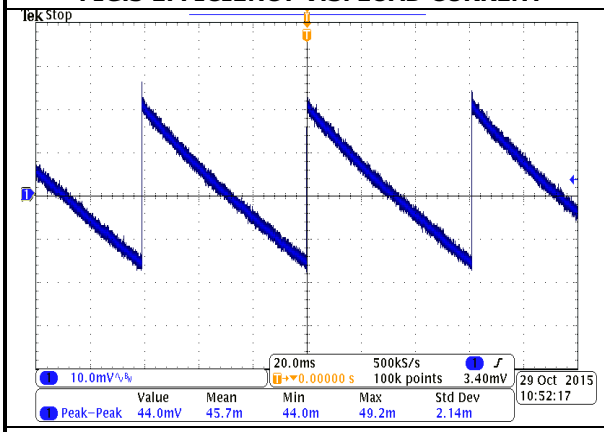



FIG.5 OUTPUT RIPPLE
(20VIN, 5.0VOUT, IOUT=0A)

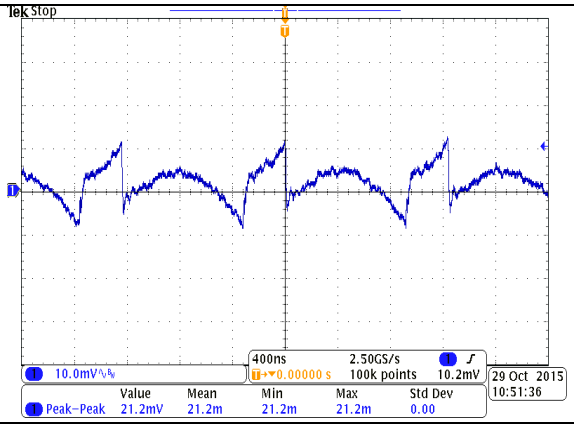



FIG.6 OUTPUT RIPPLE
(20VIN, 5.0VOUT, IOUT=3A)

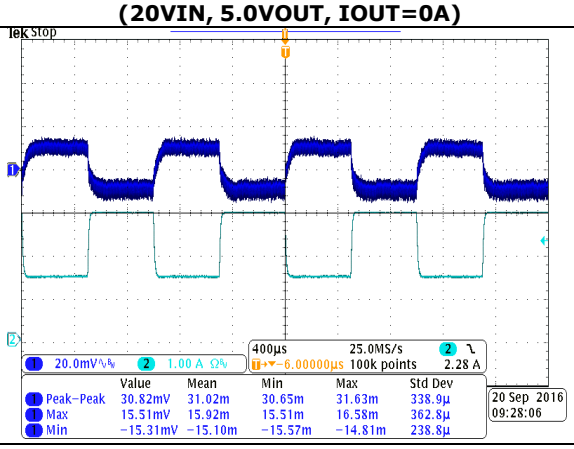



FIG.7 TRANSIENT RESPONSE
(20VIN, 5.0VOUT, 50% to 100% LOAD STEP)

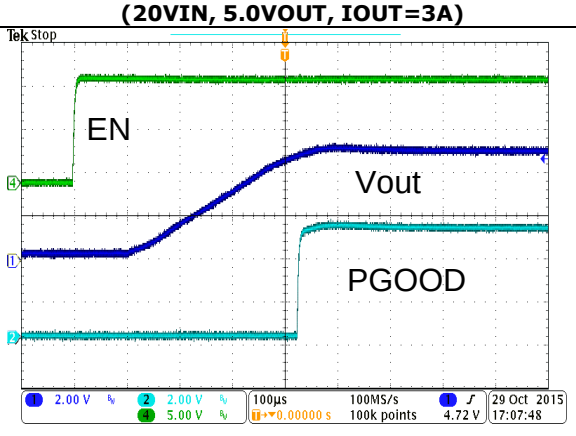



FIG.8 TURN-ON
(20VIN, 5.0VOUT, IOUT=3A)

## APPLICATIONS INFORMATION:

### REFERENCE CIRCUIT FOR GENERAL APPLICATION:

Figure 9 shows the module application schematics for input voltage +20V and turn on by input voltage directly through enable resistor (REN).

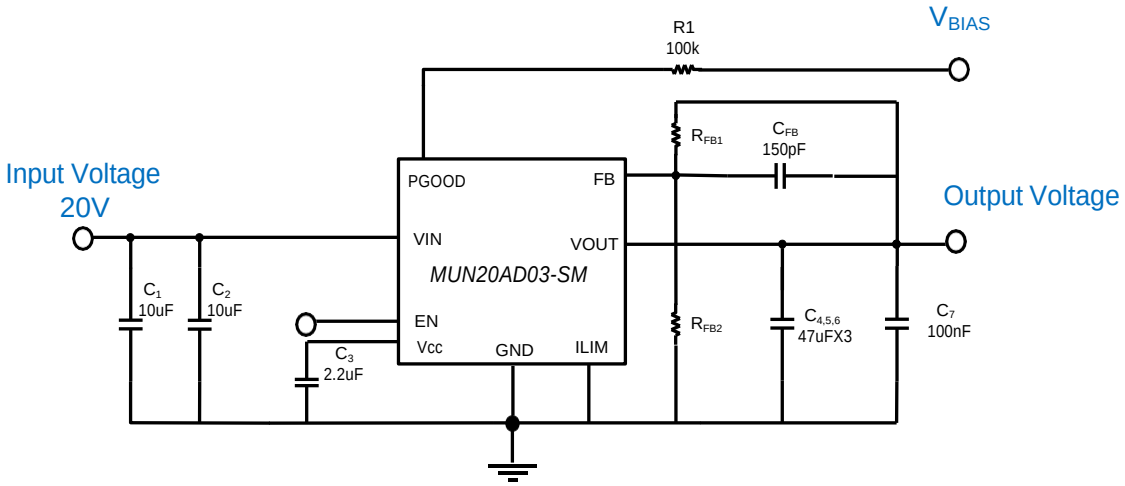



**FIG.9 REFERENCE CIRCUIT FOR GENERAL APPLICATION**

## APPLICATIONS INFORMATION: (Cont.)

### INPUT FILTERING:

The module should be connected to a source supply of low AC impedance and high inductance in which line inductance can affect the module stability. An input capacitor must be placed as near as possible to the input pin of the module so to minimize input ripple voltage and ensure module stability.

### OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response as the step load changes, an additional capacitor at the output must be connected. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

### PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±1.1% reference voltage. The output voltage can be programmed by the dividing resistor ($R_{FB}$) which connects to both Vout pin and FB pin. The output voltage can be calculated by Equation 1, resistor choice may be referred TABLE 1.

$$VOUT\,(V) = 0.6 \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad \text{(EQ.1)}$$

| Vout | RFB1(Ohm) | RFB2 (Ohm) |
|---|---|---|
| 1.0V | 13.3k | 20k |
| 1.2V | 20.0k | 20k |
| 1.8V | 40.2k | 20k |
| 2.5V | 63.3k | 20k |
| 3.3V | 90.8k | 20k |
| 5.0V | 147k | 20k |

**TABLE 1 Resistor values for common output voltages**

## REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 56 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60~150 seconds to melt the solder and make the peak temperature at the range from 245°C to 250°C (Do not exceed 30 sec). It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

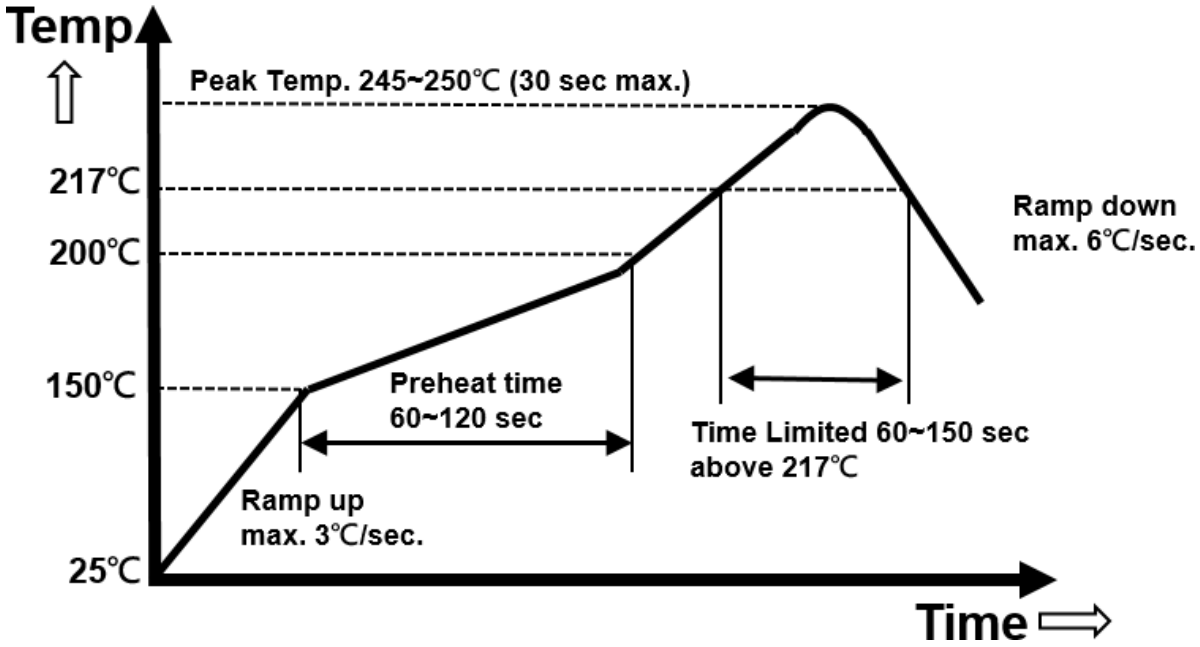



**FIG.10 Recommendation Reflow Profile**

**(Not to scale)**

***Refer to the Classification Reflow Profile of J-STD-020.**

## APPLICATIONS INFORMATION: (Cont.)

### Recommendation Layout Guide:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 59-62.

1. The ground connection between pin 23, pin25 and pin 5 to 7 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias
2. Place high frequency ceramic capacitors between pin 1, pin 19 to 21 (VIN), and pin 23, pin25, pin 5 to 7 (GND) for input side; and pin 24, pin 10 to 14 (VOUT), and pin 23, pin25, pin 5 to 7 (GND) for output side, as close to module as possible to minimize high frequency noise.
3. Keep the $R_{FB}$ connection trace to the module pin 16 (FB) short.
4. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
5. Avoid any sensitive signal traces near the pin 24, and pin 2 to 4 (PHASE).

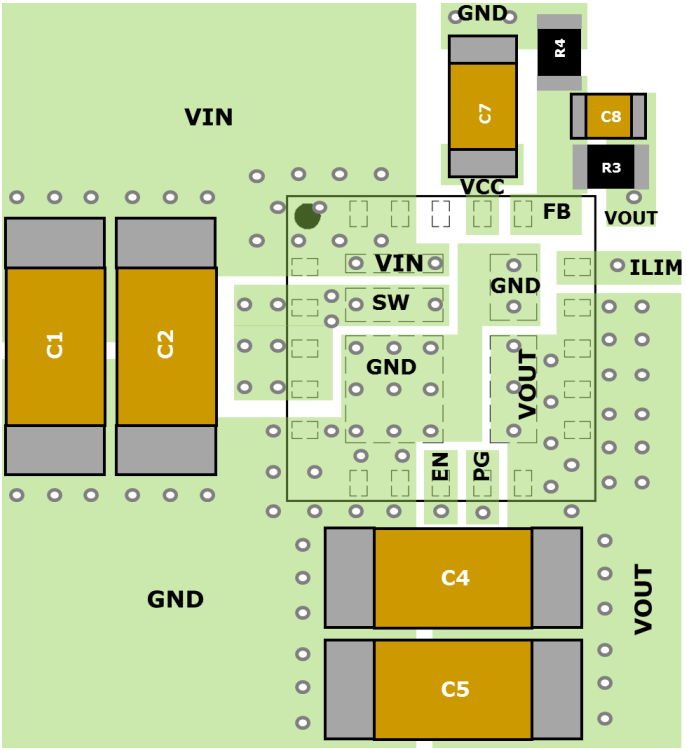



**FIG.11 Recommendation Layout (Top)**

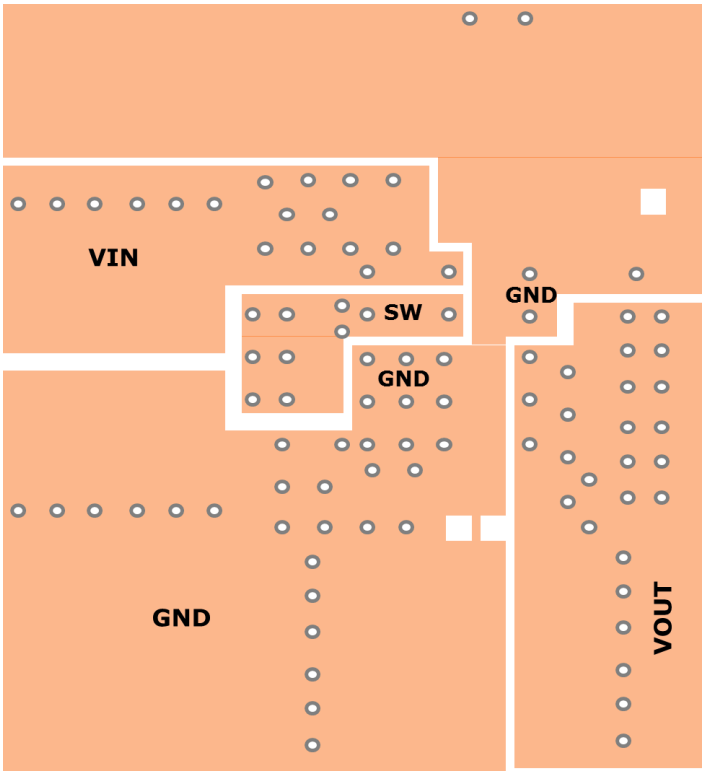



FIG.12 Recommendation Layout (Middle 1)

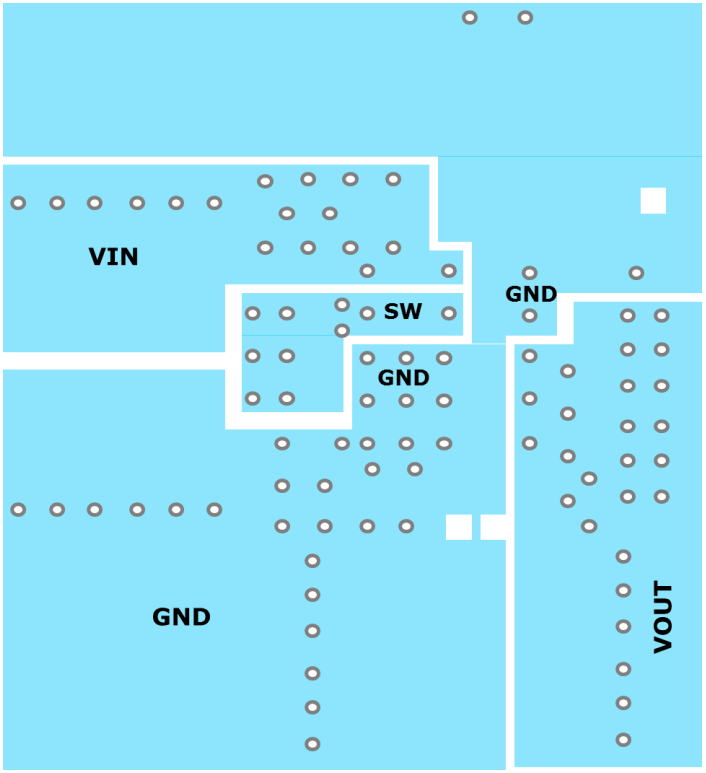



FIG.13 Recommendation Layout (Middle 1)

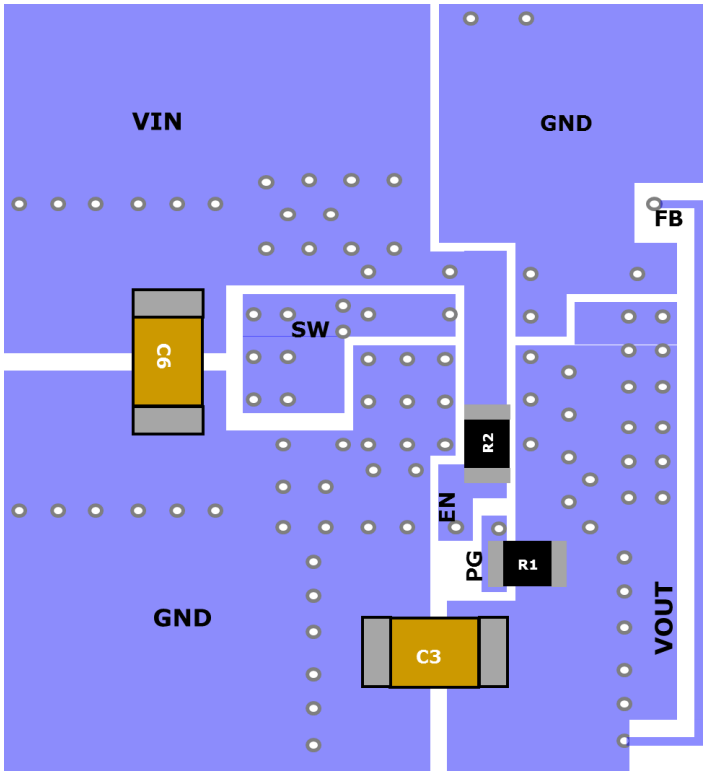



**FIG.14 Recommendation Layout (Middle 1)**

## THERMAL CONSIDERATIONS:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers 2oz. The case temperature of module sensing point is shown as FIG.15 Then Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

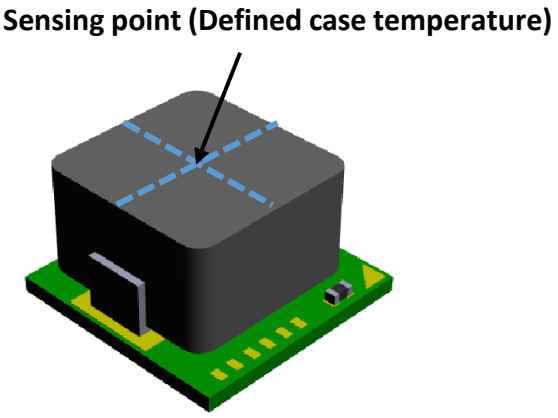
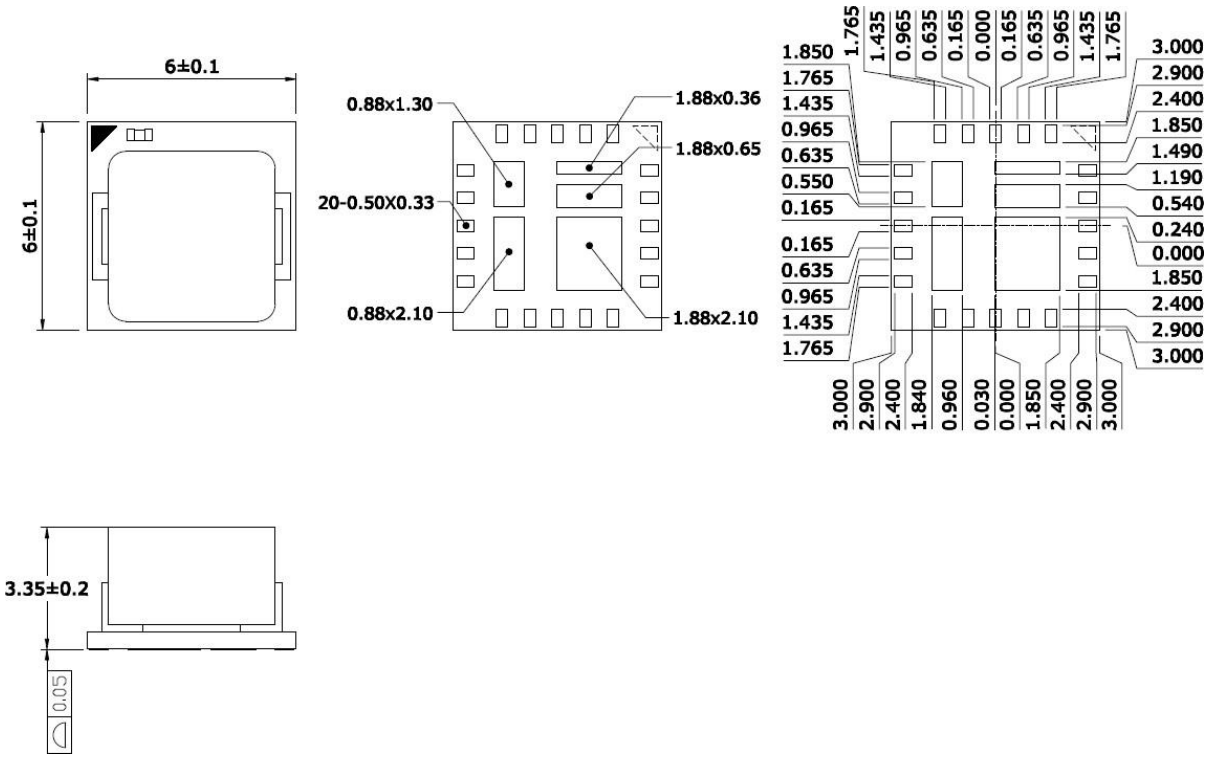



**FIG.15 CASE TEMPERATURE SENSING POINT**

## PACKAGE OUTLINE DRAWING:

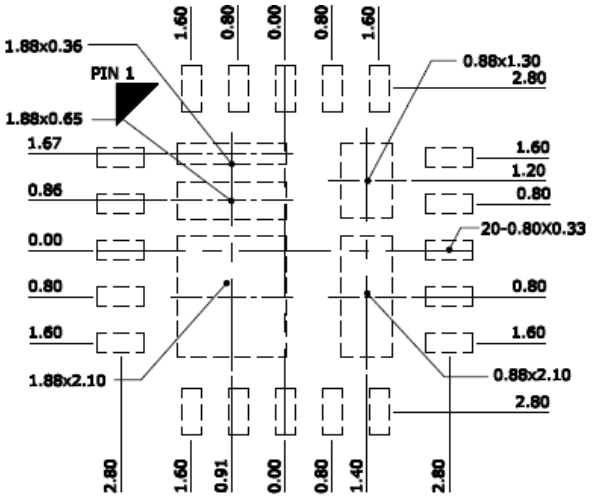
Unit: mm

General Tolerance: +/- 0.1mm



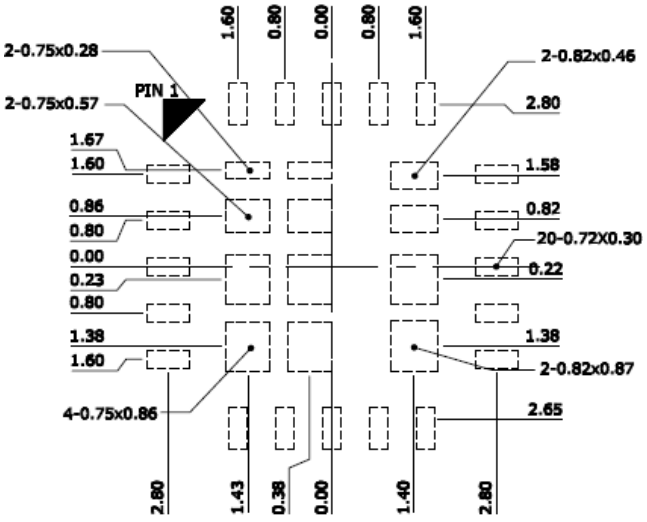
## LAND PATTERN REFERENCE:

Unit: mm




Top View

TYPICAL RECOMMENDED LAND PATTERN




Top View

STENCIL PATTERN WITH SQUARE PADS

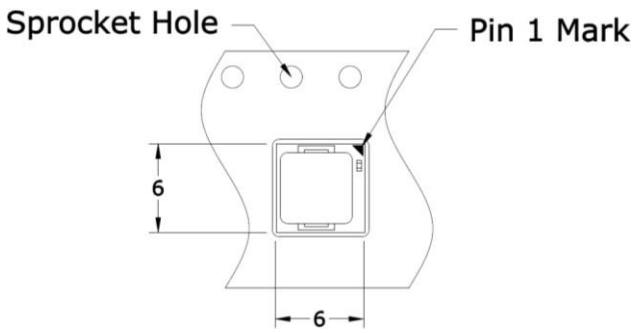
*Based on 0.1~0.15mm thickness stencil (Reference only)

*Recommended solder paste coverage 55~100%

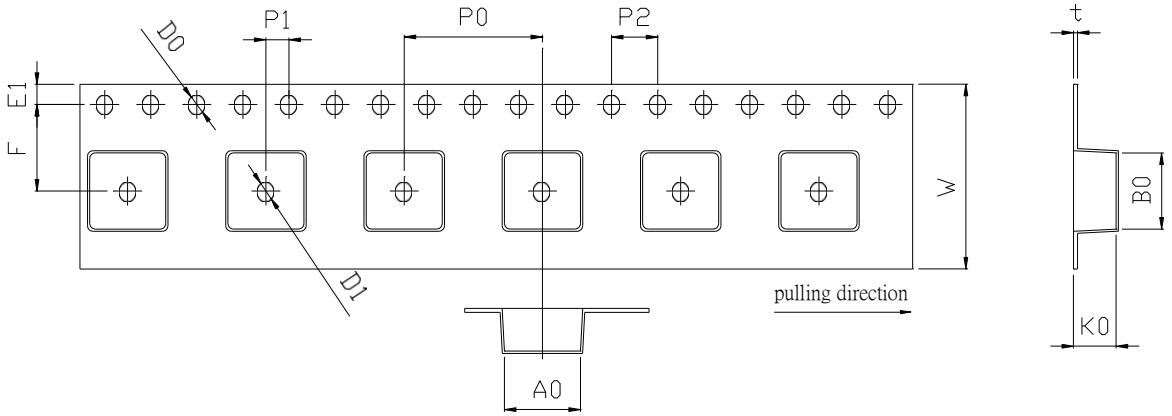
## PACKING REFERENCE:

Unit: mm

**Package In Tape Loading Orientation**




**Tape Dimension**

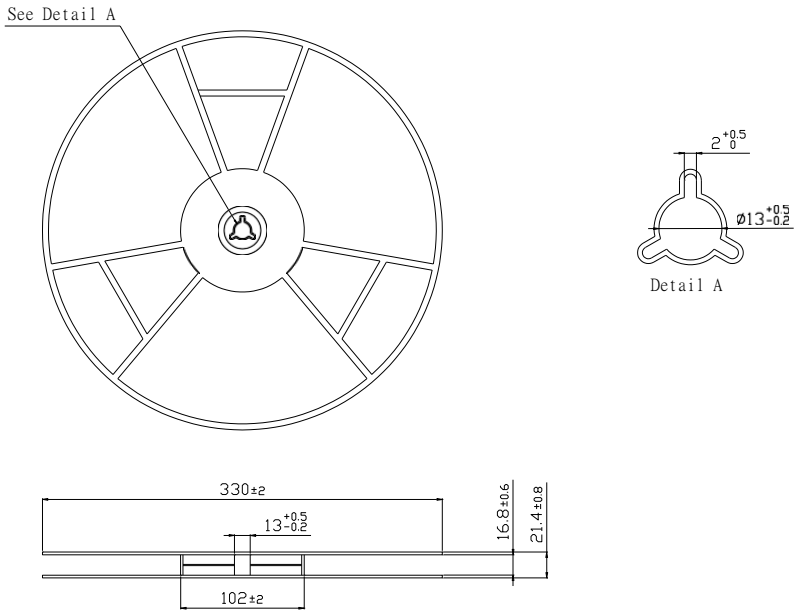



| | | | |
|---|---|---|---|
| A0 | 6.60 ± 0.10 | E1 | 1.75 ± 0.10 |
| B0 | 6.60 ± 0.10 | K0 | 3.70 ± 0.10 |
| F | 7.50 ± 0.10 | P0 | 12.00 ± 0.10 |
| W | 16.00 ± 0.30 | P1 | 2.00 ± 0.10 |
| D0 | φ1.5 +0.1/-0.0 | P2 | 4.00 ± 0.10 |
| D1 | φ1.5 Min. | t | 0.35 ± 0.05 |

## PACKING REFERENCE: (Cont.)

Unit: mm

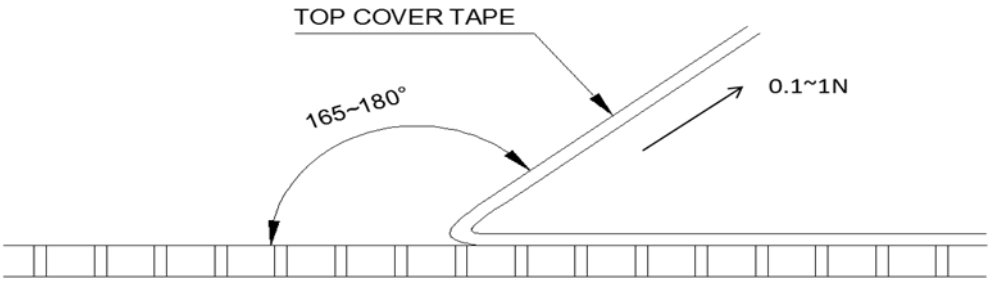
**Reel Dimension**




**Peel Strength of Top Cover Tape**

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



## REVERSION HISTORY:

| Date | Revision | Changes |
|---|---|---|
| 2015.10.29 | Preliminary | Release the preliminary specification. |
| 2016.05.05 | 01 | Change FB Resistor for output voltages |
| 2016.06.19 | 02 | Add test Conditions<br>Change Recommendation Operating Ratings |
| 2017.03.30 | 03 | Add PGOOD sink current spec |
| 2022.12.23 | 04 | 1. Page 9 update reflow parameters and FIG.10<br>2. Page 12, Add "THERMAL CONSIDERATIONS".<br>3. Page 14 change the thickness description of stencil. Add note. |
| 2024.12.16 | A1 | Synchronized with document management number |