Spartan UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics

DS930 (v1.0) January 24, 2025 **Advance Product Specification**

Summary

The AMD Spartan™ UltraScale+™ FPGAs are available in -2 and -1 speed grades, with -2E and -2I devices having the highest performance. Some -1LI devices can operate at a V_{CCINT} voltage at 0.85V or 0.72V and provide lower maximum static power. When operated at V_{CCINT} = 0.85V, using a -1LI device, the speed specification for the L devices is the same as the -1I speed grade. When operated at V_{CCINT} = 0.72V, the -1LI performance and static and dynamic power is reduced.

DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Spartan UltraScale+ FPGAs, is available on the AMD Technical Information Portal.

DC Characteristics

Absolute Maximum Ratings

Table 1: **Absolute Maximum Ratings**

Symbol	Description[1]	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.500	1.000	V
V_{CCINT_IO}[2]	Internal supply voltage for the I/O banks	–0.500	0.980	V
V_{CCAUX}[3]	Auxiliary supply voltage	–0.500	1.960	V
V_{CCBRAM}[2]	Supply voltage for the block RAM and UltraRAM	–0.500	0.980	V

Table 1: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
V_{CCO}	Output drivers supply voltage for HD I/O banks	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks and configuration bank 0	–0.500	1.960	V
	Output drivers supply voltage for XP5IO banks	–0.500	1.650	V
V_{CCAUX_IO}[3]	Auxiliary supply voltage for the I/O banks. Available as V_{CCAUX_HDIO} for HD I/O banks and V_{CCAUX_HPIO} for HP I/O banks.	–0.500	1.960	V
V_{REF}	Input reference voltage for HP I/O banks	–0.500	2.000	V
V_{IN}[4, 5, 6, 7]	I/O input voltage for HD I/O, HP I/O, and XP5IO I/O banks	–0.550	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad	–20	20	mA
I_{RMS}	Available RMS output current at the pad	–20	20	mA
GTH Transceiver[8]				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating[9]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable[10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	6	mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC	–0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC	–0.500	2.000	V
Temperature[11]				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum dry rework soldering temperature	–	260	°C
	Maximum reflow soldering temperature for SBVC529, SBVB625, SBVF784, SBVG784, SBVA1024, and FSVG1156 packages	–	250	°C
	Maximum reflow soldering temperature for CMVA361, CMVA529, and CMVB529 packages	–	245	°C

Table 1: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
T_j	Maximum junction temperature	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_HPIO} and V_{CCAUX_HDIO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. For I/O operation, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).
6. When operating outside of the recommended operating conditions, refer to Table 4 and Table 5 for maximum overshoot and undershoot specifications.
7. V_{IN} for the POR_OVERRIDE pin is unique. POR_OVERRIDE must be connected to either GND (default) or V_{CCINT}. See T_{POR} in Configuration Switching Characteristics for additional information.
8. For more information on supported GTH transceiver terminations see the *UltraScale Architecture GTH Transceivers User Guide* (UG576).
9. AC coupled operation is not supported for RX termination = floating.
10. DC coupled operation is not supported for RX termination = programmable.
11. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575).

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions**

Symbol	Description[1, 2]	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage	0.825	0.850	0.876	V
	For -1LI (V_{CCINT} = 0.72V) devices: internal supply voltage	0.698	0.720	0.742	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks	0.825	0.850	0.876	V
V_{CCBRAM}[3]	Block RAM and UltraRAM supply voltage	0.825	0.850	0.876	V
V_{CCAUX}[8]	Auxiliary supply voltage	1.746	1.800	1.854	V
V_{CCO}[4]	Supply voltage for HD I/O banks[5]	1.164	–	3.400	V
	Supply voltage for HP I/O banks and configuration bank 0[6]	0.970	–	1.854	V
	Supply voltage for XP5IO I/O banks[7]	0.970	–	1.545	V
V_{CCAUX_IO}[8]	Auxiliary I/O supply voltage. Available as V_{CCAUX_HDIO} for HD I/O banks and V_{CCAUX_HPIO} for HP I/O banks.	1.746	1.800	1.854	V
V_{IN}[9, 10]	I/O input voltage	–0.200	–	V_{CCO} + 0.200	V
I_{IN}[11]	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
GTH Transceiver					
$V_{MGTAVCC}$[12]	Analog supply voltage for the GTH transceiver	0.873	0.900	0.927	V
$V_{MGTAVTT}$[12]	Analog supply voltage for the GTH transmitter and receiver termination circuits	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$[12]	Auxiliary analog QPLL voltage supply for the transceivers	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$[12]	Analog supply voltage for the resistor calibration circuit of the GTH transceiver column	1.164	1.200	1.236	V
System Monitor					
V_{CCADC}	System Monitor supply relative to GNDADC	1.746	1.800	1.854	V

Table 2: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2]	Min	Typ	Max	Units
V_{REFP}	System Monitor externally supplied reference voltage relative to GNDADC	1.200	1.250	1.300	V
Temperature					
T_j[13]	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for eFUSE programming[14]	–40	–	125	°C

Notes:

1. All voltages are relative to GND, assuming supplies are present.
2. For the design of the power distribution system consult the *UltraScale Architecture PCB Design User Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the recommended nominal operating voltage is 1.5V or 1.8V, and the minimum voltage for power on and during configuration is 1.455V.
5. Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±3%.
6. Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V at ±3%.
7. Includes V_{CCO} of 1.0V, 1.1V, 1.2V, 1.35V, and 1.5V at ±3%.
8. V_{CCAUX_IO} must be connected to V_{CCAUX}.
9. The lower absolute voltage specification always applies.
10. V_{IN} for the POR_OVERRIDE pin is unique. POR_OVERRIDE must be connected to either GND (default) or V_{CCINT}. See T_{POR} in Configuration Switching Characteristics for additional information.
11. A total of 200 mA per bank should not be exceeded.
12. Each voltage listed requires filtering as described in the *UltraScale Architecture GTH Transceivers User Guide* (UG576).
13. AMD recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The system monitor temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, when using the system monitor with an external reference of 1.25V, and when the system monitor reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
14. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

DC Characteristics Over Recommended Operating Conditions

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (HD I/O and HP I/O[2]) (sample-tested)	–	–	15	µA
	Input or output leakage current per pin (XP5IO I/O) (sample-tested)	–	–	100	µA
C_{IN}[3]	Die input capacitance at the pad (HP I/O)	–	–	3.1	pF
	Die input capacitance at the pad (HD I/O)	–	–	4.75	pF
	Die input capacitance at the pad (XP5IO I/O)	–	–	1.90	pF

Table 3: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V	75	–	190	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V	29	–	120	µA
$I_{CCADCON}$	Analog supply current for the SYSMON circuits in the power-up state	–	–	8	mA
$I_{CCADCOFF}$	Analog supply current for the SYSMON circuits in the power-down state	–	–	1.5	mA
I_{PFS}[4]	V_{CCAUX} additional supply current during eFUSE programming	–	–	115	mA
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
	1/6 V_{CCO} (XP5IO I/O banks only)		V_{CCO} x 1/6		V
	1/8 V_{CCO} (XP5IO I/O banks only)		V_{CCO} x 1/8		V
Differential termination	Programmable differential termination (TERM_100) for HP I/O and XP5IO I/O banks	–35%	100	+35%	Ω
n	Temperature diode ideality factor	–	1.026	–	–
r	Temperature diode series resistance	–	2	–	Ω
Calibrated programmable on-die termination (DCI) in HP I/O banks[5] (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40	–10%[6]	40	+10%[6]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48	–10%[6]	48	+10%[6]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60	–10%[6]	60	+10%[6]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–10%[6]	40	+10%[6]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–10%[6]	48	+10%[6]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–10%[6]	60	+10%[6]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–10%[6]	120	+10%[6]	Ω
	Programmable input termination to $V_{CCO}$where ODT = RTT_240	–10%[6]	240	+10%[6]	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	–50%	240	+50%	Ω

Table 3: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
Calibrated programmable on-die termination (DCI) in XP5IO I/O banks[5] (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination where x = target impedance of 8, 60, 120, or 240				Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
5. VRP resistor tolerance is (240Ω ±1%).
6. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
7. On-die input termination resistance, for more information see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%
V_{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 5: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for XP5IO I/O Banks**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C

Quiescent Supply Current

Table 7: **Typical Quiescent Supply Current**

Symbol	Description[1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XCSU10P				mA
		XCSU25P				mA
		XCSU35P				mA
		XCSU50P				mA
		XCSU55P				mA
		XCSU65P				mA
		XCSU100P				mA
		XCSU150P				mA
		XCSU200P				mA

Table 7: **Typical Quiescent Supply Current** *(cont'd)*

Symbol	Description[1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current	XCSU10P				mA
		XCSU25P				mA
		XCSU35P				mA
		XCSU50P				mA
		XCSU55P				mA
		XCSU65P				mA
		XCSU100P				mA
		XCSU150P				mA
		XCSU200P				mA
I_{CCOQ}	Quiescent V_{CCO} supply current	All devices				mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XCSU10P				mA
		XCSU25P				mA
		XCSU35P				mA
		XCSU50P				mA
		XCSU55P				mA
		XCSU65P				mA
		XCSU100P				mA
		XCSU150P				mA
		XCSU200P				mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XCSU10P				mA
		XCSU25P				mA
		XCSU35P				mA
		XCSU50P				mA
		XCSU55P				mA
		XCSU65P				mA
		XCSU100P				mA
		XCSU150P				mA
		XCSU200P				mA

Table 7: **Typical Quiescent Supply Current** *(cont'd)*

Symbol	Description[1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XCSU10P				mA
		XCSU25P				mA
		XCSU35P				mA
		XCSU50P				mA
		XCSU55P				mA
		XCSU65P				mA
		XCSU100P				mA
		XCSU150P				mA
		XCSU200P				mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, and all I/O pins are 3-state and floating.
3. Use the Power Design Manager (PDM) tool (download at www.amd.com/power) to estimate static power consumption for conditions or supplies other than those specified.

Power Supply Sequencing

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Power Supply Requirements

Table 8 shows the minimum current, in addition to I_{CCQ} maximum, required by each Spartan UltraScale+ FPGA for proper power-on and configuration. If these current minimums are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Power Design Manager (PDM) tool (download at www.amd.com/power) to estimate current drain on these supplies. PDM is also used to estimate power-on current for all supplies.

Table 8: **Power-on Current by Device**

Device	$I_{CCINTMIN}$	$I_{CCBRAMMIN}$ + I_{CCINT_IOMIN}	I_{CCOMIN}	$I_{CCAUXMIN}$ + I_{CCAUX_IOMIN}	Units
XCSU10P	464	155	50	111	mA
XCSU25P	464	155	50	111	mA
XCSU35P	464	155	50	111	mA
XCSU50P					
XCSU55P					
XCSU65P					
XCSU100P					
XCSU150P					
XCSU200P					

Table 9: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

I/O Levels

Table 10: **SelectIO DC Input and Output Levels For HD I/O Banks**

I/O Standard[1, 2]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.200	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.200	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	Note 4	Note 4
LVCMOS18	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	Note 4	Note 4
LVCMOS25	–0.200	0.700	1.700	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.200	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.200	0.800	2.000	3.400	0.400	2.400	Note 4	Note 4
SSTL135	–0.200	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.9	–8.9
SSTL15	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	8.9	–8.9
SSTL18_I	–0.200	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	8.0	–8.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).
3. Supported drive strengths of 4 or 8 mA in HD I/O banks.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.

Table 11: **SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard[1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.200	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.200	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.200	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.200	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
SSTL135	–0.200	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	9.0	–9.0
SSTL15	–0.200	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	10.0	–10.0
SSTL18_I	–0.200	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	7.0	–7.0
MIPI_DPHY_ DCI_LP[6]	–0.200	0.550	0.880	V_{CCO} + 0.200	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).
3. POD10 and POD12 DC input and output levels are shown in Table 13, Table 21, and Table 23.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.
7. When operating at data rates greater than 1500 Mb/s, the minimum V_{IH} is 0.790V. MIPI D-PHY data rates are outlined in Table 36.

Table 12: **SelectIO DC Input and Output Levels for XP5IO I/O Banks**

I/O Standard[1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.200	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.200	50% V_{CCO} – 0.080	50% V_{CCO} + 0.080	V_{CCO} + 0.200	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSUL_12	–0.200	50% V_{CCO} – 0.130	50% V_{CCO} + 0.130	V_{CCO} + 0.200	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS10	–0.100	30% V_{CCO}	70% V_{CCO}	V_{CCO}	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS11	–0.100	35% V_{CCO}	65% V_{CCO}	V_{CCO}	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS12	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS135	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15/HSLVDCI_15	–0.200	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.200	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.200	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
SSTL135	–0.200	50% V_{CCO} – 0.090	50% V_{CCO} + 0.090	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	9.0	–9.0
SSTL15	–0.200	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.200	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	10.0	–10.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).
3. POD10 and POD12 DC input and output levels are shown in Table 14, Table 20, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in XP5IO I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in XP5IO I/O banks.

Table 13: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards for HP I/O Banks**

I/O Standard[1, 2]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.200	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.200
POD12	–0.200	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.200

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

Table 14: DC Input Levels for Single-ended POD10, POD12, LVSTL_11, LVSTL06_12, and LVSTL05_10 I/O Standards for XP5IO I/O Banks

I/O Standard[1, 2]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.200	70% V_{CCO} – 0.068	70% V_{CCO} + 0.068	V_{CCO} + 0.200
POD12	–0.200	70% V_{CCO} – 0.068	70% V_{CCO} + 0.068	V_{CCO} + 0.200
LVSTL05_10				
LVSTL06_12				
LVSTL11				

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

Table 15: Differential SelectIO DC Input and Output Levels for HP I/O Banks

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]			V_{ILHS}[3]	V_{IHHS}[3]	V_{OCM} (V)[4]			V_{OD} (V)[5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS[8]	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY for operation < 1.5 GB/s[9]	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270
MIPI_DPHY for operation > 1.5 GB/s[9]	0.070	–	0.330	0.040	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 25.
7. LVDS is specified in Table 27.
8. The SUB_LVDS receiver is supported in HP I/O and HD I/O banks. The SUB_LVDS transmitter is supported only in HP I/O banks.
9. High-speed option for MIPI_DPHY. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 16: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 17: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard[1]	V_{ICM} (V)[2]			V_{ID} (V)[3]		V_{OL} (V)[4]	V_{OH} (V)[5]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	V_{CCO}/2	(V_{CCO}/2) + 0.150	0.100	–	0.400	V_{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	V_{CCO}/2	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	(V_{CCO}/2) – 0.175	V_{CCO}/2	(V_{CCO}/2) + 0.175	0.100	–	0.400	V_{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	(V_{CCO}/2) – 0.120	V_{CCO}/2	(V_{CCO}/2) + 0.120	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	(V_{CCO}/2) – 0.150	V_{CCO}/2	(V_{CCO}/2) + 0.150	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.0	–8.0
DIFF_SSTL135	(V_{CCO}/2) – 0.150	V_{CCO}/2	(V_{CCO}/2) + 0.150	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	9.0	–9.0
DIFF_SSTL15	(V_{CCO}/2) – 0.175	V_{CCO}/2	(V_{CCO}/2) + 0.175	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	10.0	–10.0
DIFF_SSTL18_I	(V_{CCO}/2) – 0.175	V_{CCO}/2	(V_{CCO}/2) + 0.175	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 19, Table 21, and Table 23.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for XP5IO I/O Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–0.8
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 19: **DC Input Levels for Differential POD10 and POD12 I/O Standards for HP I/O Banks**

I/O Standard[1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.630	0.700	0.770	0.140	–
DIFF_POD12	0.756	0.840	0.924	0.160	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

Table 20: **DC Input Levels for Differential POD10, POD12, LVSTL_11, LVSTL06_12, and LVSTL05_10 I/O Standards for XP5IO I/O Banks**

I/O Standard[1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.630	0.700	0.770	0.140	–
DIFF_POD12	0.756	0.840	0.924	0.160	–
DIFF_LVSTL05_10					–
DIFF_LVSTL06_12					–
DIFF_LVSTL_11					–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards for HP I/O Banks

Symbol	Description[1, 2]	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 23)	36	40	44	Ω
R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 23)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

Table 22: DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL_11, LVSTL06_12, and LVSTL05_10 Standards for XP5IO I/O Banks

I/O Standard	Symbol	Description[1, 2]	V_{OUT}	Min	Typ	Max	Units
POD10, POD12	R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 24)	32	40	48	Ω
	R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 24)	32	40	48	Ω
LVSTL05_10	R_{OL}	Pull-down resistance	$V_{OCM\_DC\_LOW}$				Ω
	R_{OH}	Pull-up resistance	$V_{OCM\_DC\_HIGH}$				Ω
LVSTL06_12	R_{OL}	Pull-down resistance	$V_{OCM\_DC\_LOW}$				Ω
	R_{OH}	Pull-up resistance	$V_{OCM\_DC\_HIGH}$				Ω
LVSTL11	R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 24)				Ω
	R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 24)				Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861).

Table 23: Definitions for DC Output Levels for Single-ended and Differential POD10 and POD12 Standards for HP I/O Banks

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)	0.8 x V_{CCO}	V

Table 24: Definitions for DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL_11, LVSTL06_12, and LVSTL05_10 Standards for XP5IO I/O Banks

I/O Standard	Symbol	Description	All Speed Grades	Units
POD10, POD12	V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)		V
LVSTL_11	V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)		V
LVSTL05_10	V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)		V
LVSTL06_12	$V_{OM\_DC\_LOW}$	DC output Mid measurement level (for IV curve linearity), drive logic Low		V
	$V_{OM\_DC\_HIGH}$	DC output Mid measurement level (for IV curve linearity), drive logic High		V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861) for more information.

Table 25: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{CCO}	Supply voltage	2.425	2.500	2.575	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	100	350	600	mV
V_{ICM}	Input common-mode voltage	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS15)

The LVDS15 standard is available in the XP5IO I/O banks. See the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861) for more information.

Table 26: **LVDS_15 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage		1.455	1.500	1.545	V
V_{ODIFF}[2]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}[2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.200	1.320	V
V_{IDIFF}[3]	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600[3]	mV
V_{ICM_DC}[4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.320	V
V_{ICM_AC}[5]	Input common-mode voltage (AC coupling)		200	–	330	mV

Notes:

1. In XP5IO banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. AC coupling with external bias and external differential termination with EQUALIZATION settings enabled. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, or EQ_LEVEL4, any setting except EQ_NONE.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861) for more information.

Table 27: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage		1.746	1.800	1.854	V
V_{ODIFF}[2]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}[2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}[3]	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600[3]	mV
V_{ICM_DC}[4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V
V_{ICM_AC}[5]	Input common-mode voltage (AC coupling)		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the AMD Vivado™ Design Suite as outlined in the following table.

Table 28: **Speed Specification Version By Device**

2024.2.1	Device
1.10	XCSU10P, XCSU25P, XCSU35P

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

- **Advance Product Specification:** These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.
- **Preliminary Product Specification:** These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

- **Product Specification:** These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan UltraScale+ FPGAs.

Speed Grade Designations

Because individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 29 correlates the current status of the Spartan UltraScale+ FPGAs on a per speed grade basis.

Table 29: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCSU10P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU25P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU35P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU50P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU55P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU65P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		

Table 29: **Speed Grade Designations by Device** *(cont'd)*

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCSU100P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU150P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		
XCSU200P	-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V)[1] -1LI (V_{CCINT} = 0.72V)[1]		

Notes:

1. The lowest power -1L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV. Otherwise, the -1L devices, where V_{CCINT} = 0.85V, are listed in the Vivado Design Suite as -1L.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 30 lists the production released Spartan UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 30: **Spartan UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages			
	0.85V			0.72V
	-2	-1	-1L	-1L
XCSU10P				
XCSU25P				
XCSU35P				
XCSU50P				
XCSU55P				
XCSU65P				
XCSU100P				
XCSU150P				
XCSU200P				

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Spartan UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics section.

In each of the following LVDS performance tables, the I/O bank type is either high performance (HP), high density (HD), or XP5IO.

In LVDS component mode:

- For the input/output registers in HP I/O banks, the Vivado tools limit clock frequencies to 312.9 MHz for all speed grades.
- For IDDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.
- For ODDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.

Table 31: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
		0.85V				0.72V		
		-2		-1		-1		
		Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)[1]	HP	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)[1]	HP	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 32: **LVDS Native Mode Performance**

Description[1, 2]	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2[3]		-1[3]		-1[3]		
			Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	Mb/s
	8		375	1600	375	1600	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)[4]	4	HP	375	1600[5]	375	1600[5]	375	1260[5]	Mb/s
	8		375	1600[5]	375	1600[5]	375	1600[5]	Mb/s
LVDS RX SDR (RX_BITSLICE)[4]	4	HP	187.5	800	187.5	800	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. In the CMVA361, CMVA529, CMVB529, SBVC529, and SBVB625 packages, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.
5. Asynchronous receiver performance is limited to 1300 Mb/s for -2 speed grades and to 1250 Mb/s for -1 speed grades.

Table 33: **MIPI D-PHY Performance**

Description	I/O Bank Type	Packages	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
Maximum MIPI D-PHY transmitter or receiver data rate per lane[1]	XP5IO I/O	SBVF784 SBVG784 SBVA1024 FSVG1156	3200	3200	–	Mb/s
		CMVB529 SBVC529	2500	2500	–	Mb/s
	HP I/O	FSVG1156	2500	2500	2500	Mb/s
		SBVF784 SBVG784 SBVA1024	2500	2500	2500	Mb/s
		CMVA361 CMVA529 CMVB529 SBVC529 SBVB625	1500	1500	1500	Mb/s

Notes:

1. For applicable conditions, the lower maximum data rate applies.

Table 34: **LVDS Native-Mode 1000BASE-X Support**

Description[1]	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages		
		0.85V		0.72V
		-2	-1	-1
1000BASE-X	HP	Yes		

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

The following table provides the maximum data rates for applicable memory standards using the Spartan UltraScale+ FPGA memory PHY. Refer to Memory Solutions for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design User Guide* (UG583), electrical analysis, and characterization of the system.

Table 35: **Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller**

Memory Standard	I/O Bank Type	DRAM Type	Packages	Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
				-2	-1	-1	
LPDDR5/LPDDR5x	XP5IO	Single rank component	SBVF784 SBVG784 SBVA1024 FSVG1156	4267	3733		Mb/s
			CMVB529 SBVC529	2667	2667		Mb/s
LPDDR4X	XP5IO	Single rank component	FSVG1156	4267	3733		Mb/s
			SBVF784 SBVG784 SBVA1024	4267	3733		Mb/s
			CMVB529 SBVC529	2667	2667		Mb/s

Table 36: **Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller**

Memory Standard	I/O Bank Type	DRAM Type	Packages	Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
				-2	-1	-1	
DDR4	HP I/O	Single rank component	SBVF784 SBVG784 SBVA1024 FSVG1156	2400	2133	1866	Mb/s
			CMVA361 CMVA529 CMVB529 SBVC529 SBVB625	1866	1866	1866	Mb/s

FPGA Logic Switching Characteristics

Block RAM and FIFO Switching Characteristics

Table 37: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Maximum Frequency					
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes)				MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode)				MHz
F_{MAX_FIFO}	FIFO in all modes without ECC				MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE				MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode				MHz
T_{PW}[1]	Minimum pulse width				ps
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	1.02	1.103	1.529	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.281	0.299	0.433	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

Table 38: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Maximum Frequency					
F_{MAX}	UltraRAM maximum frequency with OREG_B = True	600	575	481	MHz
$F_{MAX\_ECC\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True	400	386	303	MHz
$F_{MAX\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False	500	478	389	MHz
T_{PW}[1]	Minimum pulse width	700	730	832	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required	1 clock cycle			

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 39: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
F_{REFCLK}	Reference clock frequency for IDELAYCTRL (component mode)	300 to 800			MHz
	Reference clock frequency when using BITSLICE_CONTROL with REFCLK (in native mode (for RX_BITSLICE only))	300 to 800			MHz
	Reference clock frequency for BITSLICE_CONTROL with PLL_CLK (in native mode)[1]	300 to 2666.67	300 to 2400	300 to 2133	MHz
T_{MINPER_CLK}	Minimum period for IODELAY clock	3.195	3.195	3.195	ns
T_{MINPER_RST}	Minimum reset pulse width	52.00			ns
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution	2.1 to 12			ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_F_{VCOMIN}/2.

DSP48 Slice Switching Characteristics

Table 40: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V[1]	
		-2	-1	-1	
Maximum Frequency					
F_{MAX}	With all registers used	775	645	600	MHz
F_{MAX_PATDET}	With pattern detector	687	571	524	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	544	456	413	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	492	410	371	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	565	468	423	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	410	338	304	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	379	314	280	MHz

Notes:

1. For devices operating at the lower power V_{CCINT} = 0.72V voltages, DSP cascades that cross the clock region center might operate below the specified F_{MAX}.

Clock Buffers and Networks

Table 41: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)					
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	775	667	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)					
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	775	667	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)					
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	775	667	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)					
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	775	667	667	MHz
GTH Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)					
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512	MHz

MMCM Switching Characteristics

Table 42: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
MMCM_F_{INMAX}	Maximum input clock frequency	933	800	800	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz	25–75			%
	Input duty cycle range: 50–199 MHz	30–70			%
	Input duty cycle range: 200–399 MHz	35–65			%
	Input duty cycle range: 400–499 MHz	40–60			%
	Input duty cycle range: >500 MHz	45–55			%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	500	450	450	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical[1]	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical[1]	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs[2]	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision[4]	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	775	667	667	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency[4, 5]	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	500	450	450	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	5 ns Max or one clock cycle			
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 43: **PLL Specification**

Symbol	Description[1]	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
PLL_F_{INMAX}	Maximum input clock frequency	933	800	800	MHz
PLL_F_{INMIN}	Minimum input clock frequency	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz	35–65			%
	Input duty cycle range: 400–499 MHz	40–60			%
	Input duty cycle range: >500 MHz	45–55			%
PLL_F_{VCOMIN}	Minimum PLLE4 VCO frequency[2]	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLLE4 VCO frequency[2]	1500	1500	1500	MHz
PLL_$F_{VCOHRMIN}$	Minimum PLLE4XP high range VCO frequency[3]	1075	1075	1075	MHz
PLL_$F_{VCOHRMAX}$	Maximum PLLE4XP high range VCO frequency[3]	1600	1600	1600	MHz
PLL_$F_{VCOLRMIN}$	Minimum PLLE4XP low range VCO frequency[3]	537.5	537.5	537.5	MHz
PLL_$F_{VCOLRMAX}$	Maximum PLLE4XP low range VCO frequency[3]	1075	1075	1075	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs[4]	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 5			
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision[6]	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100			µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B	775	667	667	MHz
	PLL maximum output frequency at CLKOUTPHY	2667	2400	2133	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B[7]	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1500, 1 x VCO mode: 750, 0.5 x VCO mode: 375			MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. PLLE4 has one VCO range.
3. PLLE4XP has two VCO ranges which are selected using the VCO_RANGE attribute. F_{VCOHR} should be used when VCO_RANGE = High and F_{VCOLR} should be used when VCO_RANGE = Low.
4. The static offset is measured between any PLL outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard.
6. Includes global clock buffer.
7. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 44: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew[1, 2]	XCSU10P	CMVA361	56	ps
			CMVA529	58	ps
			SBVB625	81	ps
		XCSU25P	CMVA361	56	ps
			CMVA529	58	ps
			SBVB625	81	ps
		XCSU35P	CMVA361	56	ps
			CMVA529	58	ps
			SBVB625	81	ps
		XCSU50P			
		XCSU55P			
		XCSU65P			
		XCSU100P			
		XCSU150P			
		XCSU200P			

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Spartan UltraScale+ FPGAs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

The following table summarizes the DC specifications of the GTH transceivers in Spartan UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further details.

Table 45: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV

Table 45: **GTH Transceiver DC Specifications** *(cont'd)*

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to `11111`	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based)		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages)		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceivers User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure 1: **Single-Ended Peak-to-Peak Voltage**

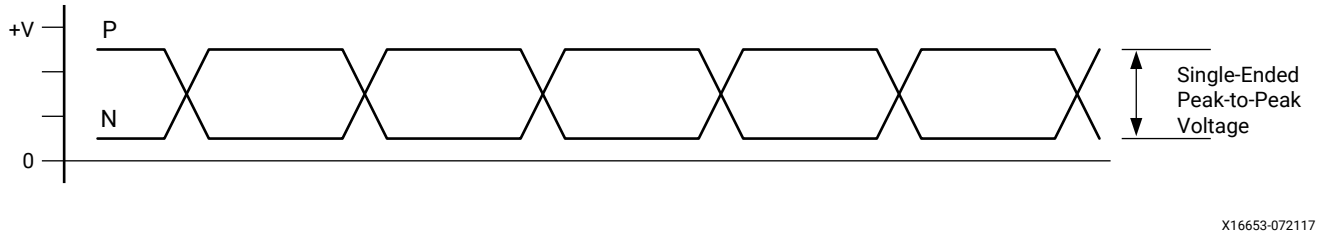

Figure 2: **Differential Peak-to-Peak Voltage**

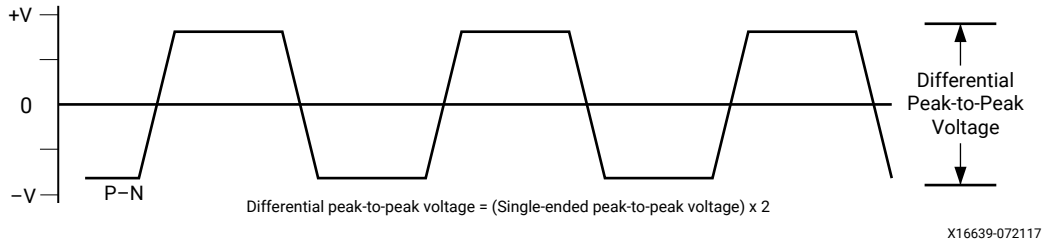

Table 46 and Table 47 summarize the DC specifications of the GTH transceivers input and output clocks in Spartan UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further details.

Table 46: **GTH Transceiver Clock Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 47: **GTH Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further information.

Table 48: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2		-1		-1		
F_{GTHMAX}	GTH maximum line rate		16.375[1]		12.5		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate		0.5		0.5		0.5		Gb/s
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTHCRANGE}$	CPLL line rate range[2]	1	4	12.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A						Gb/s
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTHQRANGE1}$	QPLL0 line rate range[3]	1	9.8	16.375	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.15	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.075	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0375	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0188	0.6125	1.0188	Gb/s
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTHQRANGE2}$	QPLL1 line rate range[4]	1	8.0	13.0	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s

Table 48: **GTH Transceiver Performance** *(cont'd)*

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2		-1		-1		
			Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2	6.25	2	4.25	2	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8	13	8	13	8	13	GHz

Notes:

1. GTH transceivers in the CMVA361, CMVA529, and CMVB529 packages support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 × CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 49: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	250	MHz

Table 50: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Table 51: **GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$[1, 2]	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$[1, 2]	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 × Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 52: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3×10^6	UI

Table 53: **GTH Transceiver User Clock Switching Characteristics**

Symbol	Description[1]	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2[2]	-1[3, 4]	-1[4]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	390.625	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	390.625	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[5] maximum frequency	16	16, 32	511.719	390.625	322.266	MHz
		32	32, 64	511.719	390.625	322.266	MHz
		20	20, 40	409.375	312.500	257.813	MHz
		40	40, 80	409.375	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[5] maximum frequency	16	16, 32	511.719	390.625	322.266	MHz
		32	32, 64	511.719	390.625	322.266	MHz
		20	20, 40	409.375	312.500	257.813	MHz
		40	40, 80	409.375	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[5] maximum frequency	16	16	511.719	390.625	322.266	MHz
		16	32	255.859	195.313	161.133	MHz
		32	32	511.719	390.625	322.266	MHz
		32	64	255.859	195.313	161.133	MHz
		20	20	409.375	312.500	257.813	MHz
		20	40	204.688	156.250	128.906	MHz
		40	40	409.375	312.500	257.813	MHz
		40	80	204.688	156.250	128.906	MHz

Table 53: **GTH Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2[2]	-1[3, 4]	-1[4]	
F_{RXIN2}	RXUSRCLK2[5] maximum frequency	16	16	511.719	390.625	322.266	MHz
		16	32	255.859	195.313	161.133	MHz
		32	32	511.719	390.625	322.266	MHz
		32	64	255.859	195.313	161.133	MHz
		20	20	409.375	312.500	257.813	MHz
		20	40	204.688	156.250	128.906	MHz
		40	40	409.375	312.500	257.813	MHz
		40	80	204.688	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceivers User Guide* (UG576).
2. For speed grades -2E and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grades -1E, -1I, and -1Q, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
4. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
5. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *UltraScale Architecture GTH Transceivers User Guide* (UG576).

Table 54: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500.00	ps
$T_{J16.375}$	Total jitter[2, 4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J15.0}$	Total jitter[2, 4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter[2, 4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter[2, 4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter[3, 4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter[2, 4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI

Table 54: **GTH Transceiver Transmitter Switching Characteristics** *(cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J10.3125\_QPLL}$	Total jitter[2, 4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter[3, 4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter[2, 4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter[3, 4]	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter[3, 4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter[3, 4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter[3, 4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter[3, 4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J4.0}$	Total jitter[3, 4]	4.0 Gb/s	–	–	0.32	UI
$D_{J4.0}$	Deterministic jitter[3, 4]		–	–	0.16	UI
$T_{J3.20}$	Total jitter[3, 4]	3.20 Gb/s[5]	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter[3, 4]	2.5 Gb/s[6]	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J1.25}$	Total jitter[3, 4]	1.25 Gb/s[7]	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter[3, 4]		–	–	0.06	UI
T_{J500}	Total jitter[3, 4]	500 Mb/s[8]	–	–	0.10	UI
D_{J500}	Deterministic jitter[3, 4]		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 55: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHRX}	Serial data rate		0.500	–	F_{GTHMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking[1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI

Table 55: **GTH Transceiver Receiver Switching Characteristics** *(cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance[2]						
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)[3]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)[3]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)[3]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)[3]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)[3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)[3]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (QPLL)[3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL)[3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)[3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)[3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)[3]	3.2 Gb/s[4]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)[3]	2.5 Gb/s[5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)[3]	1.25 Gb/s[6]	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)[3]	500 Mb/s[7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye[2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye[8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye[8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceivers User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 56: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR[1]	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3, 4	PCI Express base 4.0	2.5, 5.0, 8.0, and 16.0	Compliant
SDI[2]	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI[2]	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI[2]	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort[2]	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express® designs can be found at PCI Express. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many PCIE4CE blocks are in each Spartan UltraScale+ FPGA. For supported modes, link widths, and link speeds, see the *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

Table 57: **Maximum Performance for PCIE4CE-based PCI Express Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency	125.00	125.00	125.00	MHz

System Monitor Specifications

Table 58: **System Monitor Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy[1]						
Resolution			10	–	–	Bits
Integral nonlinearity[2]	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity[2]	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs[2]						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V

Table 58: **System Monitor Specifications** *(cont'd)*

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-Chip Sensor Accuracy						
Temperature sensor error[1, 3]		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C
Supply sensor error[4]		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate[5]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference[6]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the Analog Input section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

SYSMON I2C/PMBus Interfaces

Table 59: **SYSMON I2C Fast Mode Interface Switching Characteristics**

Symbol	Description[1]	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	µs
T_{SMFCKH}	SCL High time	0.6	–	µs
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 60: **SYSMON I2C Standard Mode Interface Switching Characteristics**

Symbol	Description[1]	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	µs
T_{SMSCKH}	SCL High time	4.0	–	µs
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Configuration Switching Characteristics

Table 61: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Power-up Timing Characteristics					
T_{PL}	Program latency time from PROGRAM_B Low to output High-Z	10	10	10	ms, Max
T_{POR}[1, 2]	Power-on reset time from start of power-up ramp to INIT_B High-Z (40 ms maximum ramp rate)	65	65	65	ms, Max
		0	0	0	ms, Min
	Power-on reset time from start of power-up ramp to INIT_B High-Z with POR override (2 ms maximum ramp rate)	15	15	15	ms, Max
		5	5	5	ms, Min
$T_{PROGRAM}$	PROGRAM_B Low pulse width	250	250	250	ns, Min
OSC Core and IRO Clock Switching					
$F_{OSC\_CORE\_CLK}$	Internal clock source core configuration frequency	510	510	510	MHz, Typ
	Internal clock source core configuration tolerance	±15	±15	±15	%
$F_{CCU\_IRO\_CLK}$	Internal configuration control unit clock frequency	170	170	170	MHz, Max
$F_{PMC\_IRO\_CLK}$	Internal PMC control clock frequency	255	255	255	MHz, Max
AXI32 Clock Switching					
F_{AXI_CLK}	PL AXI32 clock (AXICLK) to PMC	200	200	200	MHz, Max
CCLK Output (Master Configuration Modes)					
T_{MCCKDC}	Master CCLK clock duty cycle	45/55	45/55	45/55	%, Min/Max
F_{MCCK}	Master SPI (x1/x2/x4) CCLK frequency	150	150	125	MHz, Max
	Master OSPI (x8) CCLK frequency	150	150	125	
F_{MCCK_START}	Master CCLK frequency at start of configuration	21	21	21	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±15	±15	±15	%, Max
CCLK Input (Slave Configuration Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave serial CCLK frequency	125	125	125	MHz, Max
	Slave SelectMAP CCLK frequency	125	125	125	
EMCCLK Input (Master Configuration Modes)					
$T_{EMCCKDC}$	External master CCLK duty cycle	45/55	45/55	45/55	ns, Min
F_{EMCCK}	External master configuration clock (EMCCLK) frequency with master SPI (x1/x2/x4)	150	150	125	MHz, Max
	External master configuration clock (EMCCLK) frequency with master OSPI (x1/x8)	150	150	125	
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE3)	200	200	150	MHz, Max

Table 61: **Configuration Switching Characteristics** *(cont'd)*

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Slave Serial Mode Programming Switching					
T_{DCCK}/T_{CCKD}	D_{IN} setup/hold from CCLK rising edge	3.0/0	3.0/0	4.0/0	ns, Min
T_{CCO}	CCLK falling edge to D_{OUT}	8.0	8.0	8.0	ns, Max
$T_{SCSCLK/SCLKCS}$	Serial chip select (CS_B) setup and hold to CCLK rising edge				ns, Min
$C_{READYCS}$	READY deassertion to chip select deassertion	24	24	24	clock cycles, Max
Slave SelectMAP Mode Programming Switching					
$T_{SMAPDCLK/SMAPCLKD}$	SelectMAP data (D[31:00]) setup and hold to CCLK rising edge	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
$T_{SMAPCSCLK/SMAPCLKCS}$	SelectMAP chip select (CSI_B) setup and hold to CCLK rising edge	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
$T_{SMAPRWCLK/SMAPCLKRW}$	SelectMAP read write (RDWR_B) setup and hold to CCLK rising edge	9.0/0.0	9.0/0.0	10.0/0.0	ns, Min
$T_{SMAPCLKO}$	SelectMAP CCLK rising edge to data output	8	8	8	ns, Max
$C_{SMAPBUSYCS}$	SelectMAP BUSY assertion to CSI_B deassertion	24	24	24	clock cycles, Max
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold to/from TCK rising edge	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7	7	8	ns, Max
F_{TCK}	TCK frequency	66	66	50	MHz, Max
eFUSE Clock Switching					
F_{FUSE_CLK}	Internal eFUSE clock for programming source from FUSE_CLK or EMCCLK	25/200	25/200	25/200	MHz, Min/Max
DNA_PORTE2 Switching					
F_{DNACK}	DNA_PORTE2 CLK frequency	200	200	175	MHz, Max
STARTUPE3 Ports					
$T_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay	0.25/6.50	0.25/7.50	0.25/9.00	ns, Min/Max
T_{DO}	DO[3:0] ports to D03-D00 pins output delay	0.25/7.70	0.25/8.40	0.25/10.00	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays	0.25/7.70	0.25/8.40	0.25/10.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay	0.25/7.50	0.25/8.40	0.25/9.80	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay	0.25/7.50	0.25/8.40	0.25/9.80	ns, Min/Max
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay	0.25/9.40	0.25/10.50	0.25/12.10	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay	0.25/9.40	0.25/10.50	0.25/12.10	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay	0.5/3.1	0.5/3.5	0.5/4.0	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency	50	50	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance	±15	±15	±15	%, Max

Table 61: **Configuration Switching Characteristics** *(cont'd)*

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
T_{DCI_MATCH}	Specifies a stall in the start-up cycle until the digitally controlled impedance (DCI) match signals are asserted	4	4	4	ms, Max

Notes:

1. The T_{POR} specification begins when the last of the monitored supplies (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO_0}) reaches 95% of its recommended operating condition voltage.
2. The T_{POR} time is determined by the POR_OVERRIDE input pin which must be tied to V_{CCINT} or GND. The POR_OVERRIDE pin can be tied to V_{CCINT} for POR override only when the monitored supplies ramp within the specified 2 ms maximum ramp rate. Otherwise, POR_OVERRIDE must be tied to GND.

Table 62: **Master SPI Mode Programming Switching**

Symbol	Description[1, 2]	Min	Max	Units
SPI clock frequency operating at ≥ 51 MHz				
F_{QSPI_CLK}	SPI clock frequency	51	150	MHz
T_{SPIIVW}	Input valid data window			UI
$T_{QSPICKO}$	Clock to output delay, all outputs			ns
$T_{QSPICSCLK}$	Chip select asserted to next clock edge			ns
$T_{QSPICLKCS}$	Clock edge to chip select deasserted			ns
SPI clock frequency operating at < 51 MHz				
F_{QSPI_CLK}	SPI clock frequency		50	MHz
$T_{QSPIDCK}$	Setup time, all inputs			ns
$T_{QSPICKD}$	Hold time, all inputs			ns
$T_{QSPICKO}$	Clock to output delay, all outputs			ns
$T_{QSPICSCLK}$	Chip select asserted to next clock edge			ns
$T_{QSPICLKCS}$	Clock edge to chip select deasserted			ns

Notes:

1. The test conditions are configured for the Master SPI configuration mode 4-bit interface with a 12 mA drive strength, fast slew rate, and load conditions (15 pF/30 pF for an SPI 4-bit interface clock frequency up to 100 MHz and 15 pF for clock frequency >100 MHz), tested at 1.8V.
2. 30 pF loads are for QSPI dual-stacked.

Table 63: **Master Octal-SPI Mode Programming Switching**

Symbol	Description[1]	Min	Max	Units
Octal-SPI clock frequency operating at DDR > 51 MHz				
F_{OSPI_CLK}	Octal-SPI clock frequency	51	150	MHz
$T_{OSPIIVW}$	Input valid data window			UI
$T_{OSPICKO}$	Clock edge to OSPID[07:00] and FCS_B outputs			ns
$T_{OSPICSCLK}$	Chip select asserted to next clock edge			ns
$T_{OSPICLKCS}$	CCLK edge to chip select deasserted			ns
Octal-SPI clock frequency operating at SDR > 51 MHz				
F_{OSPI_CLK}	Octal-SPI clock frequency	51	150	MHz

Table 63: **Master Octal-SPI Mode Programming Switching** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
$T_{OSPIIVW}$	Input valid data window			UI
$T_{OSPICKO}$	Clock edge to OSPID[07:00] and FCS_B outputs			ns
$T_{OSPICSCLK}$	Chip select asserted to next clock edge			ns
$T_{OSPICLKCS}$	Clock edge to chip select deasserted			ns
Octal-SPI clock frequency operating at SDR < 51 MHz				
F_{OSPI_CLK}	Octal-SPI clock frequency		50	MHz
$T_{OSPIDCK}$	Setup time, all data inputs			ns
$T_{OSPICKD}$	Hold time, all data inputs			ns
$T_{OSPICKO}$	Clock edge to OSPID[07:00] and FCS_B outputs			ns
$T_{OSPICSCLK}$	Chip select asserted to next clock edge			ns
$T_{OSPICLKCS}$	Clock edge to chip select deasserted			ns

Notes:

1. The test conditions are configured for the Octal-SPI interface with a 12 mA drive strength, fast slew rate, and 12 pF load. The maximum Octal-SPI device clock frequency under different load conditions are 150 MHz for a 20 pF load and 100 MHz for a 40 pF load.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
01/24/2025 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright