



PDTD113ET-Q

50 V, 500 mA NPN resistor-equipped transistor;
R1 = 1 k Ω , R2 = 1 k Ω

26 March 2025

Product data sheet

1. General description

500 mA NPN Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Built-in bias resistors
- Reduces component count
- Simplifies circuit design
- Reduces pick and place costs
- 500 mA output current capability
- 10 % resistor ratio tolerance
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital application in automotive and industrial segments
- Controlling IC inputs
- Cost saving alternative for BC817 series in digital applications
- Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	500	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	0.7	1	1.3	k Ω
R2/R1	bias resistor ratio		0.9	1	1.1	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SOT23	 sym007
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTD113ET-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTD113ET-Q	%7R

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage			-10	10	V
I _O	output current			-	500	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

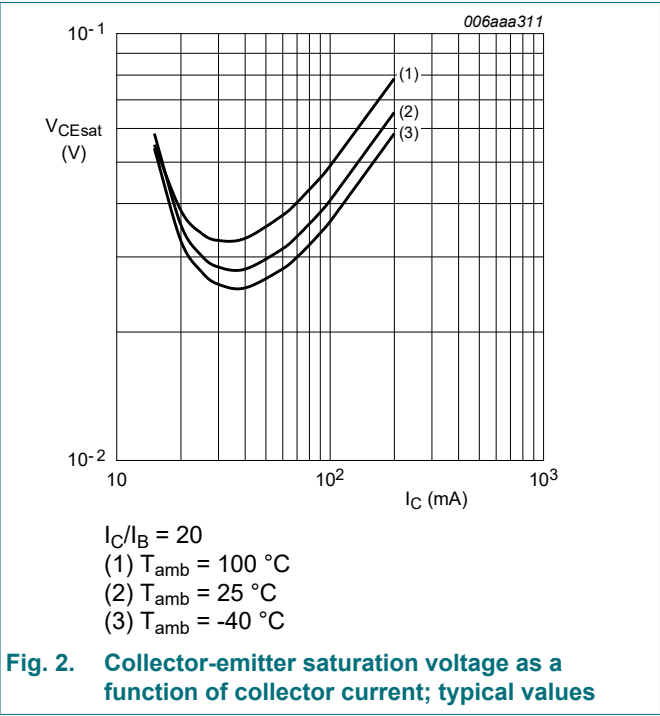
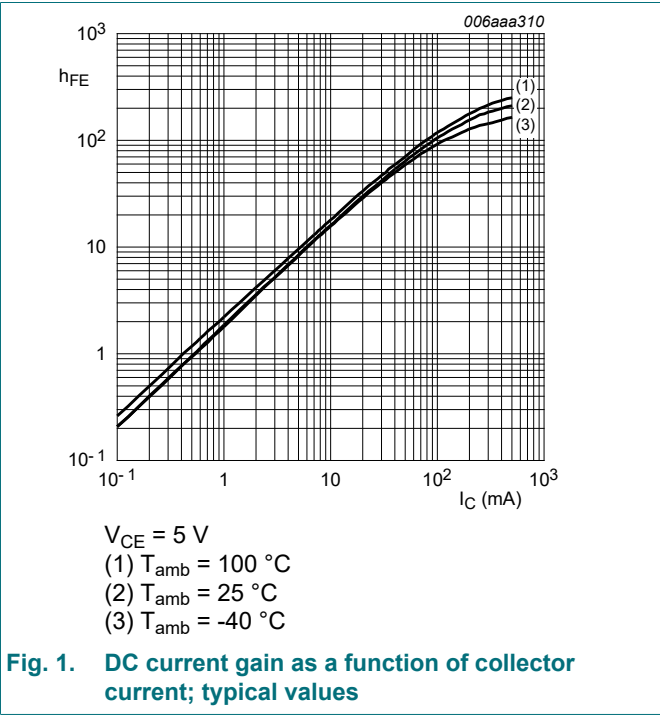
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	$V_{CB} = 40\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
		$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 50\text{ V}; I_B = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	0.5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	4	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 50\text{ mA}; T_{amb} = 25\text{ °C}$	33	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50\text{ mA}; I_B = 2.5\text{ mA}; T_{amb} = 25\text{ °C}$	-	-	0.3	V
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ μA}; T_{amb} = 25\text{ °C}$	0.6	1.1	1.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 20\text{ mA}; T_{amb} = 25\text{ °C}$	1	1.4	1.8	V
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ °C}$	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.9	1	1.1	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}$	-	7	-	pF



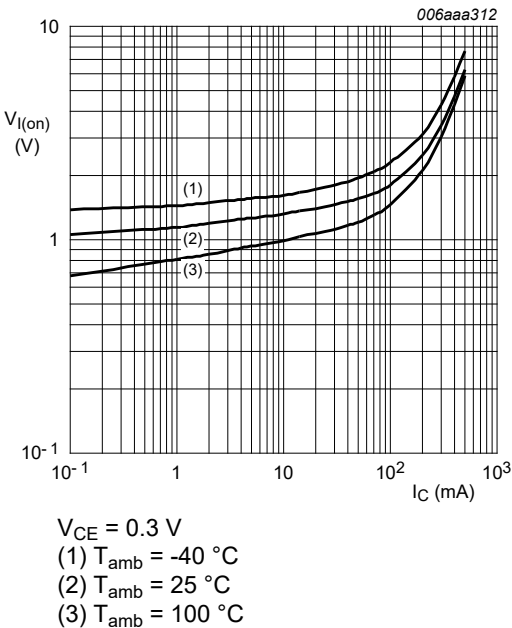


Fig. 3. On-state input voltage as a function of collector current; typical values

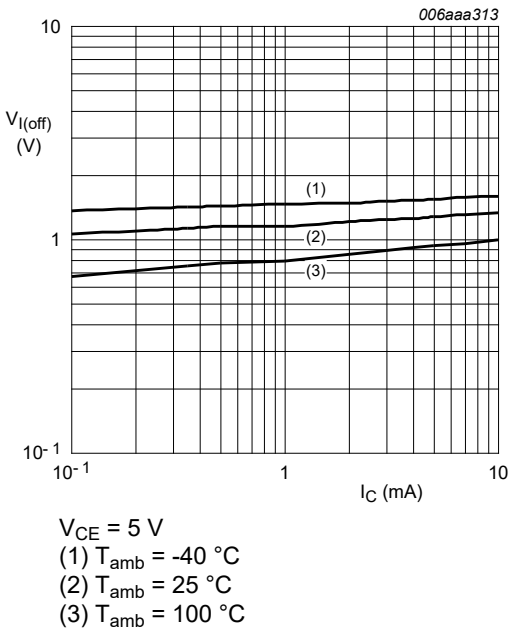


Fig. 4. Off-state input voltage as a function of collector current; typical values

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

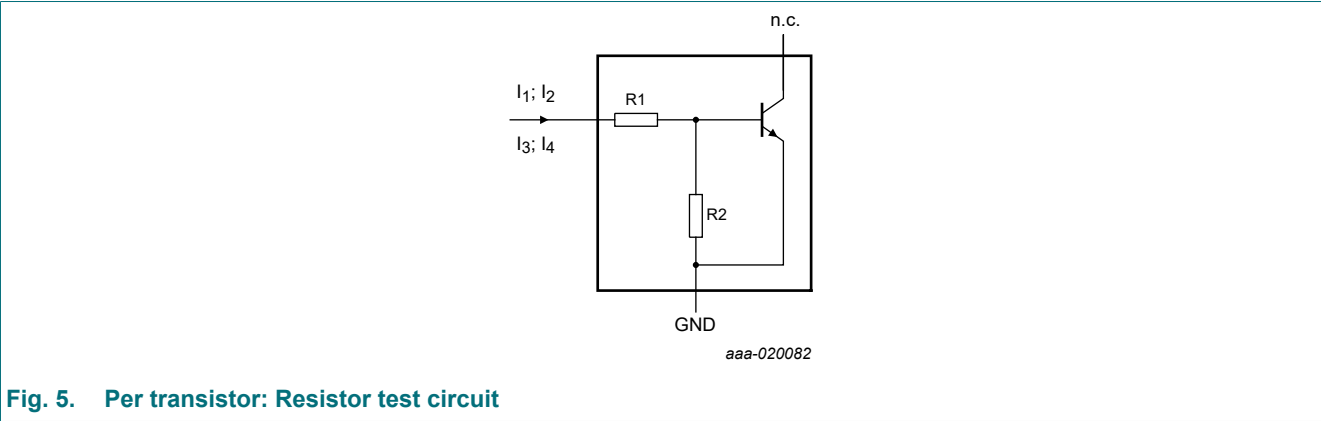
Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

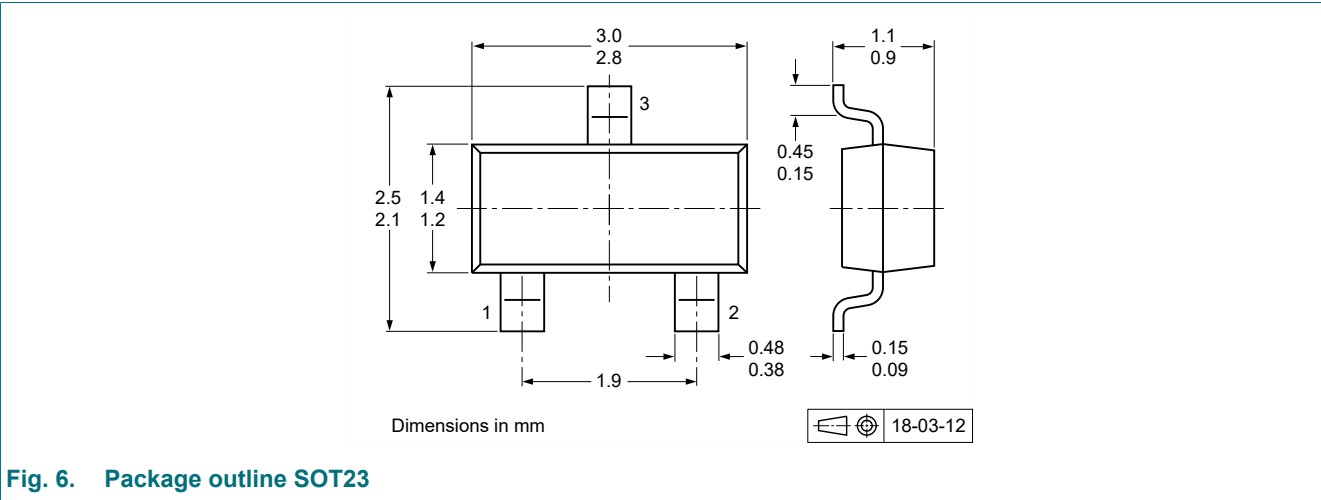


Resistor test conditions

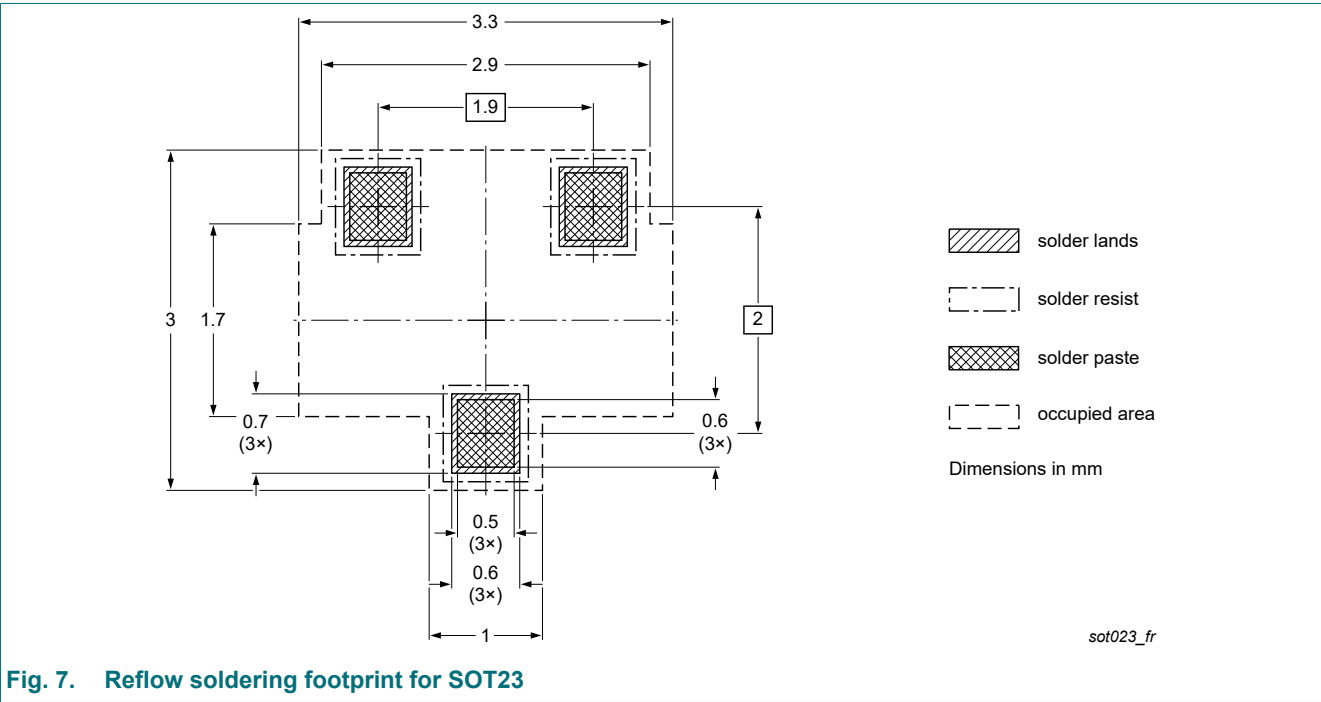
Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PDTD113ET-Q	1	1	1.5 mA	1.9 mA	-2.0 mA	-2.4 mA

12. Package outline



13. Soldering



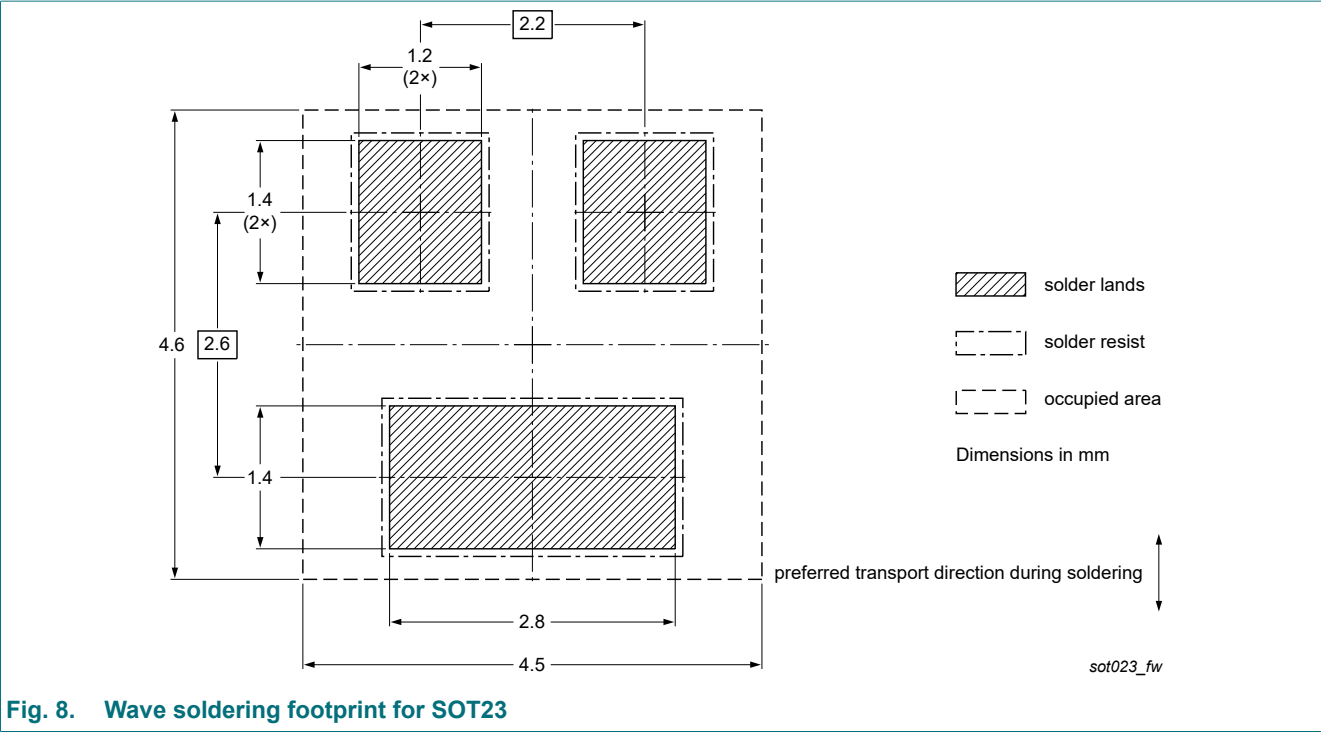


Fig. 8. Wave soldering footprint for SOT23

50 V, 500 mA NPN resistor-equipped transistor; R1 = 1 kΩ, R2 = 1 kΩ

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTD113ET-Q v.1	20250326	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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