



# PDTC143ZT-Q

50 V, 100 mA NPN resistor-equipped transistor;  
R1 = 4.7 k $\Omega$ , R2 = 47 k $\Omega$

10 October 2024

Product data sheet

## 1. General description

NPN Resistor-Equipped Transistor (RET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA143ZT-Q

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

## 4. Quick reference data

Table 1. Quick reference data

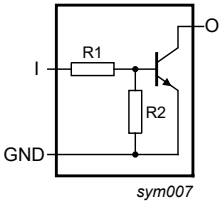
| Symbol           | Parameter                 | Conditions |     | Min | Typ | Max | Unit       |
|------------------|---------------------------|------------|-----|-----|-----|-----|------------|
| V <sub>CEO</sub> | collector-emitter voltage | open base  |     | -   | -   | 50  | V          |
| I <sub>O</sub>   | output current            |            |     | -   | -   | 100 | mA         |
| R1               | bias resistor 1 (input)   |            | [1] | 3.3 | 4.7 | 6.1 | k $\Omega$ |
| R2/R1            | bias resistor ratio       |            | [1] | 8   | 10  | 12  |            |

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN resistor-equipped transistor; R1 = 4.7 kΩ, R2 = 47 kΩ

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description        | Simplified outline                                                                         | Graphic symbol                                                                                |
|-----|--------|--------------------|--------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| 1   | I      | input (base)       | <br>SOT23 | <br>sym007 |
| 2   | GND    | ground (emitter)   |                                                                                            |                                                                                               |
| 3   | O      | output (collector) |                                                                                            |                                                                                               |

6. Ordering information

Table 3. Ordering information

| Type number                 | Package |                                                                                          |                       |
|-----------------------------|---------|------------------------------------------------------------------------------------------|-----------------------|
|                             | Name    | Description                                                                              | Version               |
| <a href="#">PDTC143ZT-Q</a> | SOT23   | plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body | <a href="#">SOT23</a> |

7. Marking

Table 4. Marking codes

| Type number | Marking code[1] |
|-------------|-----------------|
| PDTC143ZT-Q | %18             |

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol           | Parameter                 | Conditions               |     | Min | Max | Unit |
|------------------|---------------------------|--------------------------|-----|-----|-----|------|
| V <sub>CBO</sub> | collector-base voltage    | open emitter             |     | -   | 50  | V    |
| V <sub>CEO</sub> | collector-emitter voltage | open base                |     | -   | 50  | V    |
| V <sub>EBO</sub> | emitter-base voltage      | open collector           |     | -   | 5   | V    |
| V <sub>I</sub>   | input voltage             |                          |     | -5  | 30  | V    |
| I <sub>O</sub>   | output current            |                          |     | -   | 100 | mA   |
| P <sub>tot</sub> | total power dissipation   | T <sub>amb</sub> ≤ 25 °C | [1] | -   | 250 | mW   |
| T <sub>j</sub>   | junction temperature      |                          |     | -   | 150 | °C   |
| T <sub>amb</sub> | ambient temperature       |                          |     | -65 | 150 | °C   |
| T <sub>stg</sub> | storage temperature       |                          |     | -65 | 150 | °C   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

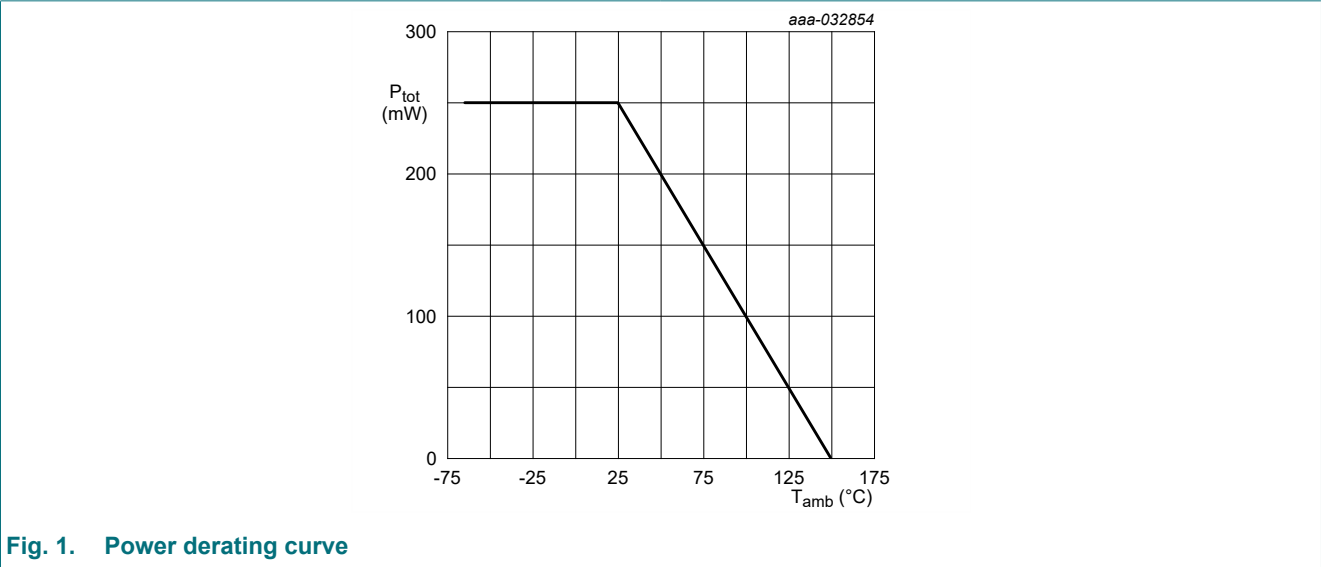


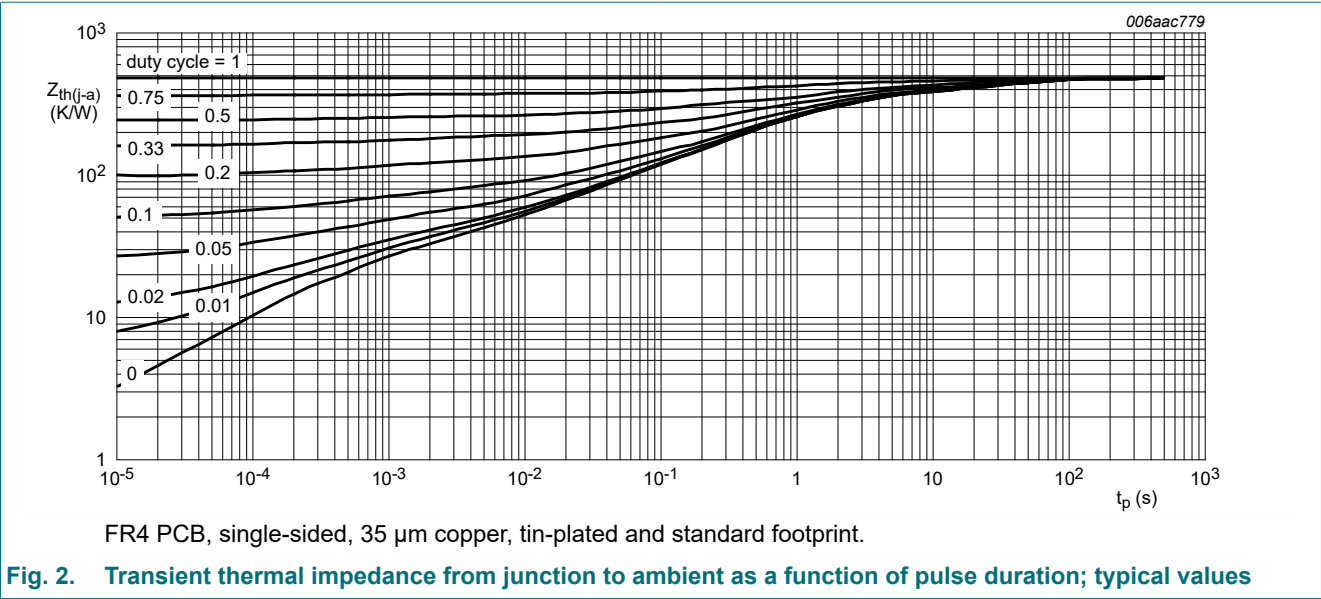
Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol        | Parameter                                   | Conditions  |     | Min | Typ | Max | Unit |
|---------------|---------------------------------------------|-------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | -   | -   | 500 | K/W  |

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

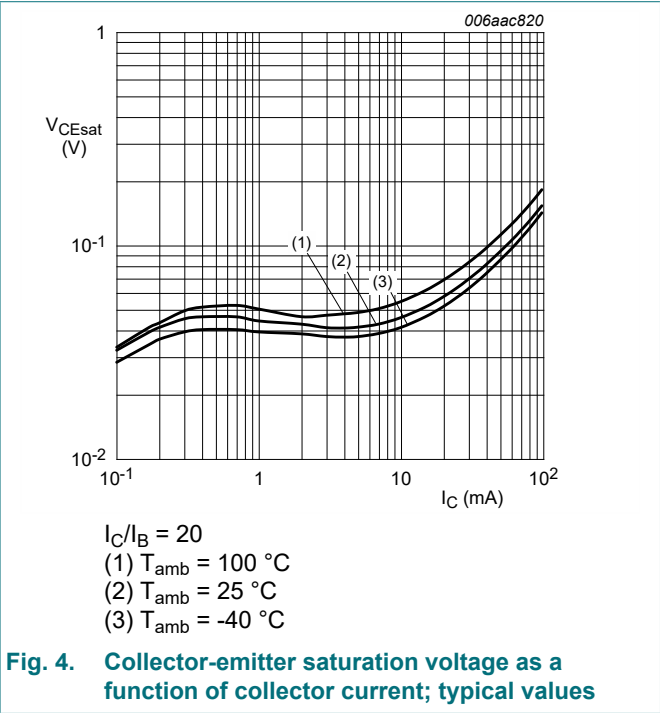
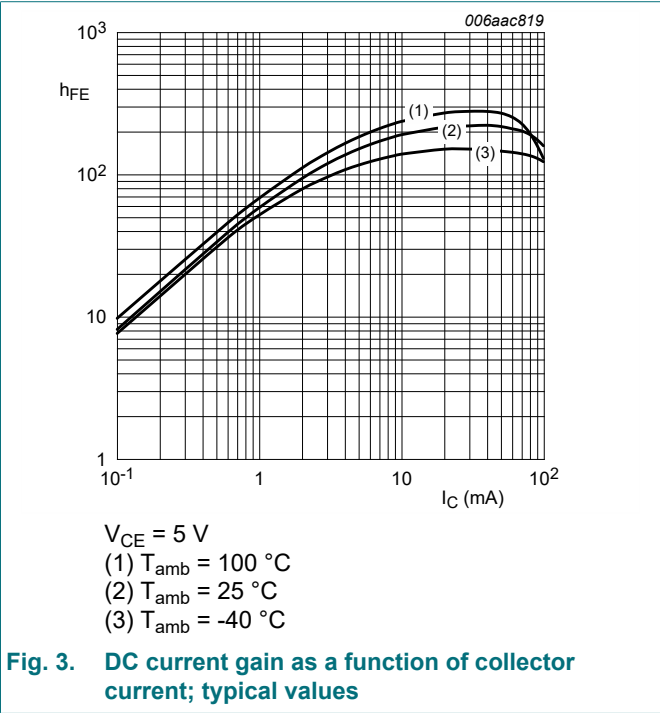


10. Characteristics

Table 7. Characteristics

| Symbol        | Parameter                            | Conditions                                                                                                                     | Min | Typ | Max | Unit          |
|---------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $V_{(BR)CBO}$ | collector-base breakdown voltage     | $I_C = 100\text{ }\mu\text{A}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                   | 50  | -   | -   | V             |
| $V_{(BR)CEO}$ | collector-emitter breakdown voltage  | $I_C = 2\text{ mA}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                              | 50  | -   | -   | V             |
| $I_{CBO}$     | collector-base cut-off current       | $V_{CB} = 50\text{ V}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                           | -   | -   | 100 | nA            |
| $I_{CEO}$     | collector-emitter cut-off current    | $V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                           | -   | -   | 100 | nA            |
|               |                                      | $V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_j = 150\text{ }^{\circ}\text{C}$                                              | -   | -   | 5   | $\mu\text{A}$ |
| $I_{EBO}$     | emitter-base cut-off current         | $V_{EB} = 5\text{ V}$ ; $I_C = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                            | -   | -   | 170 | $\mu\text{A}$ |
| $h_{FE}$      | DC current gain                      | $V_{CE} = 5\text{ V}$ ; $I_C = 10\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                          | 100 | -   | -   |               |
| $V_{CEsat}$   | collector-emitter saturation voltage | $I_C = 5\text{ mA}$ ; $I_B = 0.25\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                          | -   | -   | 100 | mV            |
| $V_{I(off)}$  | off-state input voltage              | $V_{CE} = 5\text{ V}$ ; $I_C = 100\text{ }\mu\text{A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                | -   | 0.6 | 0.5 | V             |
| $V_{I(on)}$   | on-state input voltage               | $V_{CE} = 0.3\text{ V}$ ; $I_C = 5\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                                         | 1.3 | 0.9 | -   | V             |
| R1            | bias resistor 1 (input)              |                                                                                                                                | [1] | 3.3 | 4.7 | 6.1 kΩ        |
| R2/R1         | bias resistor ratio                  |                                                                                                                                | [1] | 8   | 10  | 12            |
| $C_c$         | collector capacitance                | $V_{CB} = 10\text{ V}$ ; $I_E = 0\text{ A}$ ; $i_e = 0\text{ A}$ ; $f = 1\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$ | -   | -   | 2.5 | pF            |
| $f_T$         | transition frequency                 | $V_{CE} = 5\text{ V}$ ; $I_C = 10\text{ mA}$ ; $f = 100\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                   | [2] | -   | 230 | MHz           |

[1] See "Section 11: Test information" for resistor calculation and test conditions.  
[2] Characteristics of built-in transistor.



50 V, 100 mA NPN resistor-equipped transistor; R1 = 4.7 kΩ, R2 = 47 kΩ

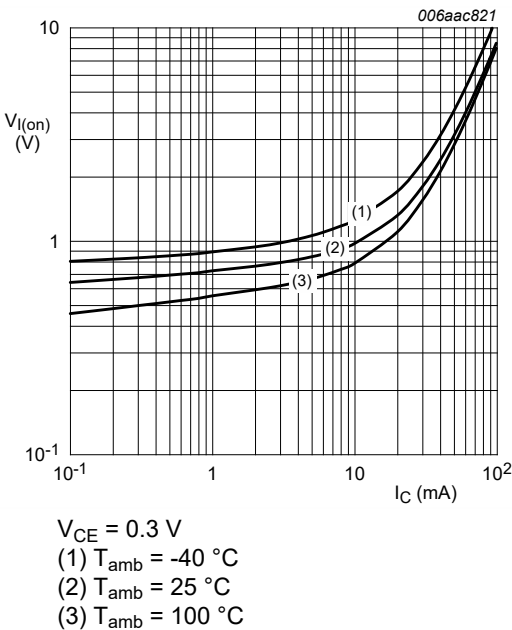


Fig. 5. On-state input voltage as a function of collector current; typical values

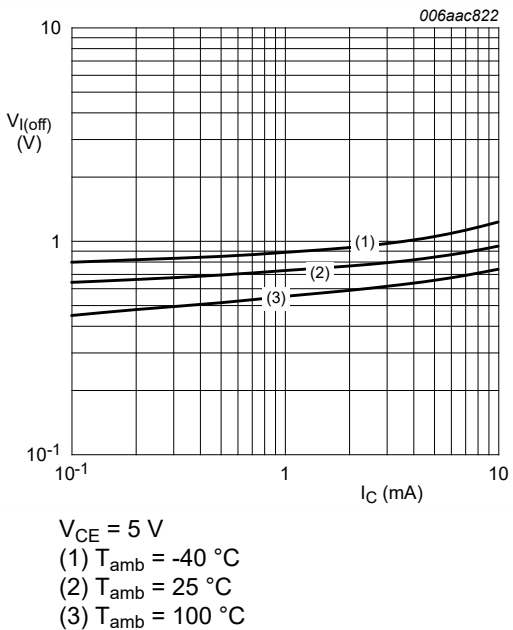


Fig. 6. Off-state input voltage as a function of collector current; typical values

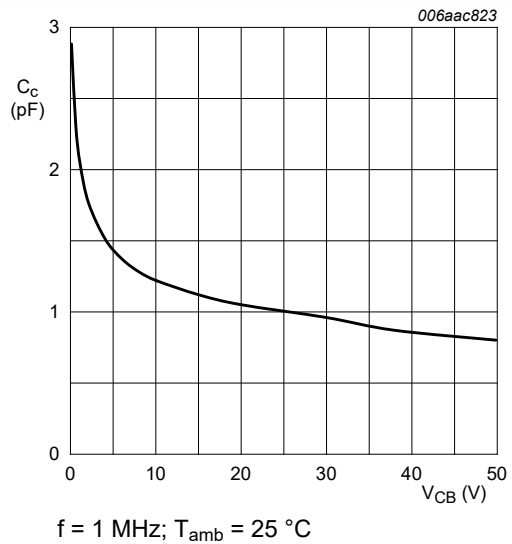


Fig. 7. Collector capacitance as a function of collector-base voltage; typical values

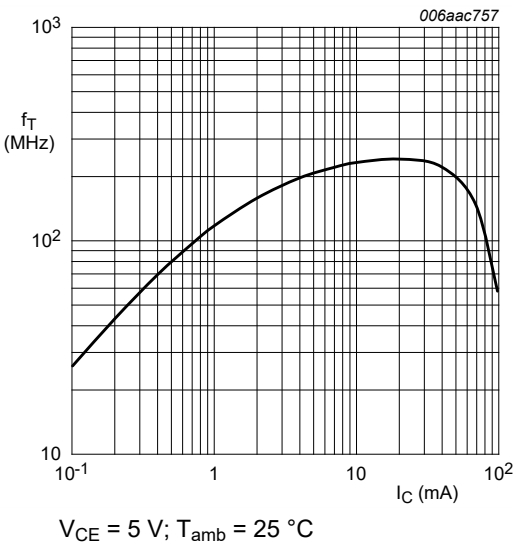


Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

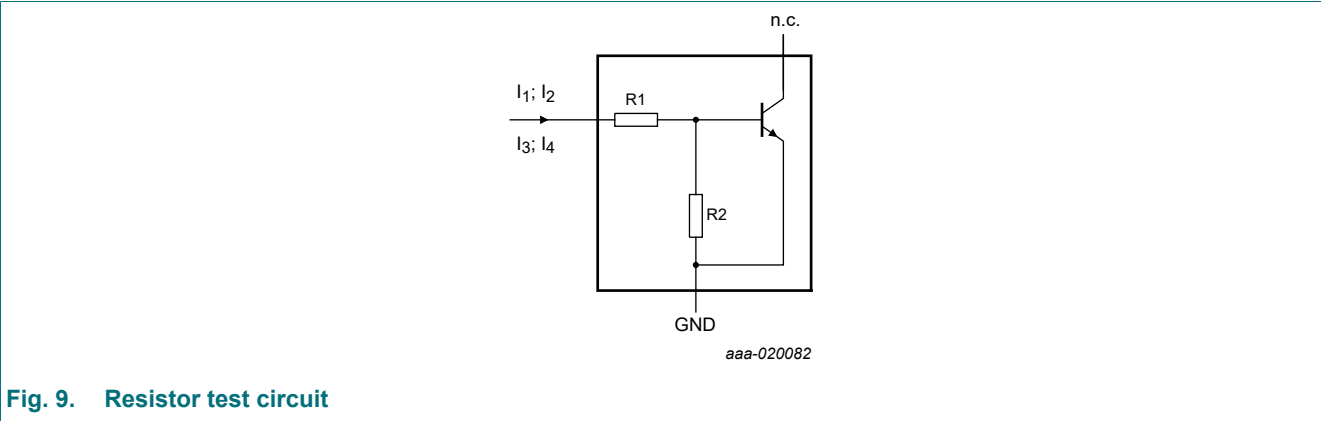


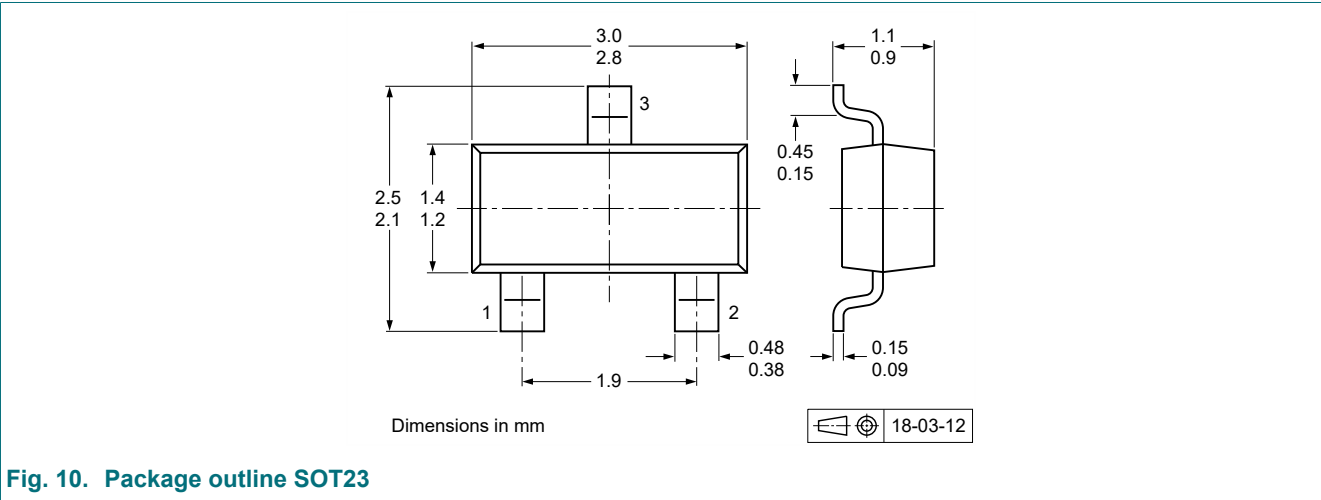
Fig. 9. Resistor test circuit

Resistor test conditions

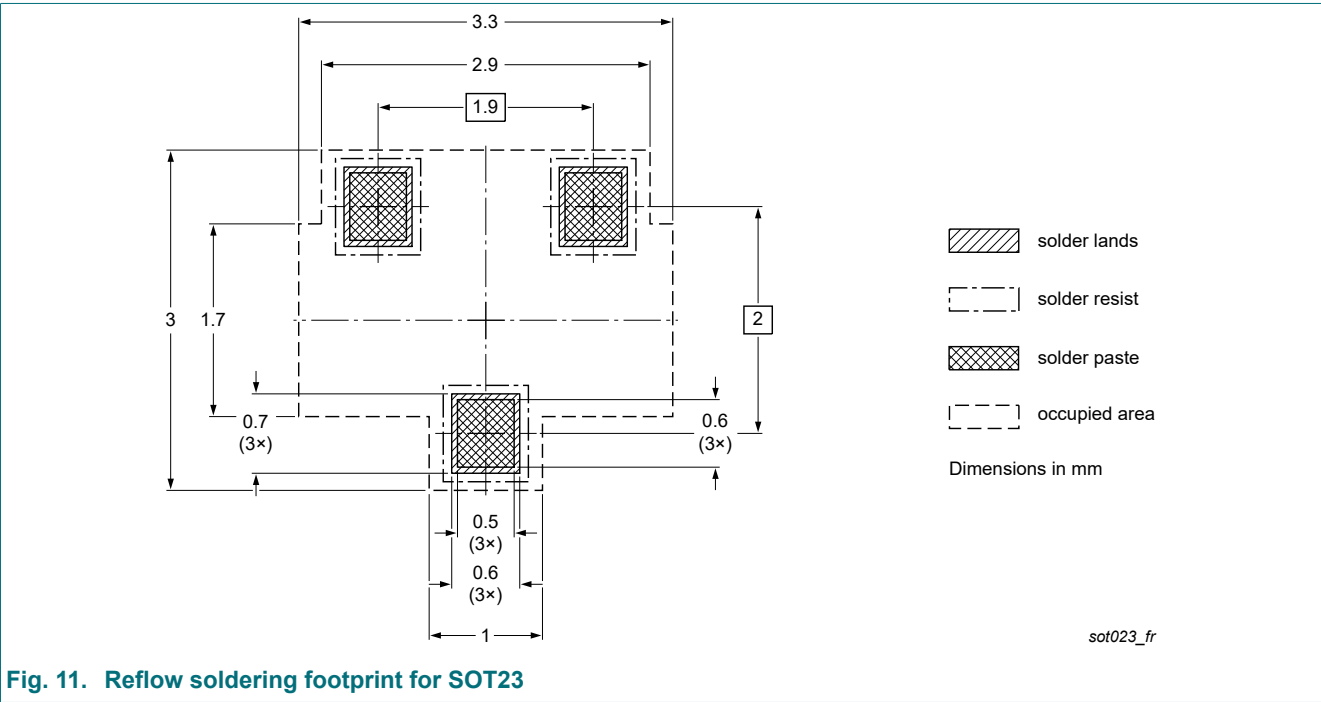
Table 8. Resistor test conditions

| Type number | R1 (kΩ) | R2 (kΩ) | Test conditions |                |                |                |
|-------------|---------|---------|-----------------|----------------|----------------|----------------|
|             |         |         | I <sub>1</sub>  | I <sub>2</sub> | I <sub>3</sub> | I <sub>4</sub> |
| PDTC143ZT-Q | 4.7     | 47      | 90 μA           | 140 μA         | -55 μA         | -105 μA        |

12. Package outline



13. Soldering



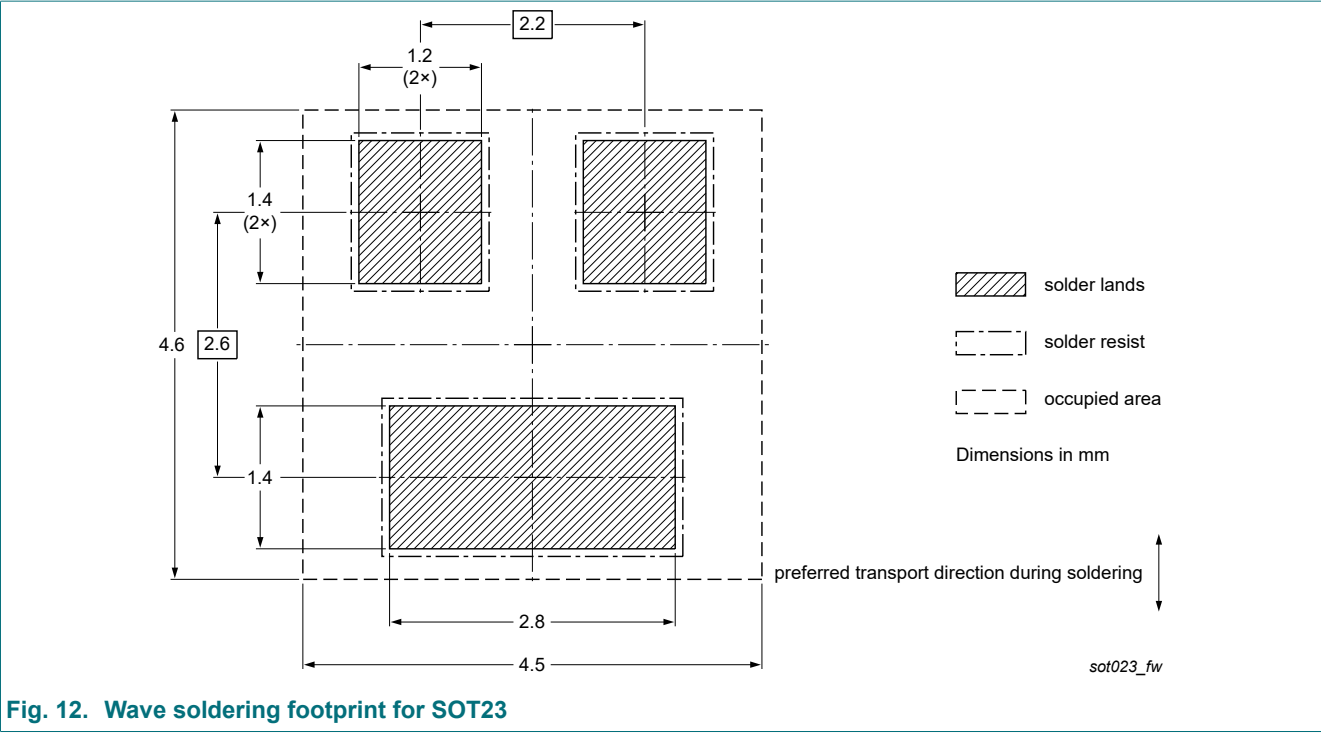


Fig. 12. Wave soldering footprint for SOT23

50 V, 100 mA NPN resistor-equipped transistor; R1 = 4.7 kΩ, R2 = 47 kΩ

14. Revision history

Table 9. Revision history

| Data sheet ID   | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PDTC143ZT-Q v.1 | 20241010     | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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