



# BUK9K61-100L

Dual N-channel 100 V, 61 mOhm logic level MOSFET in LFAK56D

20 January 2025

Product data sheet

## 1. General description

Dual N-channel logic level MOSFET in an LFAK56D (Dual Power-SO8) package. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET – two silicon dies in one LFAK56D package for significant space saving
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automatic optical inspection

## 3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting, and solenoid control
- Transmission control
- LED lighting
- Circuit protection

## 4. Quick reference data

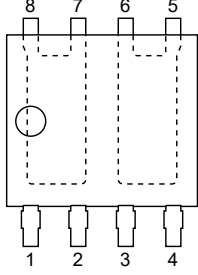
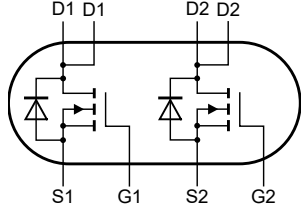
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Limiting values FET1 and FET2</b>						
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	15	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	32	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	33	44.6	60.1	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 5\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	0.2	1.9	4.2	nC

[1] 15 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p><b>LFAK56D; Dual LFAK (SOT1205)</b></p>	 <p><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9K61-100L	LFAK56D; Dual LFAK	plastic, single ended surface mounted package (LFAK56D); 8 leads	SOT1205

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK9K61-100L	9611HL

## 8. Limiting values

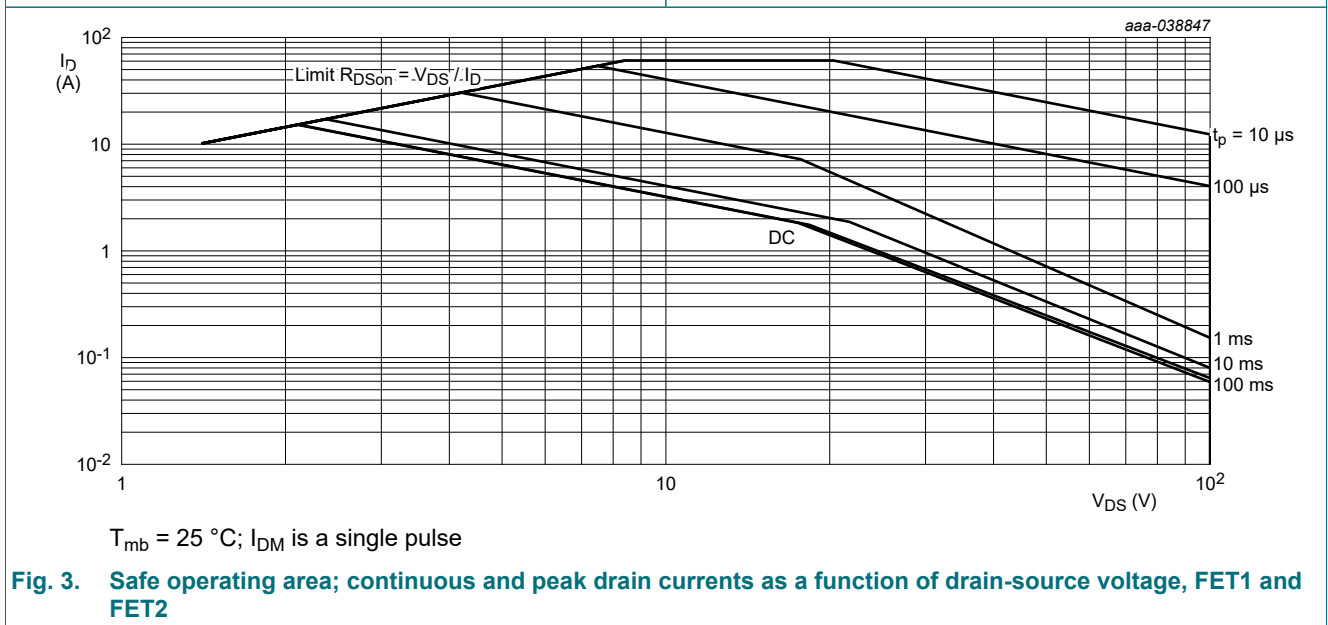
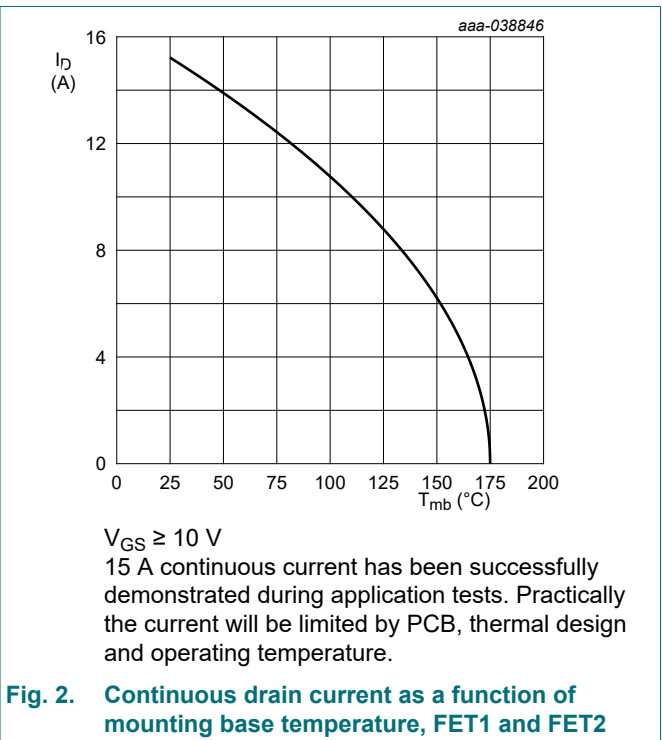
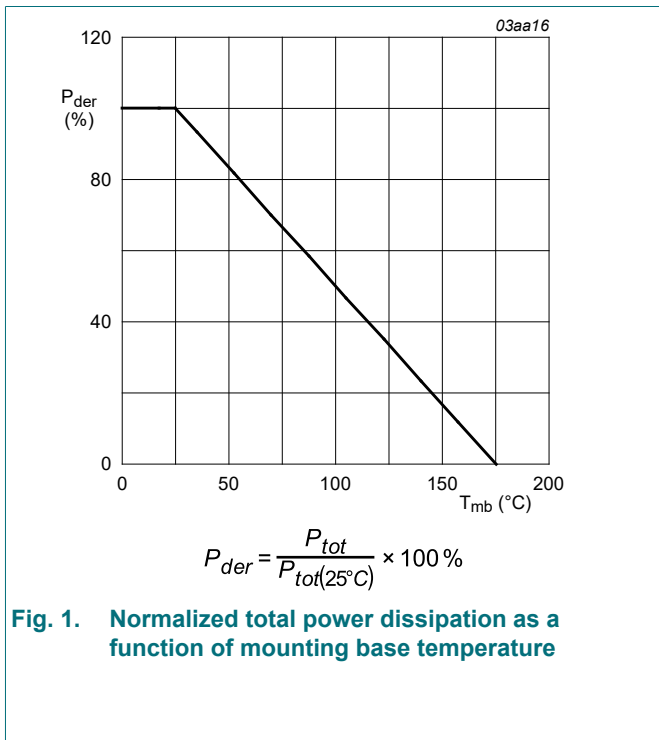
**Table 5. Limiting values**

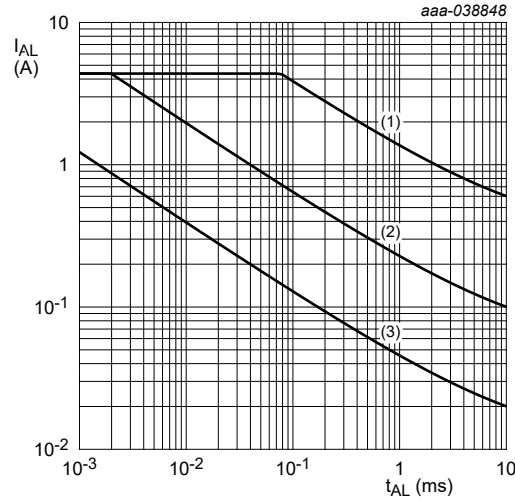
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Limiting values FET1 and FET2</b>						
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V	
$V_{GS}$	gate-source voltage	[1]	-20	20	V	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	32	W	
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	[2]	-	15	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2		-	11	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3	-	61	A	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
<b>Source-drain diode FET1 and FET2</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	15	A	
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	61	A	

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Avalanche ruggedness FET1 and FET2</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 4.4 \text{ A}$ ; $V_{sup} \leq 100 \text{ V}$ ; $R_{GS} = 50 \text{ } \Omega$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; unclamped; $t_{AL} = 77 \text{ } \mu\text{s}$ ; Fig. 4	[3] [4]	-	23	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} = 100 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; $R_{GS} = 50 \text{ } \Omega$ ; Fig. 4	[3] [4]	-	4.4	A

- [1] Refer to application note AN90001 for further information.
- [2] 15 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.





(1)  $T_{j\text{ (init)}} = 25\text{ °C}$ ; (2)  $T_{j\text{ (init)}} = 150\text{ °C}$ ; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	4.2	4.68	K/W

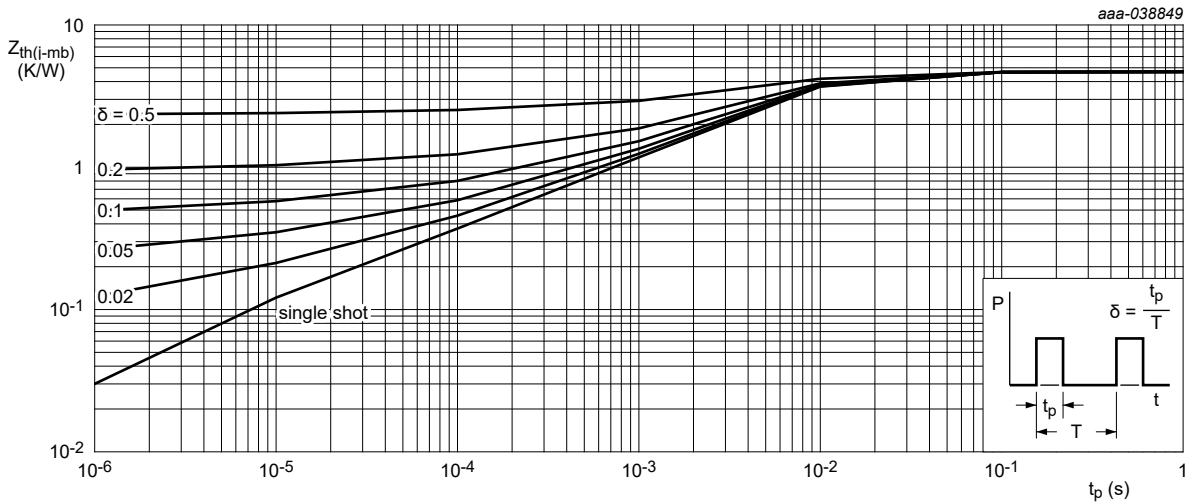


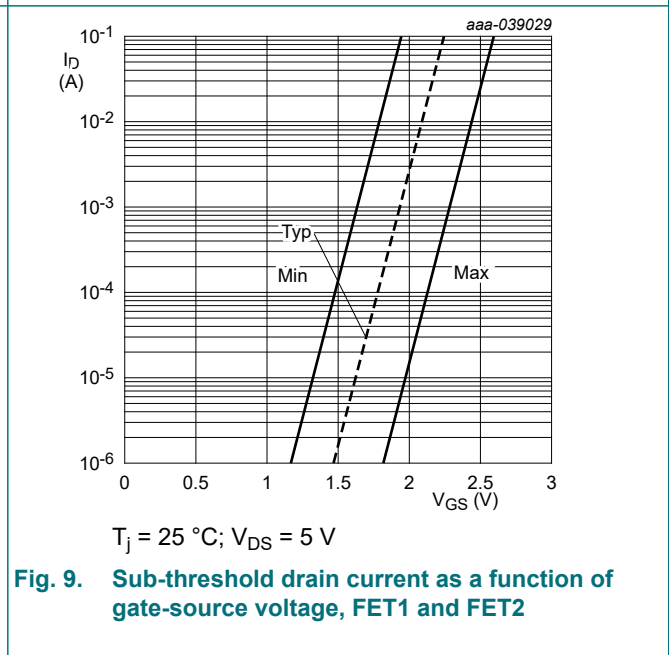
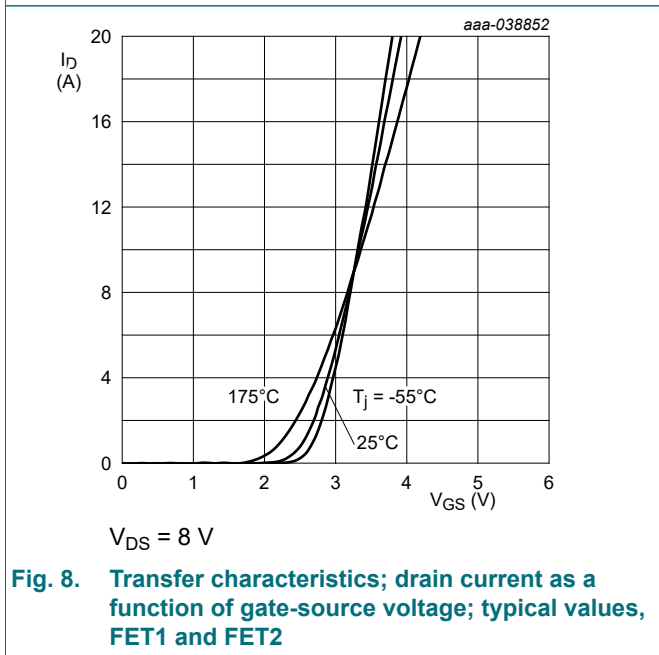
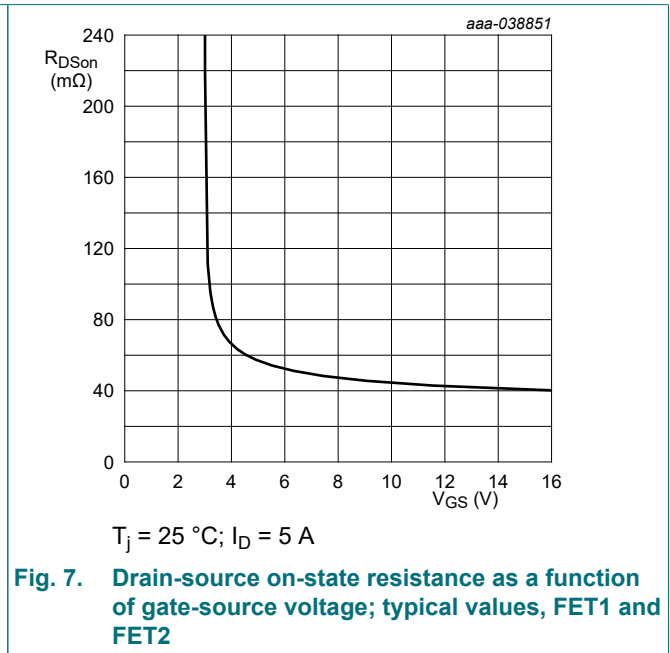
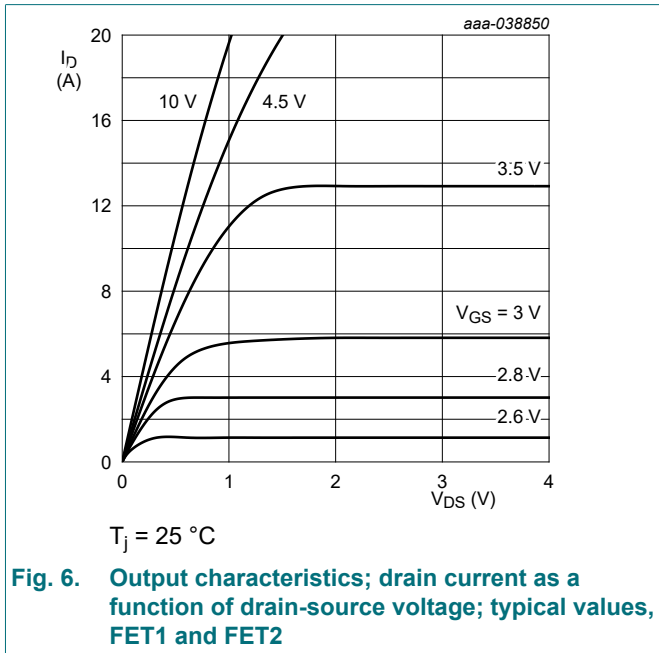
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	119	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -40 \text{ }^\circ\text{C}$	92	109	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	90	106	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.03 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 9; Fig. 10</a>	1.4	1.7	2.05	V
		$I_D = 0.03 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	0.5	-	-	V
		$I_D = 0.03 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.006	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	1.5	100	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	20	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	33	44.6	60.1	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	48.2	68.6	96.1	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 125 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	52.6	75.4	106.8	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	64	94.5	137.5	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	42	60	90	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	61	92	145	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 125 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	67	101.5	160	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	81	127	207	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	0.75	1.5	3	$\Omega$
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 9.6 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13; Fig. 14</a>	3.2	6.3	9.5	nC
		$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13; Fig. 14</a>	5.9	11.8	17.7	nC
$Q_{GS}$	gate-source charge	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13; Fig. 14</a>	1.3	2.2	3.1	nC
$Q_{GD}$	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13; Fig. 14</a>	0.2	1.9	4.2	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13;</a> <a href="#">Fig. 14</a>	-	2.9	-	V
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	434	723	1012	pF
$C_{oss}$	output capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	126	211	338	pF
$C_{rss}$	reverse transfer capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	9.6	24	53	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 12.8\ \Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	6.4	-	ns
$t_r$	rise time		-	8.6	-	ns
$t_{d(off)}$	turn-off delay time		-	8.4	-	ns
$t_f$	fall time		-	7.7	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.85	1	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	39	-	ns
$Q_r$	recovered charge	$V_{DS} = 40\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 17</a>	-	23	-	nC



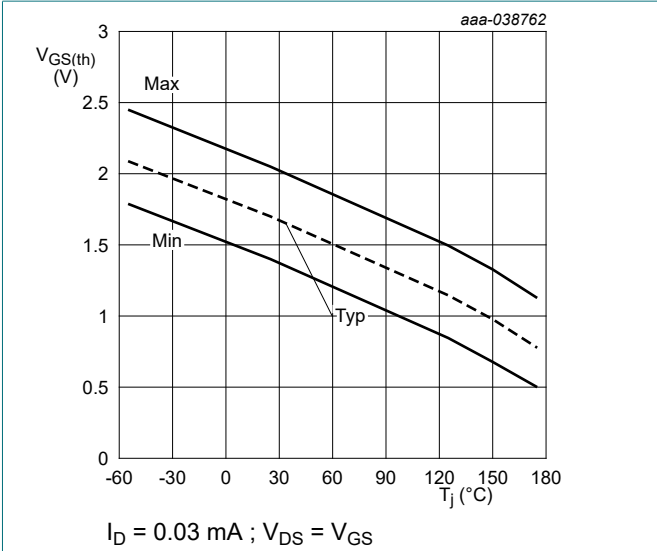


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

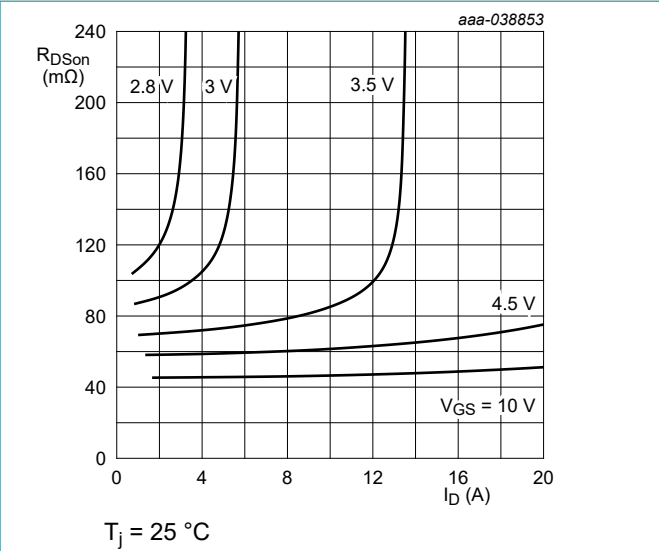


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

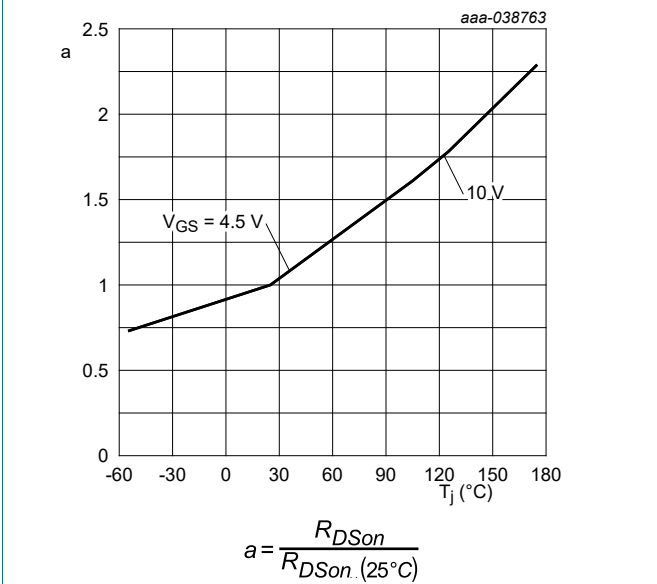


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

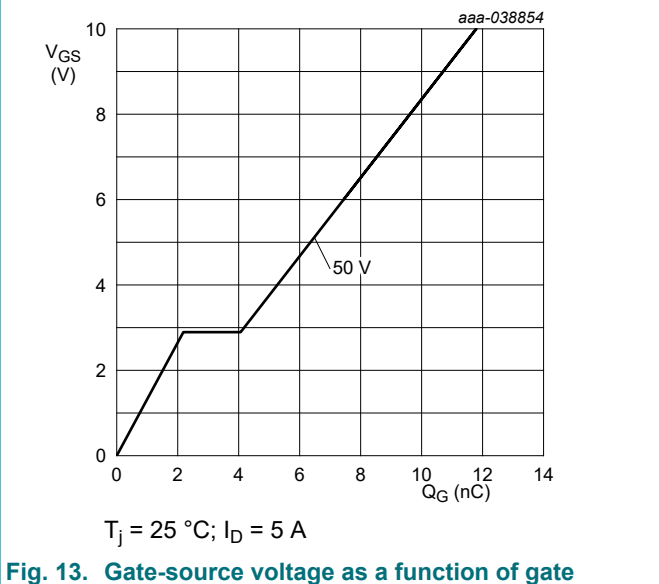


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

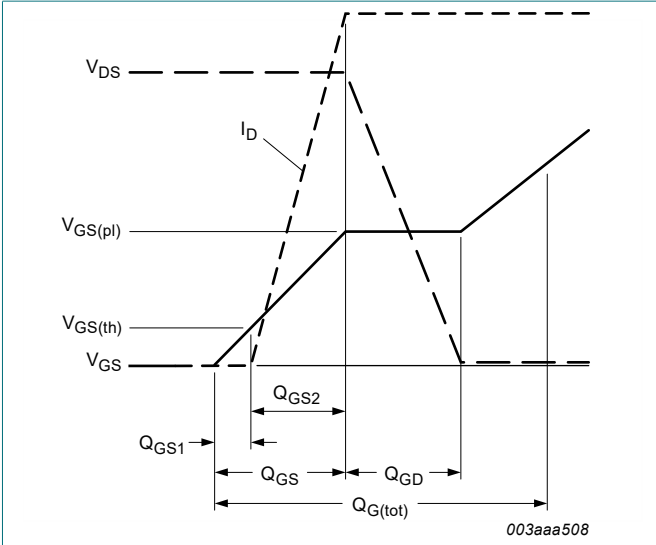


Fig. 14. Gate charge waveform definitions

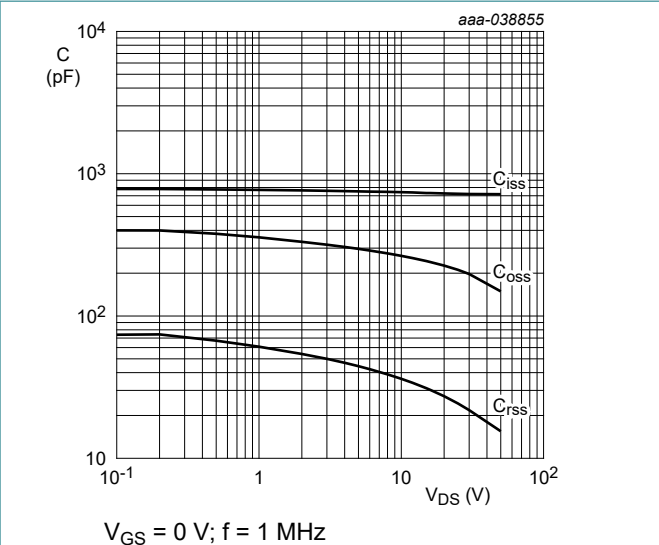


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

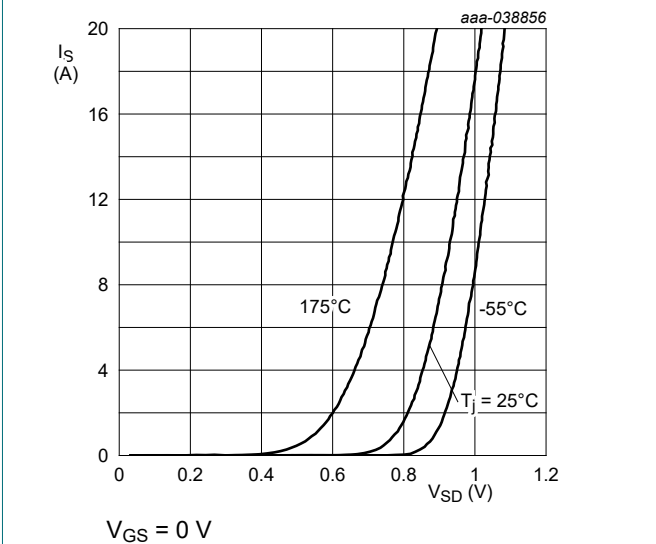


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

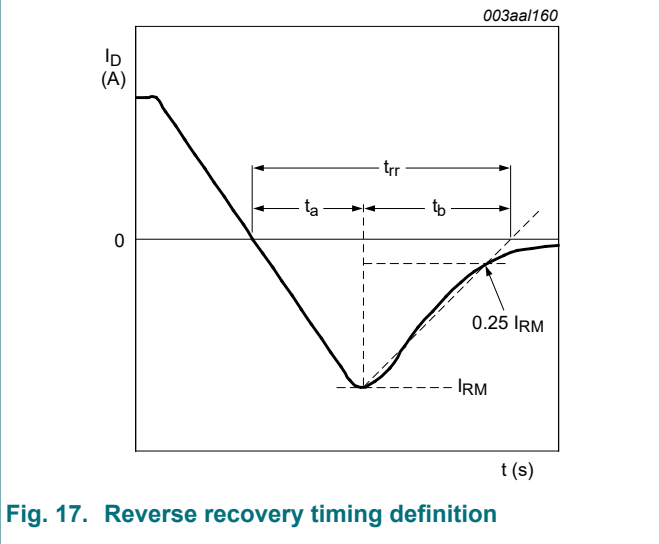


Fig. 17. Reverse recovery timing definition

### 11. Package outline

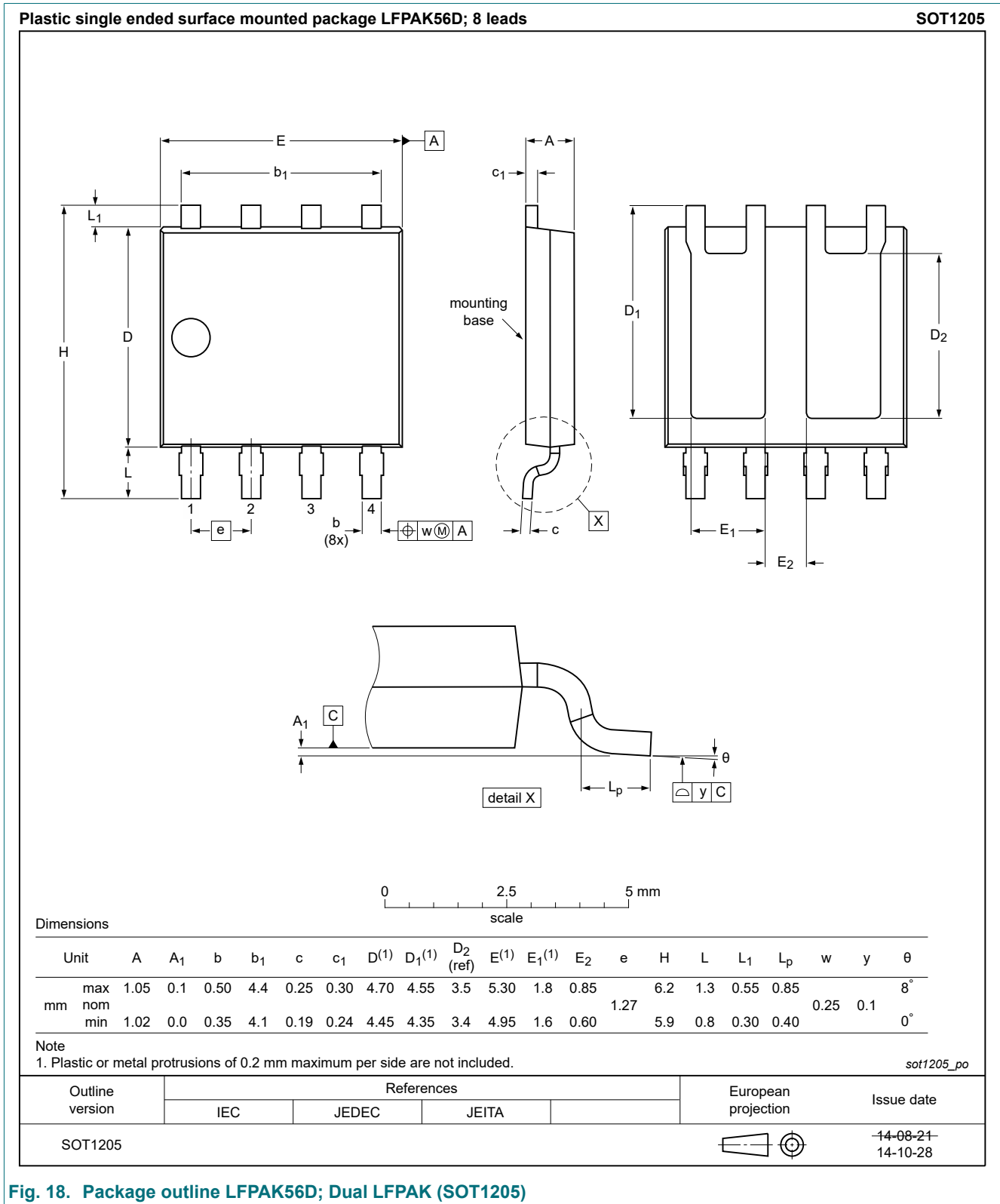


Fig. 18. Package outline LPAK56D; Dual LPAK (SOT1205)

## 12. Soldering

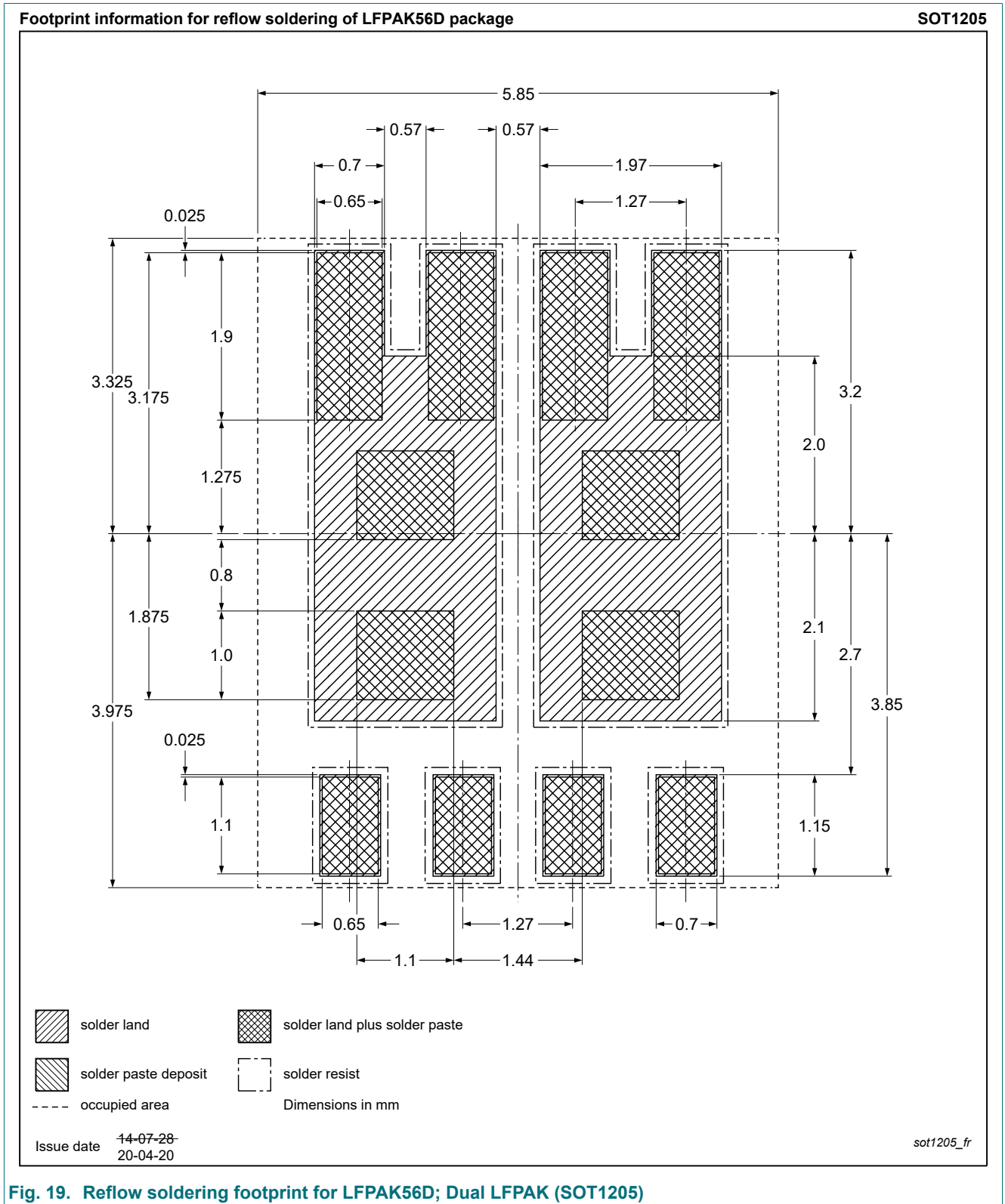


Fig. 19. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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