



BUK7K3R7-40N

Dual N-channel 40 V, 3.7 mOhm standard level MOSFET in LPAK56D

3 March 2025

Product data sheet

1. General description

Automotive qualified Dual N-channel standard level MOSFET using the latest Trench 15 low ohmic enhanced-Trench Bottom Oxide (e-TBO) technology, providing high ruggedness at low $R_{DS(on)}$, housed in an LPAK56D (Dual Power-SO8) package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Dual MOSFET – two silicon dies in one LPAK56D package for significant space saving
- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 15 e-TBO technology:
 - Merging benefits of superjunction technology (high ruggedness) and split-gate technology (low $R_{DS(on)}$)
- Fast and efficient switching with high damping and low spiking
- Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- LPAK copper clip technology:
 - Improved reliability, with reduced R_{th} , $R_{DS(on)}$, and package inductance
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motor, lighting, and solenoid control
- Transmission control
- Ultra high-performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Limiting values FET1 and FET2							
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	105	A
Static characteristics FET1 and FET2							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12		2.2	3.2	3.7	mΩ

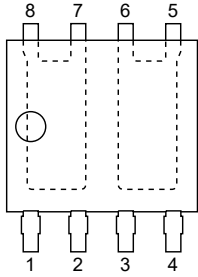
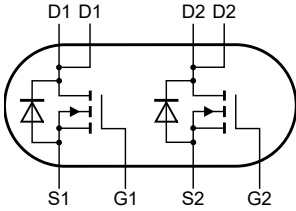
Dual N-channel 40 V, 3.7 mOhm standard level MOSFET in LFPAK56D

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15	28	47	66	nC

[1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D; Dual LPAK (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K3R7-40N	LFPAK56D; Dual LPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K3R7-40N	73N740K

8. Limiting values

Table 5. Limiting values

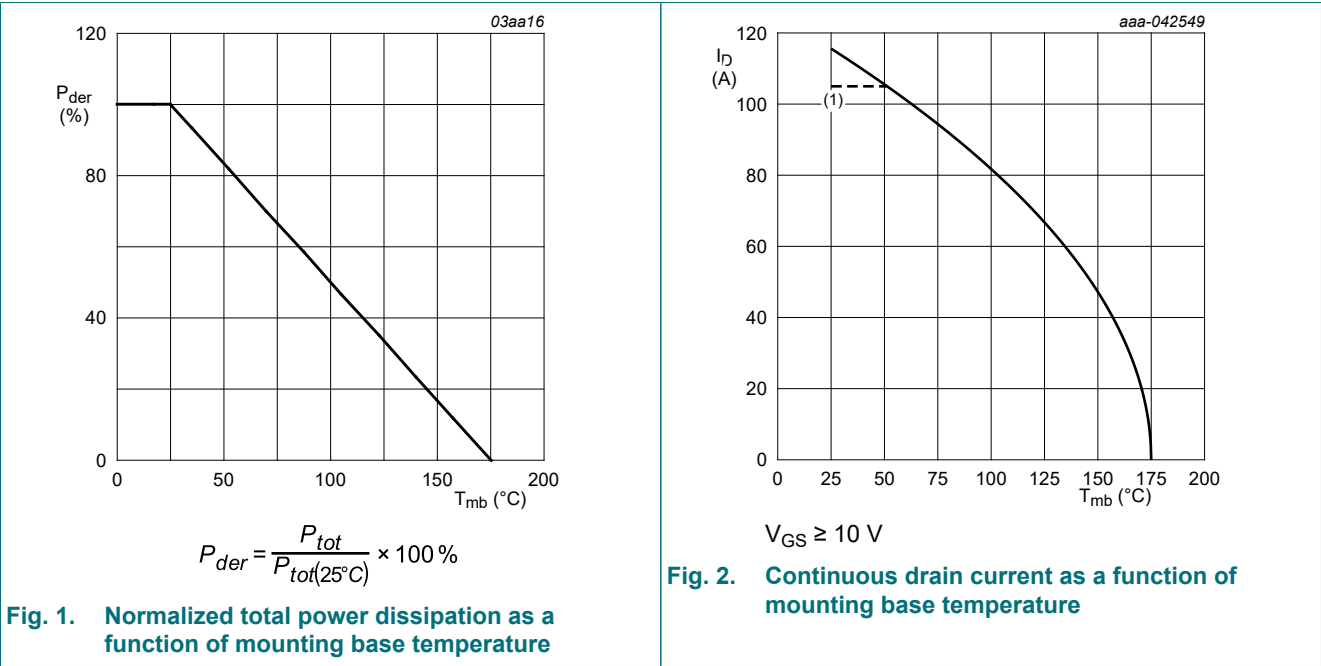
In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
Limiting values FET1 and FET2					
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	97	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	105	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	82	A

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Symbol	Parameter	Conditions		Min	Max	Unit
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3 ; Fig. 4	[1]	-	462	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C	[1]	-	97	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	462	A
Avalanche ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 95 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 5	[2] [3]	-	29.5	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[4]	-	95	A

- [1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test.



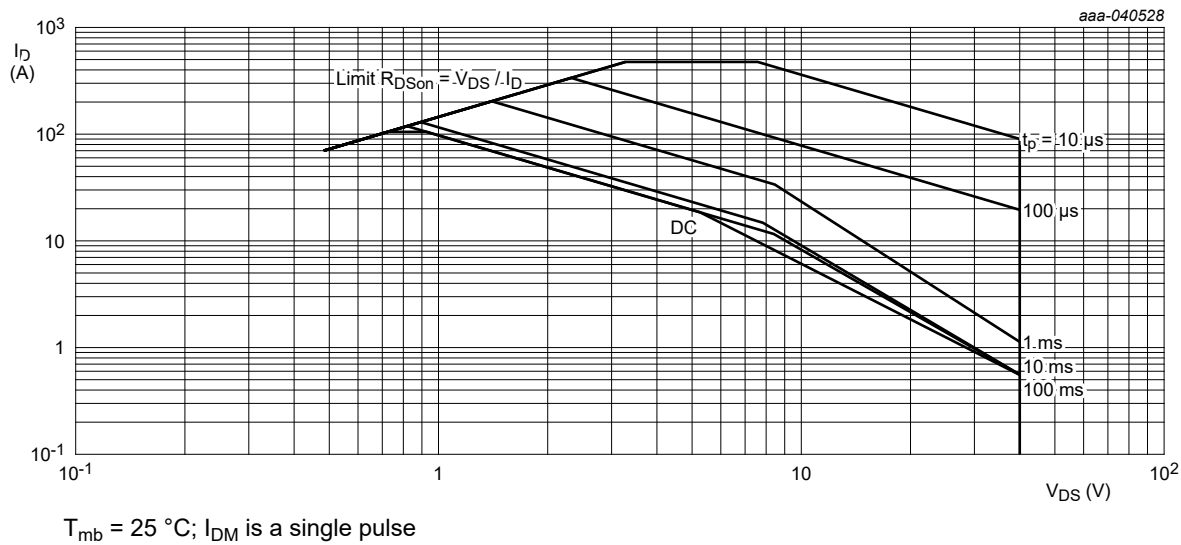


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

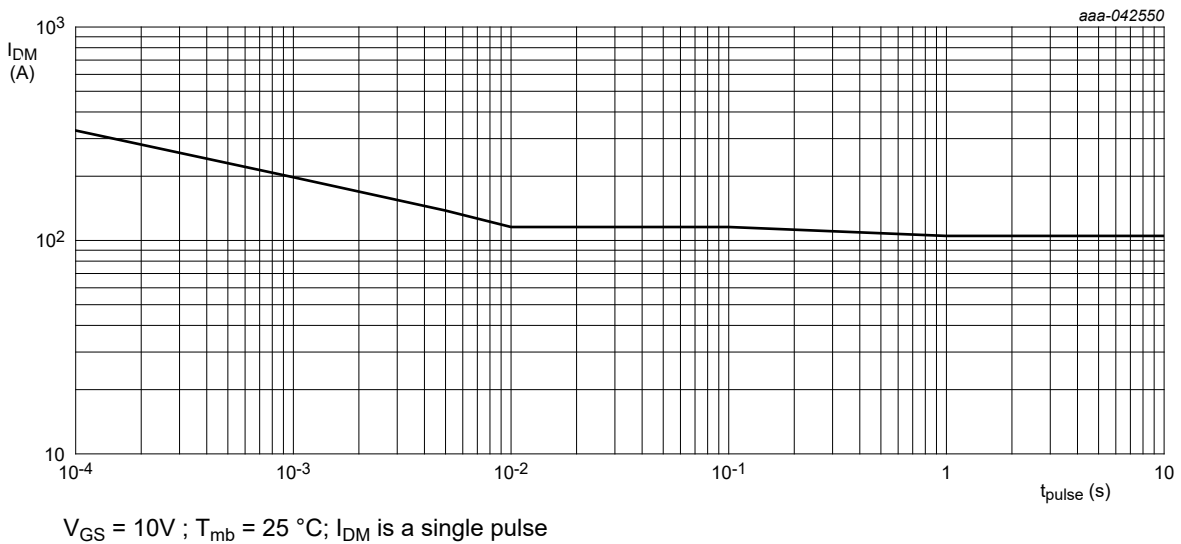
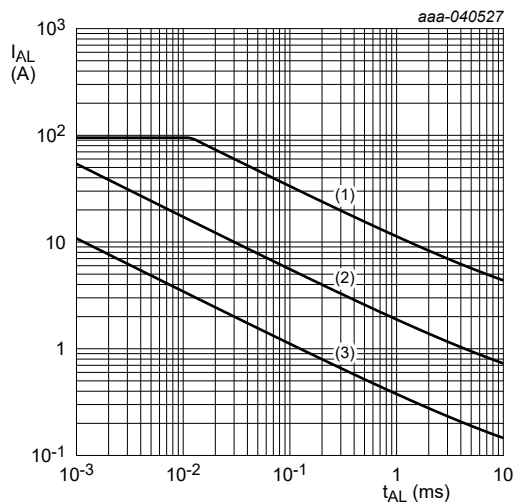


Fig. 4. Peak Current Capability



(1) $T_{j (init)} = 25 \text{ }^{\circ}\text{C}$; (2) $T_{j (init)} = 150 \text{ }^{\circ}\text{C}$; (3) Repetitive Avalanche

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	1.3	1.54	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	30	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

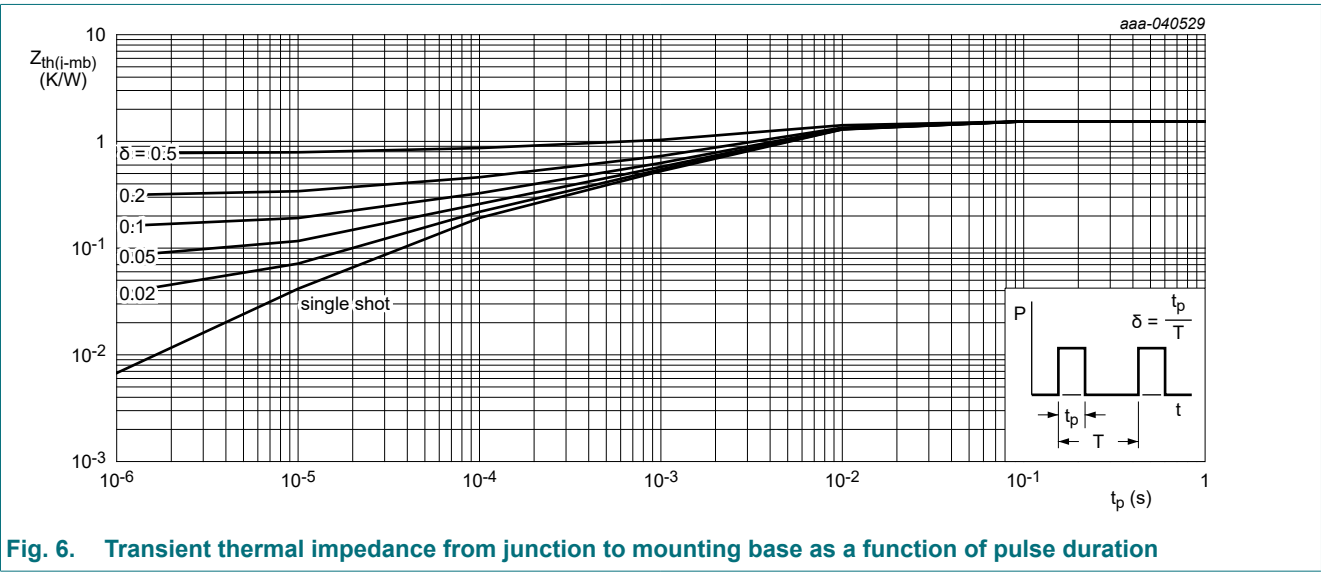


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

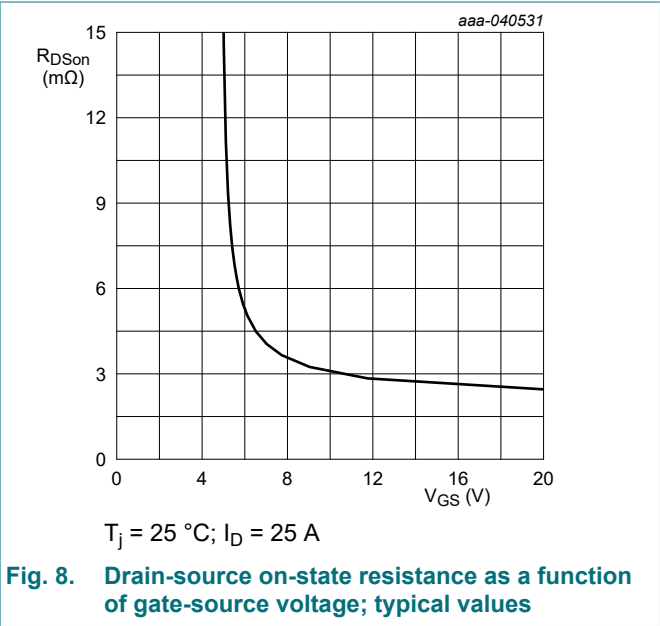
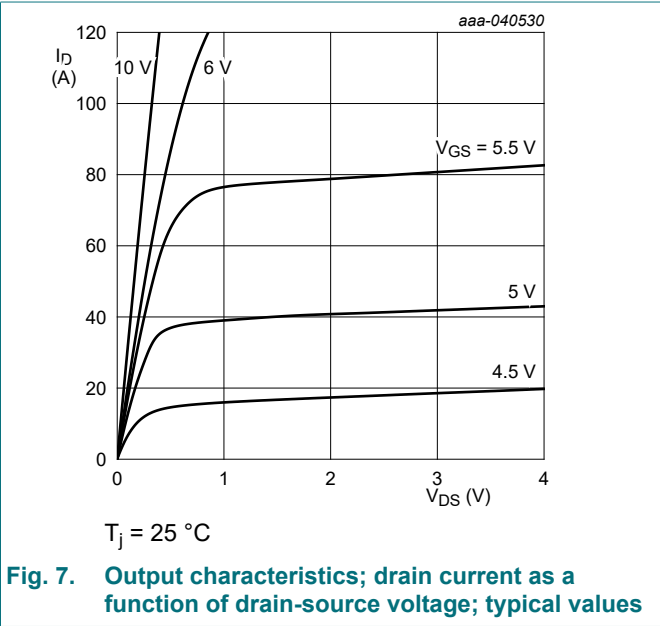
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		40	43	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$		-	41	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ }^\circ\text{C}$		36	40.7	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10		2.4	3	3.6	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = -55\text{ }^\circ\text{C}$; Fig. 11		-	-	4.3	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 11		1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	0.02	1	μA
		$V_{DS} = 16\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$		-	0.26	10	μA
		$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$		-	22	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12		2.2	3.2	3.7	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 105 °C; Fig. 13		2.9	4.4	5.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 125 °C; Fig. 13		3.2	4.8	6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 13		3.8	5.7	7.3	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		-	1	-	Ω
Dynamic characteristics FET1 and FET2							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		28	47	66	nC
Q _{GS}	gate-source charge			6	10	15	nC
Q _{GD}	gate-drain charge			5	16	28	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 16		1404	2340	3277	pF
C _{oss}	output capacitance			474	677	880	pF
C _{rss}	reverse transfer capacitance			86	212	342	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	10	-	ns
t _r	rise time			-	22	-	ns
t _{d(off)}	turn-off delay time			-	27	-	ns
t _f	fall time			-	22	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17		-	0.84	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C; Fig. 18		-	22	-	ns
Q _r	recovered charge		[1]	-	11	-	nC

[1] includes capacitive recovery



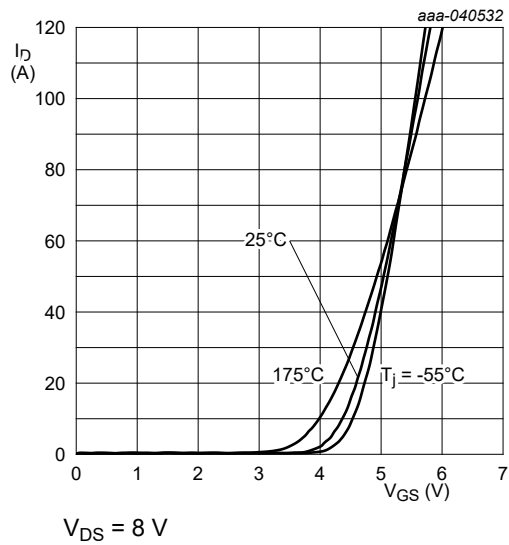


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

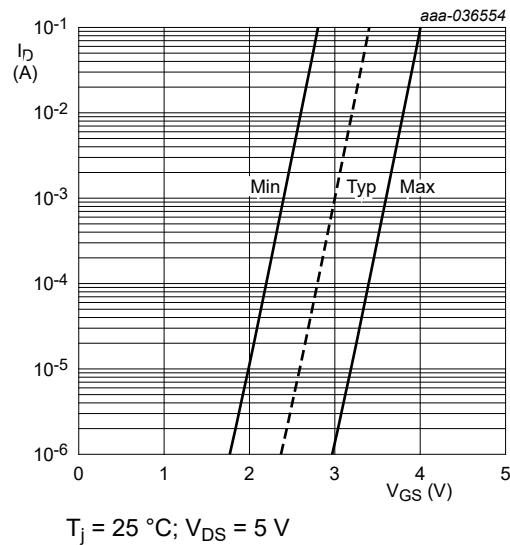


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

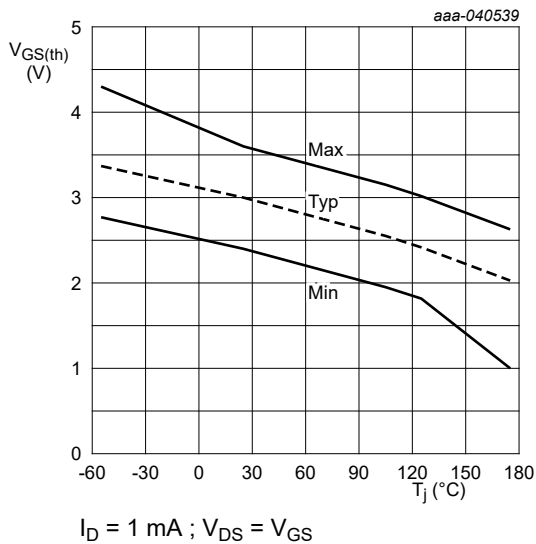


Fig. 11. Gate-source threshold voltage as a function of junction temperature

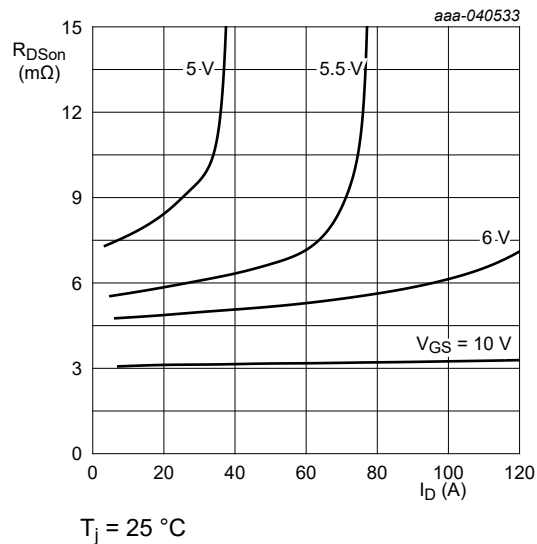


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

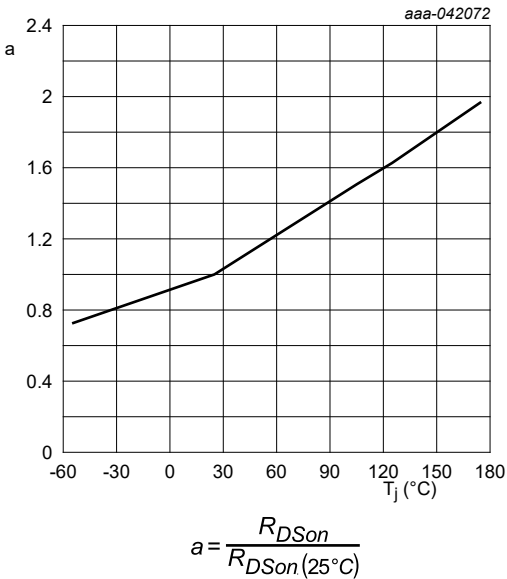


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

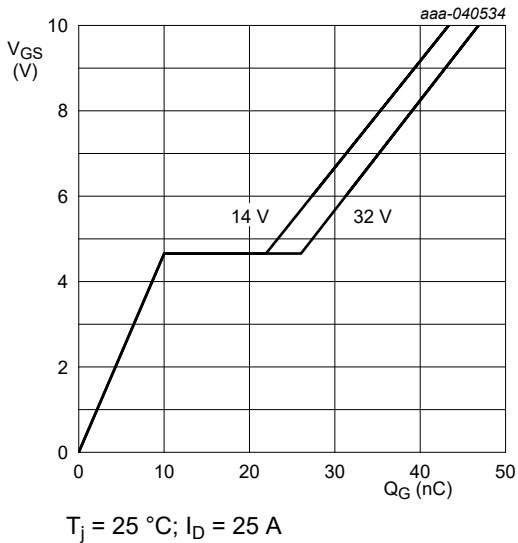


Fig. 14. Gate-source voltage as a function of gate charge; typical values

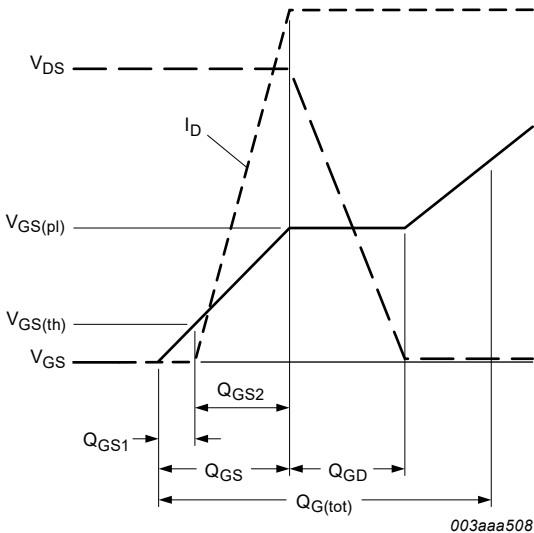


Fig. 15. Gate charge waveform definitions

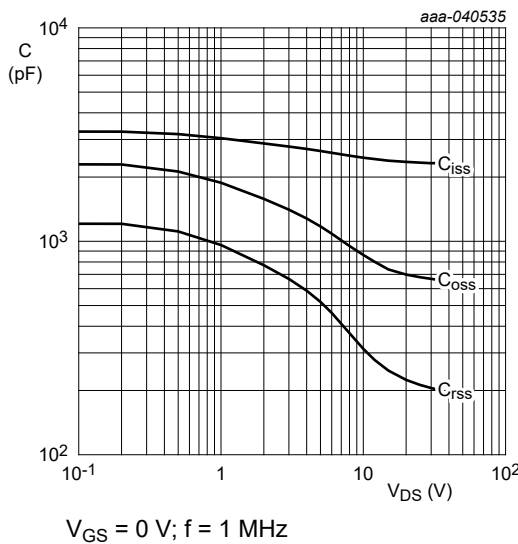


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

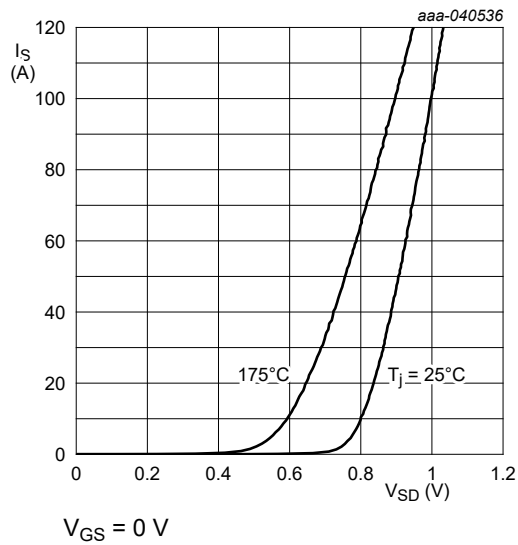


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

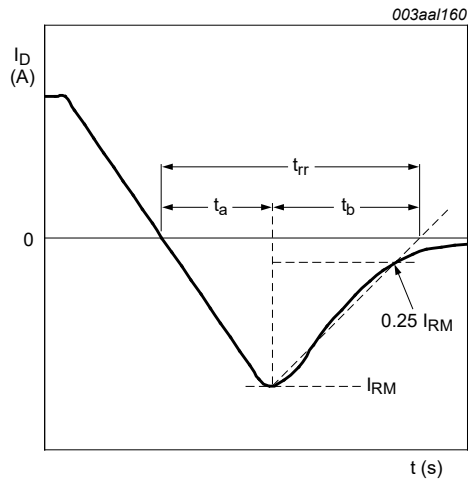
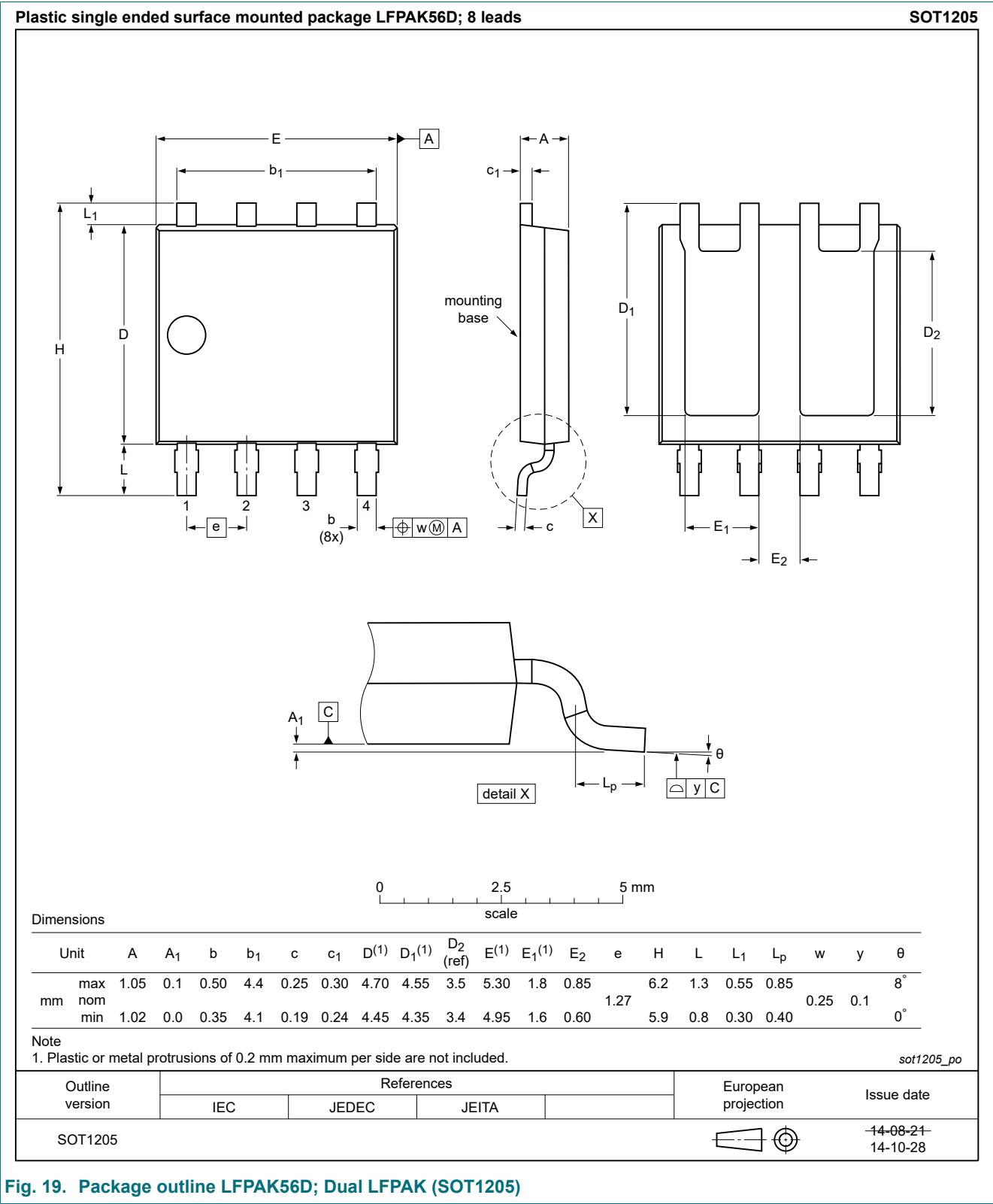


Fig. 18. Reverse recovery timing definition

11. Package outline



12. Soldering

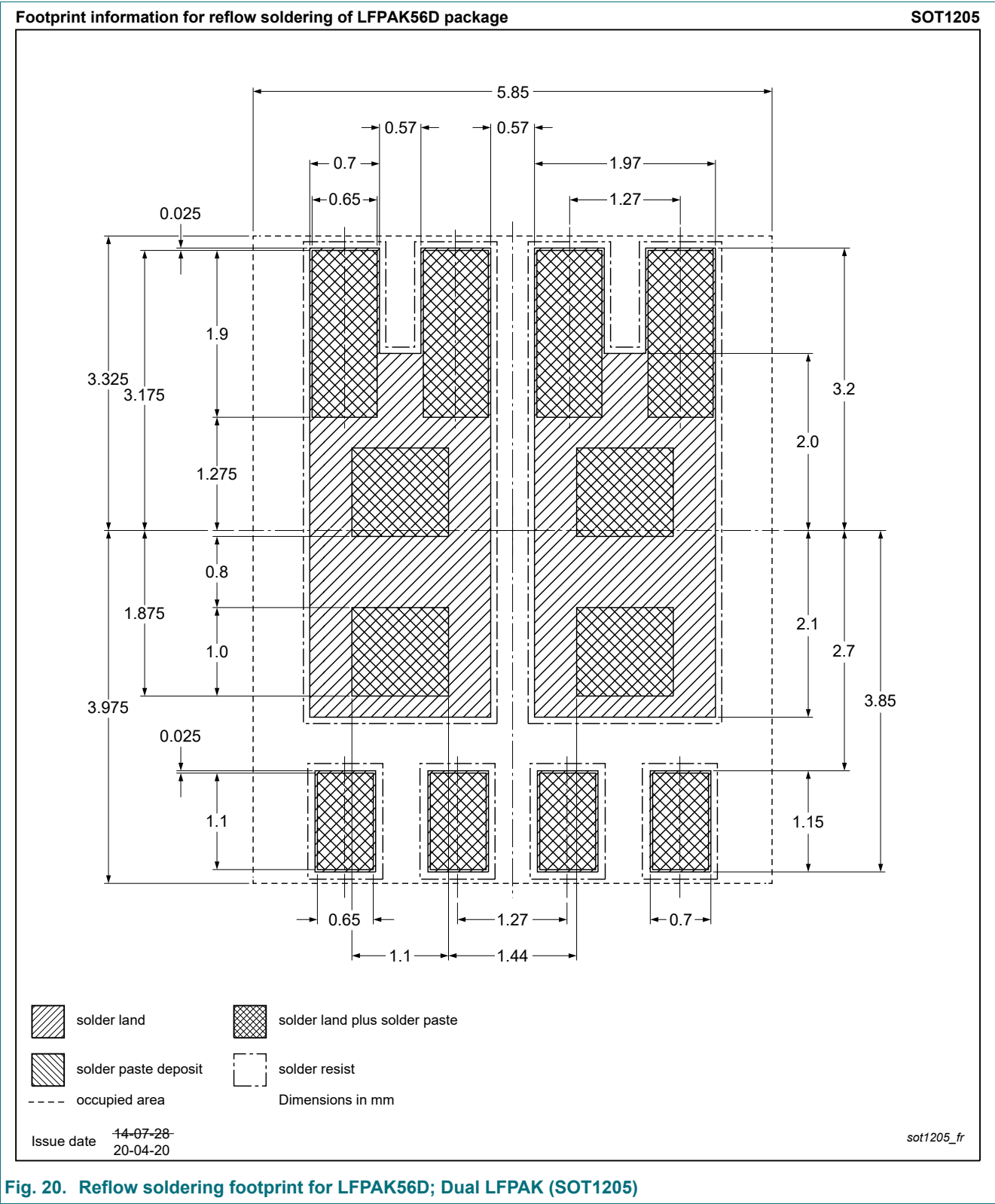


Fig. 20. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 3 March 2025