



BUK9K31-100L

Dual N-Channel 100V, 31 mOhm logic level MOSFET in LPAK56D

17 December 2024

Product data sheet

1. General description

Dual N-channel logic level MOSFET in an LPAK56D (Dual Power-SO8) package. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET – two silicon dies in one LPAK56D package for significant space saving
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automatic optical inspection

3. Applications

- 12 V 24 V and 48 V automotive systems
- Motor, lighting, and solenoid control
- Transmission control
- LED lighting
- Circuit protection

4. Quick reference data

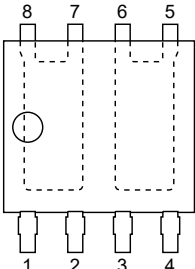
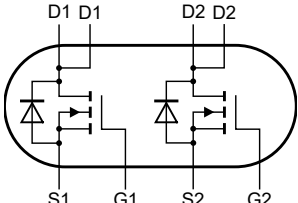
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Limiting values FET1 and FET2							
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	24	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	43	W
Static characteristics FET1 and FET2							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		13.4	25	31.7	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		0.8	2.8	6	nC

[1] 24 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LPAK56D; Dual LPAK (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K31-100L	LPAK56D; Dual LPAK	plastic, single ended surface mounted package (LPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K31-100L	9311HL

8. Limiting values

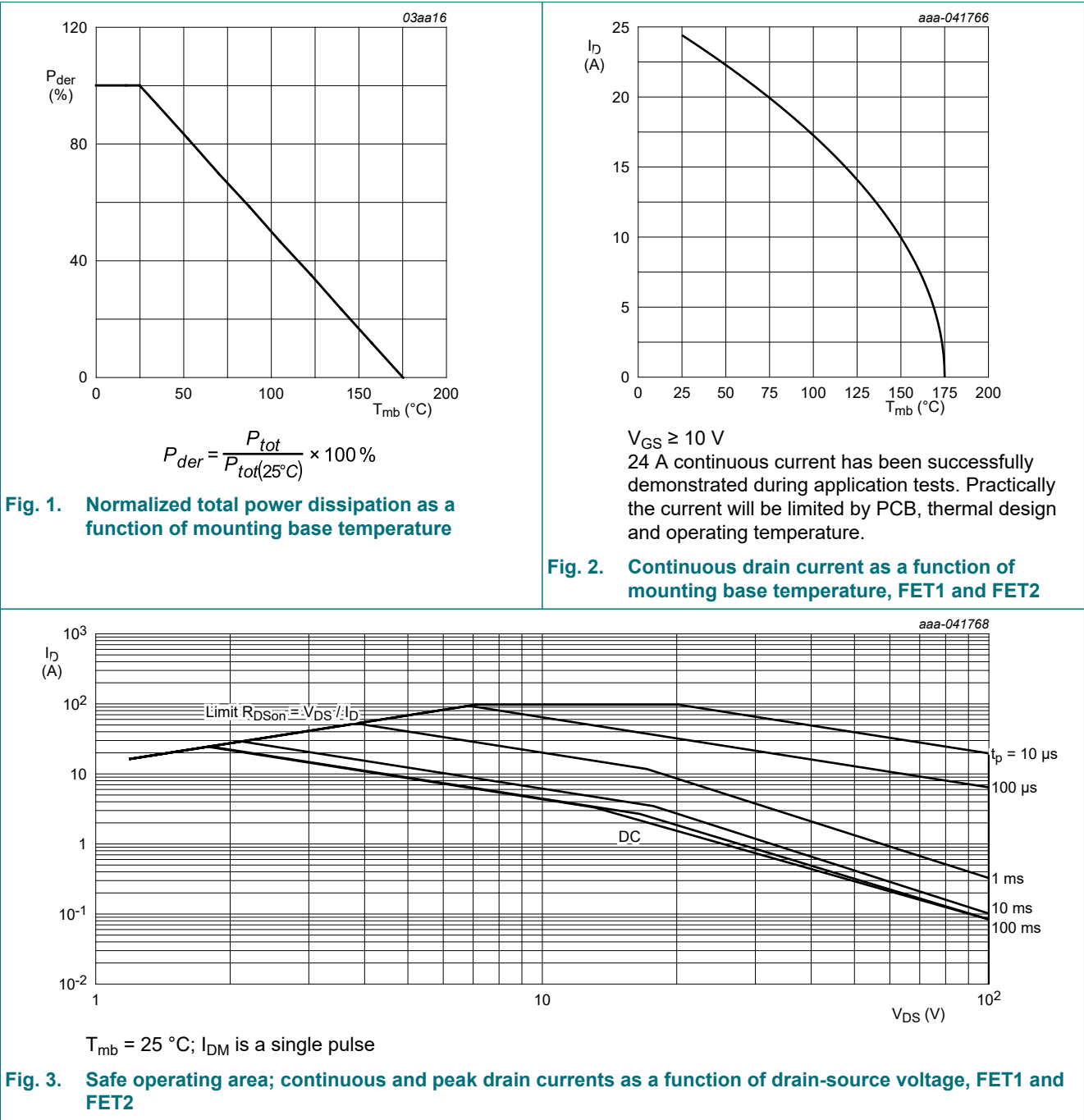
Table 5. Limiting values

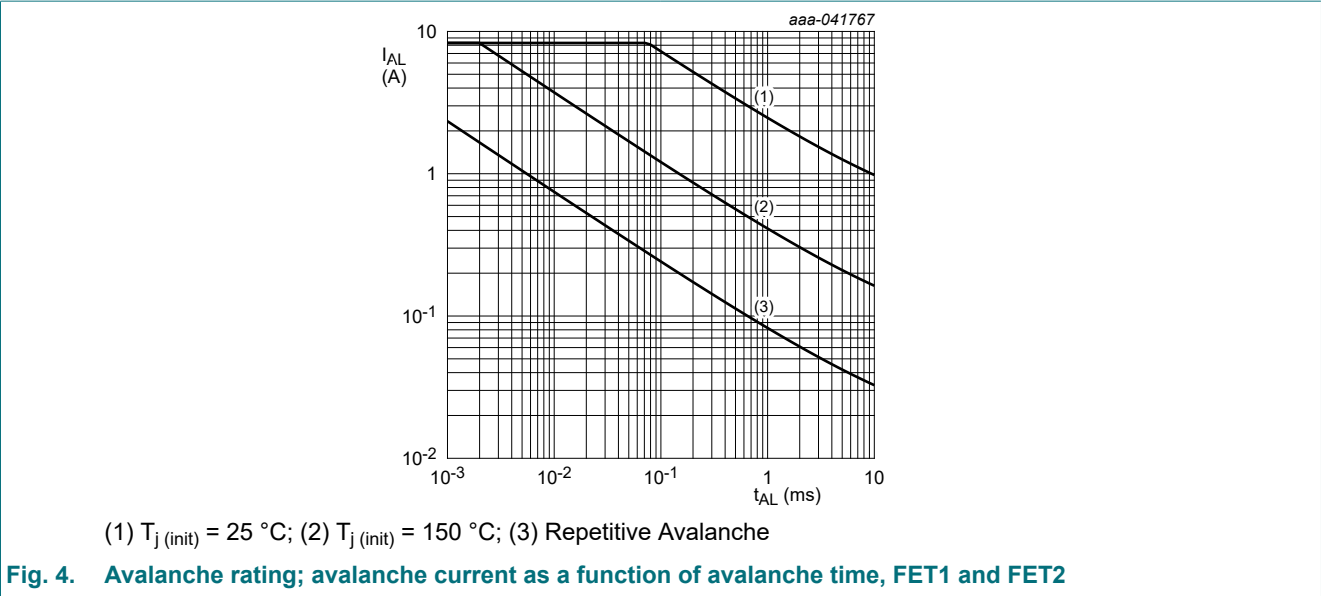
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
Limiting values FET1 and FET2						
VDS	drain-source voltage	25 °C ≤ Tj ≤ 175 °C		-	100	V
VGS	gate-source voltage		[1]	-20	20	V
Ptot	total power dissipation	Tmb = 25 °C; Fig. 1		-	43	W
ID	drain current	VGS = 10 V; Tmb = 25 °C; Fig. 2	[2]	-	24	A
		VGS = 10 V; Tmb = 100 °C; Fig. 2		-	17	A
IDM	peak drain current	pulsed; tp ≤ 10 μs; Tmb = 25 °C; Fig. 3		-	98	A
Tstg	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
IS	source current	Tmb = 25 °C		-	24	A
ISM	peak source current	pulsed; tp ≤ 10 μs; Tmb = 25 °C		-	98	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 8.3 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; t _{AL} = 75 μs; Fig. 4	[3] [4]	-	40.7	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 100 V; V _{GS} = 5 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[3] [4]	-	8.3	A

- [1] Refer to application note AN90001 for further information.
- [2] 24 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

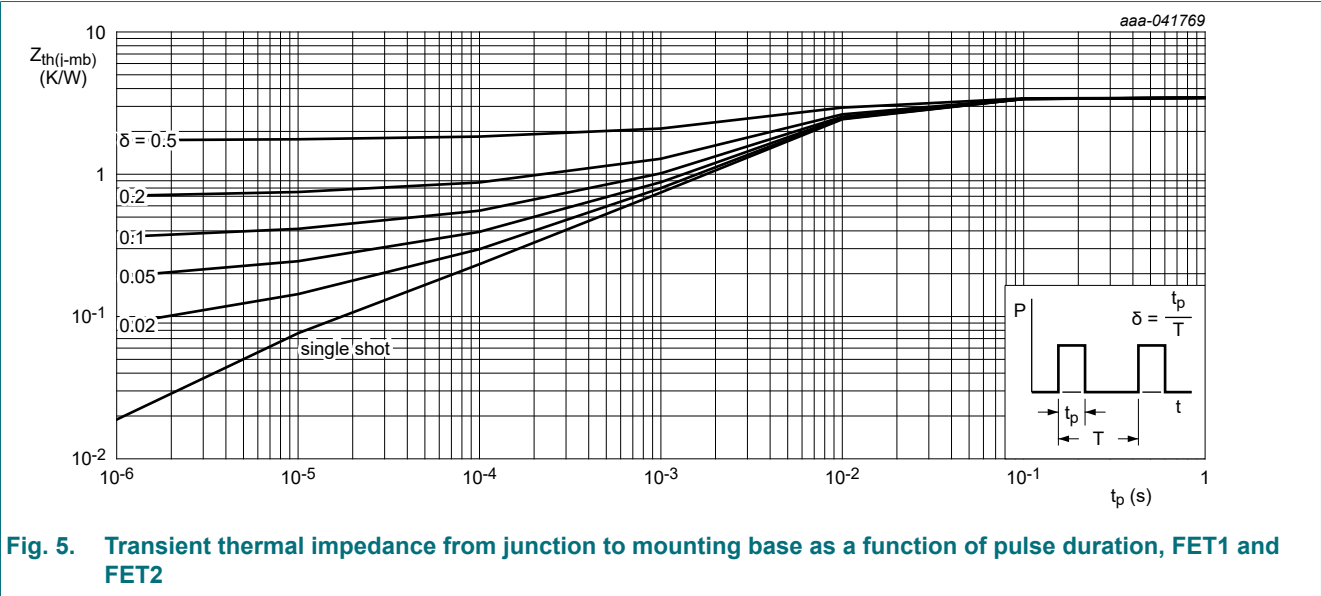




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	2.11	3.45	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 µA; V _{GS} = 0 V; T _J = 25 °C		100	118.3	-	V
		I _D = 250 µA; V _{GS} = 0 V; T _J = -40 °C		92	112	-	V
		I _D = 250 µA; V _{GS} = 0 V; T _J = -55 °C		90	110	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 0.05 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 9 ; Fig. 10		1.4	1.7	2.05	V
		I _D = 0.05 mA; V _{DS} =V _{GS} ; T _J = 175 °C; Fig. 10		0.5	-	-	V
		I _D = 0.05 mA; V _{DS} =V _{GS} ; T _J = -55 °C; Fig. 10		-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _J = 25 °C		-	0.006	1	µA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 125 °C		-	2	100	µA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 175 °C		-	25	500	µA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _J = 25 °C; Fig. 11		13.4	25	31.7	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 100 °C; Fig. 12		19.7	38.5	51	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 125 °C; Fig. 12		21.5	42.3	56.3	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 175 °C; Fig. 12		26.2	53	72.5	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 25 °C; Fig. 11		21.7	31	47	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 100 °C; Fig. 12		32	47.7	75.5	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 125 °C; Fig. 12		34.8	52.4	83.5	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 175 °C; Fig. 12		42.4	65.7	107.6	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.8	1.6	3.2	Ω
Dynamic characteristics FET1 and FET2							
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 5 V; T _J = 25 °C; Fig. 13 ; Fig. 14		5.4	10.9	16.3	nC
		I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		10.3	20.7	31	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 5 V; T _J = 25 °C; Fig. 13 ; Fig. 14		2.2	3.7	5.2	nC
Q _{GD}	gate-drain charge			0.8	2.8	6	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 5 A; V _{DS} = 50 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	2.8	-	V
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15		832	1386	1940	pF
C _{oss}	output capacitance			196	326	521	pF
C _{rss}	reverse transfer capacitance			12	30	49	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 10 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	9.7	-	ns
t _r	rise time			-	9.2	-	ns
t _{d(off)}	turn-off delay time			-	14.5	-	ns
t _f	fall time			-	9.1	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.83	1	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;		-	42	-	ns
Q _r	recovered charge	V _{DS} = 50 V; T _j = 25 °C; Fig. 17		-	29	-	nC

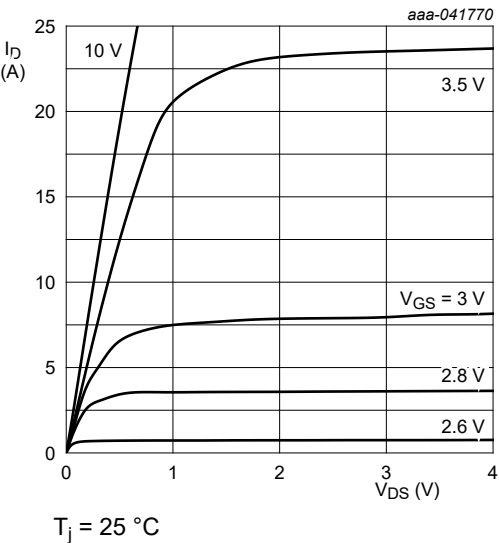


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

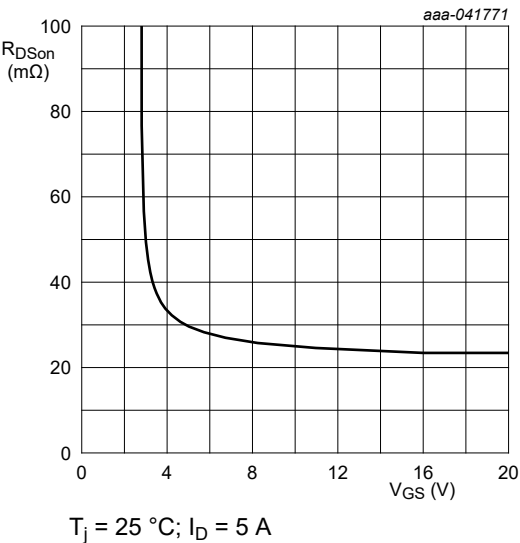


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

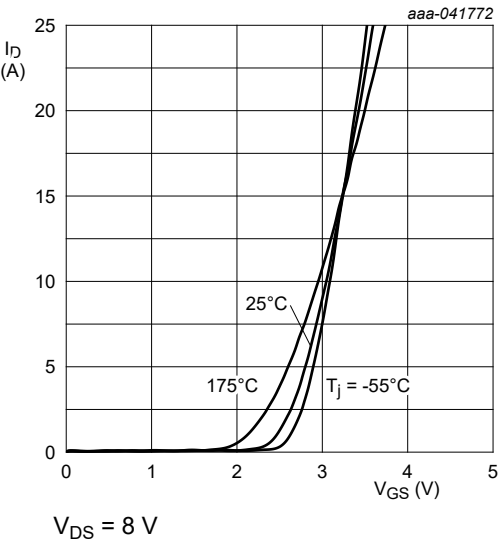


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

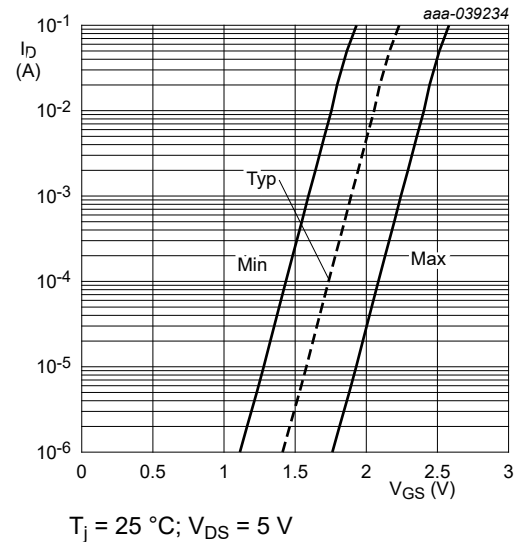


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

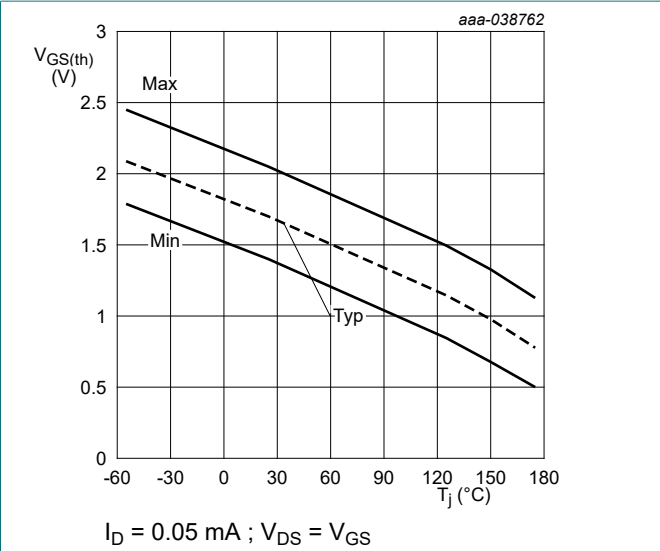


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

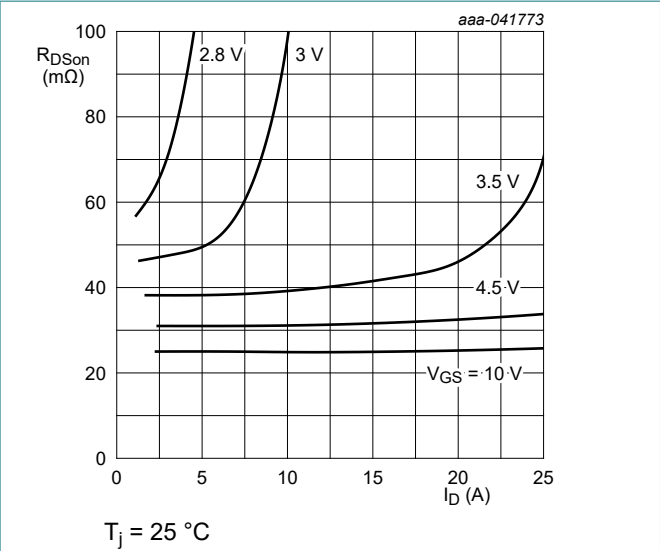


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

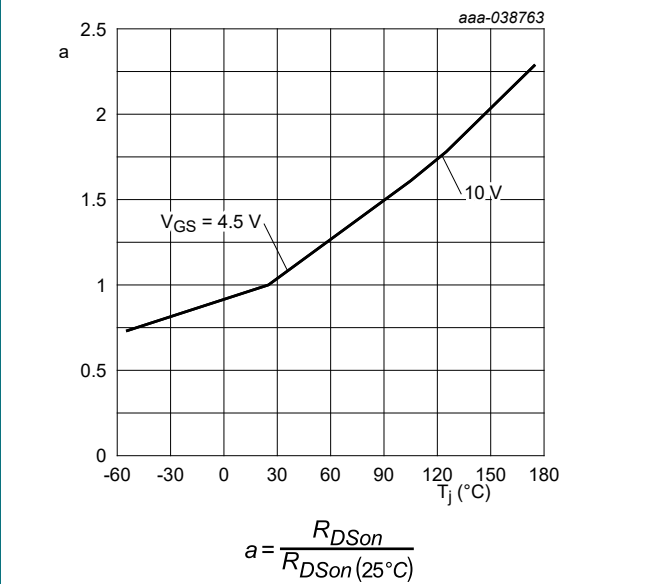


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

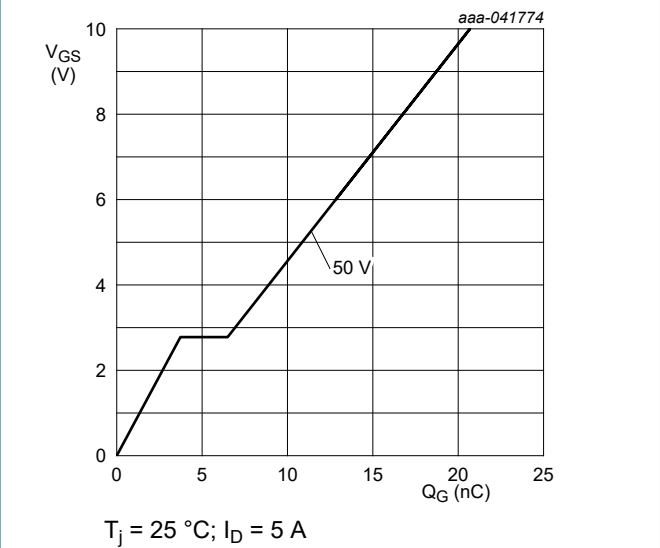


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

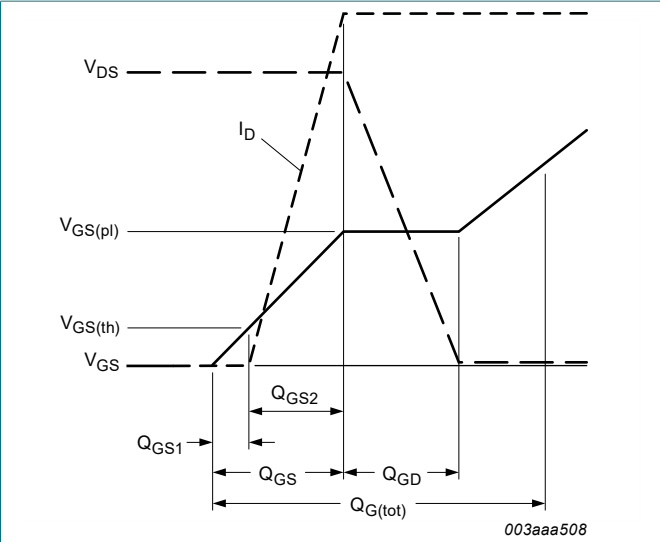


Fig. 14. Gate charge waveform definitions

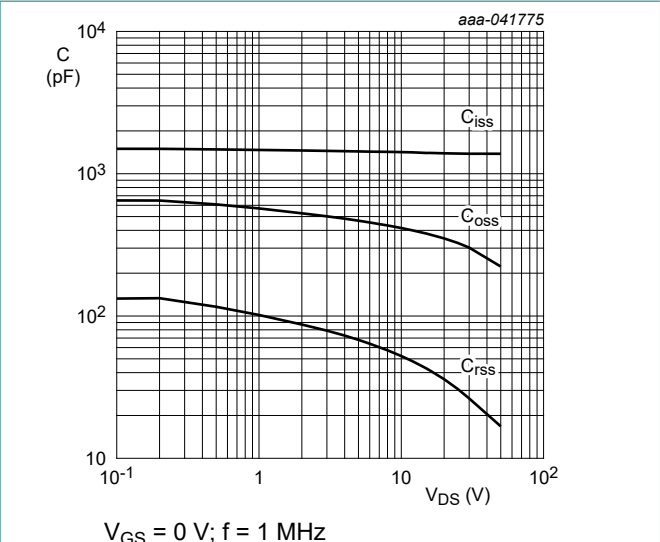


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

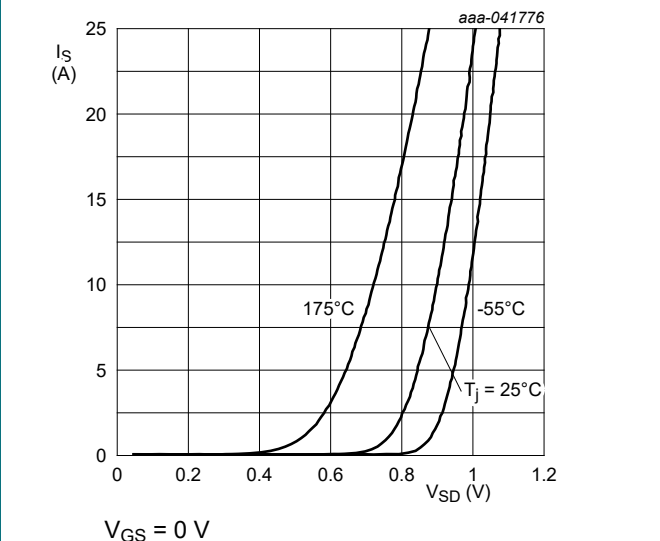


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

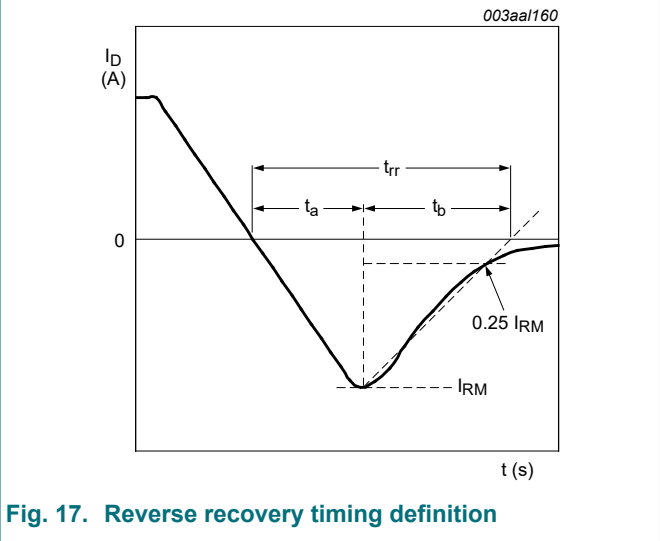


Fig. 17. Reverse recovery timing definition

11. Package outline

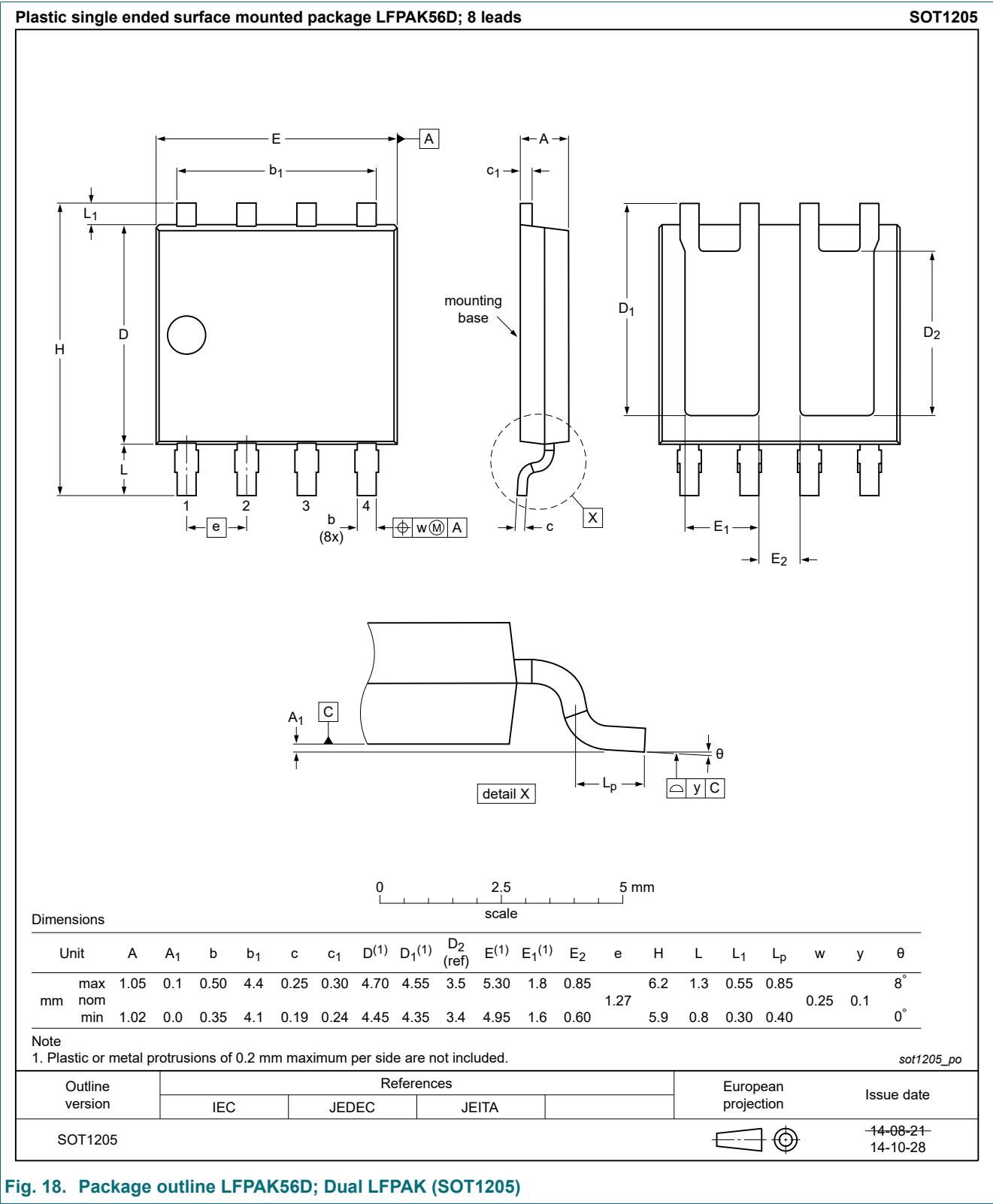


Fig. 18. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Legal information

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