

BXC9R4R5-40H

Logic level N-Channel MOSFET in MLPAK56-WF (SOT8038-2)

15 January 2025

Product data sheet

1. General description

Logic level N-Channel MOSFET in a small MLPAK56-WF (SOT8038-2) package, using Trench 9 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Trench 9 technology
- Low $R_{DS(on)}$ to minimize conduction losses
- Small footprint (5 x 6 mm) for compact design
- Qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automated optical inspection

3. Applications

- Motor drive
- Battery protection
- DC-DC conversion

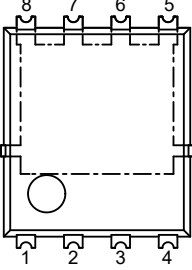
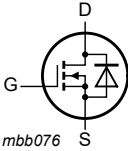
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	91	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	71	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	2.7	3.8	4.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	3.7	7.4	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK56-WF (SOT8038-2)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BXK9R4R5-40H	MLPAK56-WF	MLPAK56-WF: 8 terminals; body 5.15 x 6.2 x 1.0 mm	SOT8038-2

7. Marking

Table 4. Marking codes

Type number	Marking code
BXK9R4R5-40H	94H540R

8. Limiting values

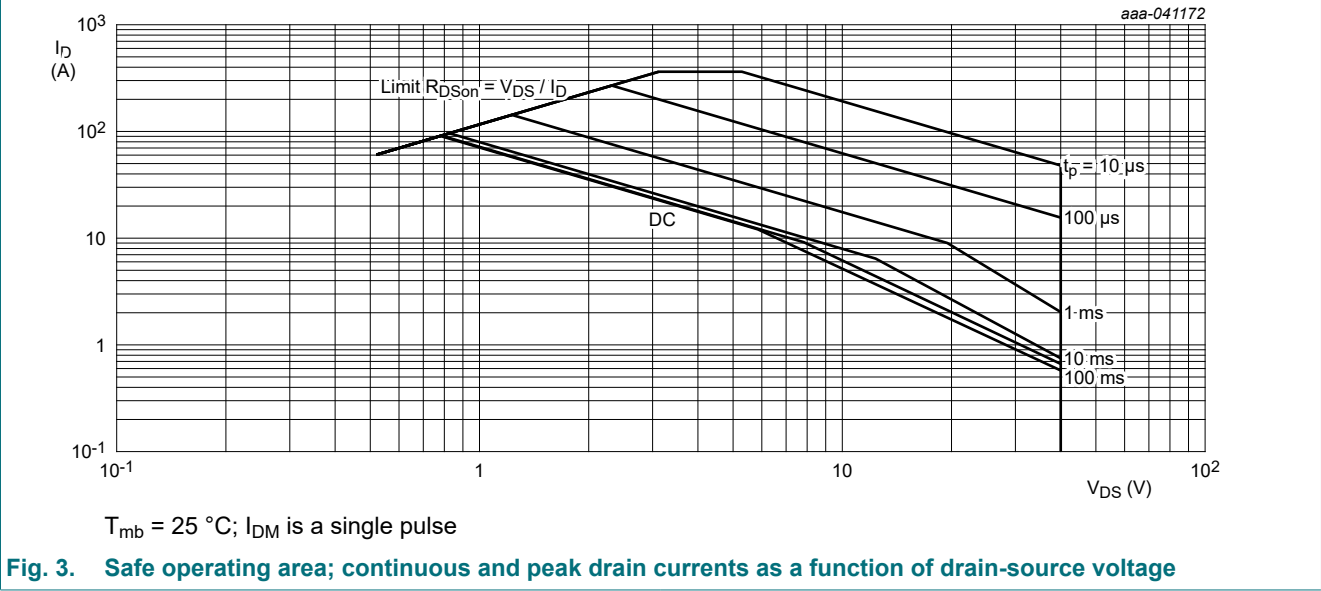
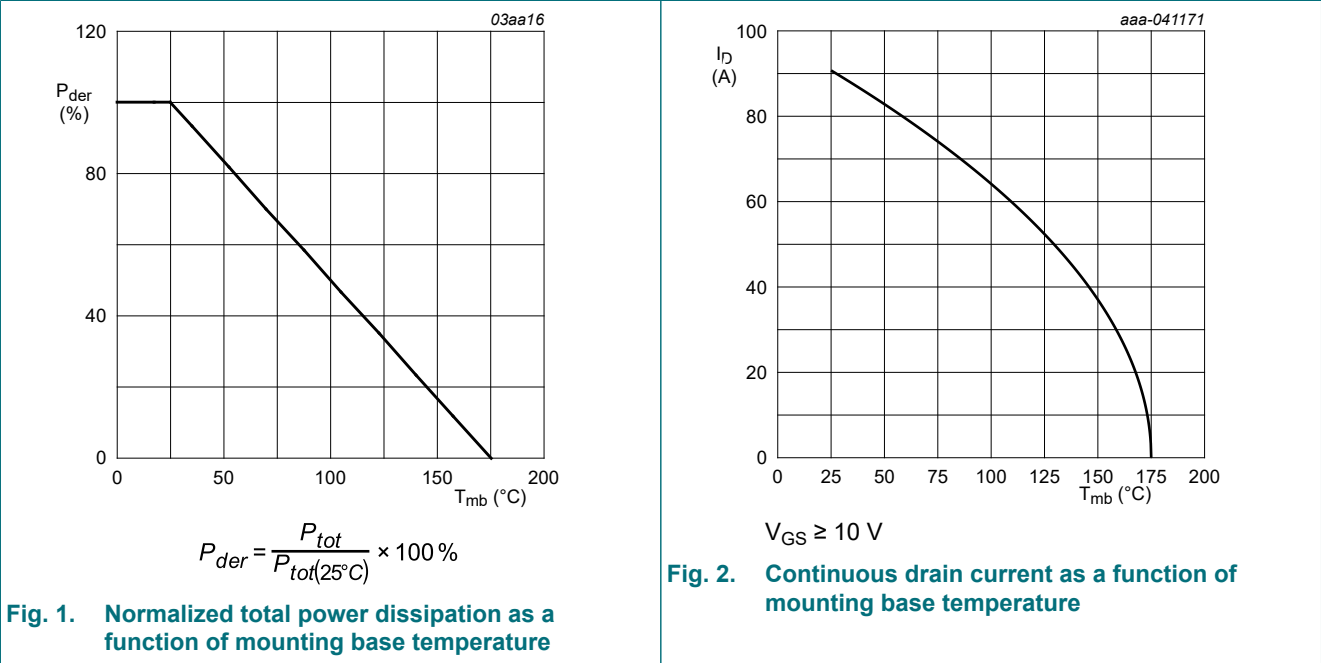
Table 5. Limiting values

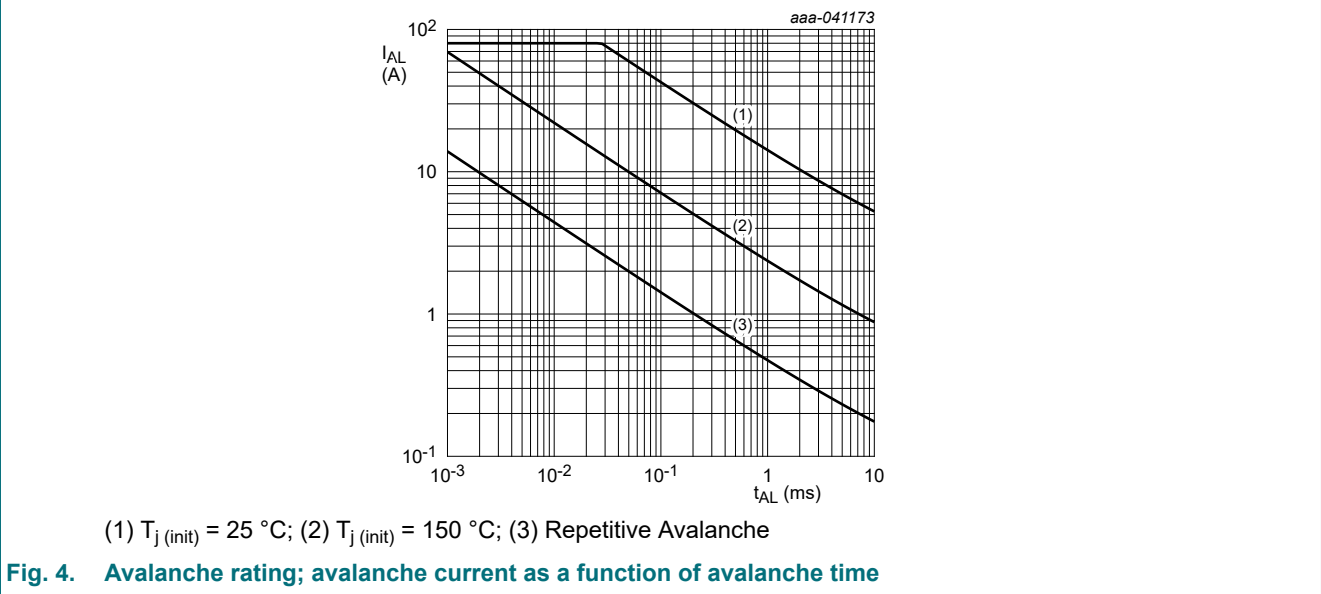
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
VDS	drain-source voltage	25 °C ≤ Tj ≤ 175 °C		-	40	V
VGS	gate-source voltage			-20	20	V
Ptot	total power dissipation	Tmb = 25 °C; Fig. 1		-	71	W
ID	drain current	VGS = 10 V; Tmb = 25 °C; Fig. 2		-	91	A
		VGS = 10 V; Tmb = 100 °C		-	64	A
IDM	peak drain current	pulsed; tp ≤ 10 μs; Tmb = 25 °C; Fig. 3		-	363	A
Tstg	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain diode						
IS	source current	Tmb = 25 °C		-	59	A
ISM	peak source current	pulsed; tp ≤ 10 μs; Tmb = 25 °C		-	363	A
Avalanche ruggedness						
EDS(AL)S	non-repetitive drain-source avalanche energy	ID = 80 A; Vsup ≤ 40 V; RGS = 50 Ω; VGS = 10 V; Tj(init) = 25 °C; unclamped	[1] [2] [3]	-	58	mJ

Symbol	Parameter	Conditions		Min	Max	Unit
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[3]	-	80	A

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.
- [3] Protected by 100% test.



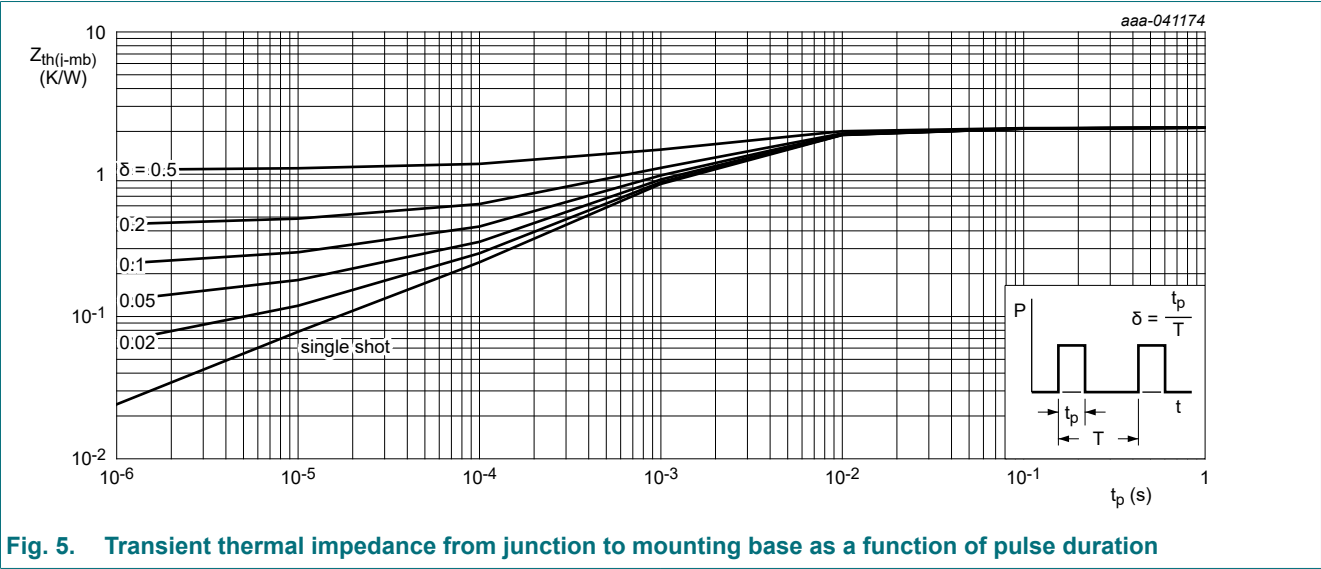


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.77	2.12	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	25	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		40	43	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = -40\text{ }^\circ\text{C}$		-	40.5	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = -55\text{ }^\circ\text{C}$		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10		1.45	1.76	2.15	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = -55\text{ }^\circ\text{C}$; Fig. 10		-	-	2.6	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 175\text{ }^\circ\text{C}$; Fig. 10		0.7	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	0.02	1	μA
		$V_{DS} = 16\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 125\text{ }^\circ\text{C}$		-	0.7	10	μA
		$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 175\text{ }^\circ\text{C}$		-	70	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 11		2.7	3.8	4.5	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 105\text{ }^\circ\text{C}$; Fig. 12		3.6	5.4	6.7	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 125\text{ }^\circ\text{C}$; Fig. 12		3.9	5.9	7.3	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 175\text{ }^\circ\text{C}$; Fig. 12		4.6	7	8.6	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 11		3.2	4.6	5.9	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_J = 105\text{ }^\circ\text{C}$; Fig. 12		4.3	6.5	8.7	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_J = 125\text{ }^\circ\text{C}$; Fig. 12		4.7	7	9.5	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_J = 175\text{ }^\circ\text{C}$; Fig. 12		5.5	8.4	11.3	m Ω
R_G	gate resistance	$f = 1\text{ MHz}$; $T_J = 25\text{ }^\circ\text{C}$		0.8	2	5.1	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 13 ; Fig. 14		-	36	50	nC
		$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 13 ; Fig. 14		-	16	23	nC
Q_{GS}	gate-source charge			-	6.6	10	nC
Q_{GD}	gate-drain charge			-	3.7	7.4	nC
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 15		-	2512	3517	pF
C_{oss}	output capacitance			-	437	612	pF
C_{rss}	reverse transfer capacitance			-	100	220	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}$; $R_L = 0.8\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$; $T_J = 25\text{ }^\circ\text{C}$		-	16	-	ns
t_r	rise time			-	24	-	ns
$t_{d(off)}$	turn-off delay time			-	22	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t _f	fall time			-	14	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.83	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	[1]	-	23	-	ns
Q _r	recovered charge	V _{DS} = 20 V; T _j = 25 °C; Fig. 17		-	14	-	nC

[1] includes capacitive recovery

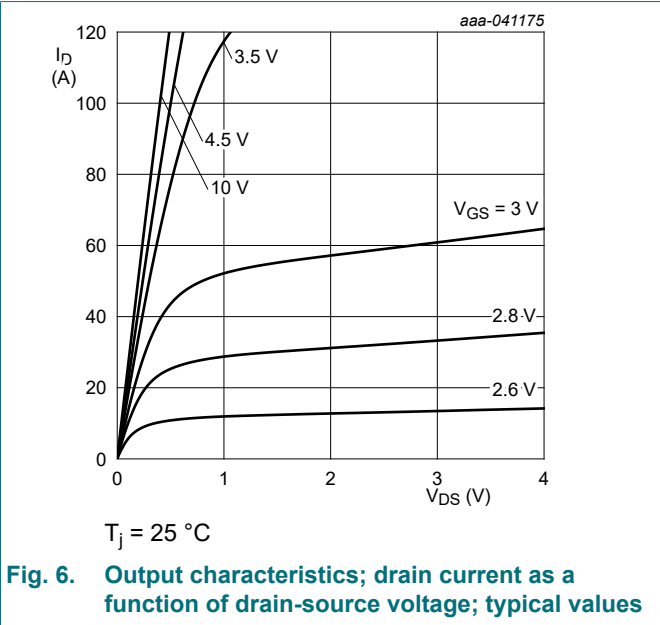


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

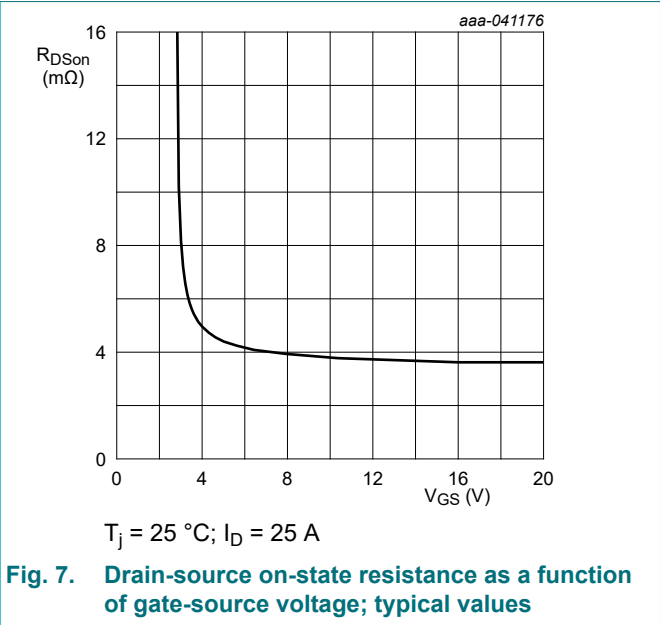


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

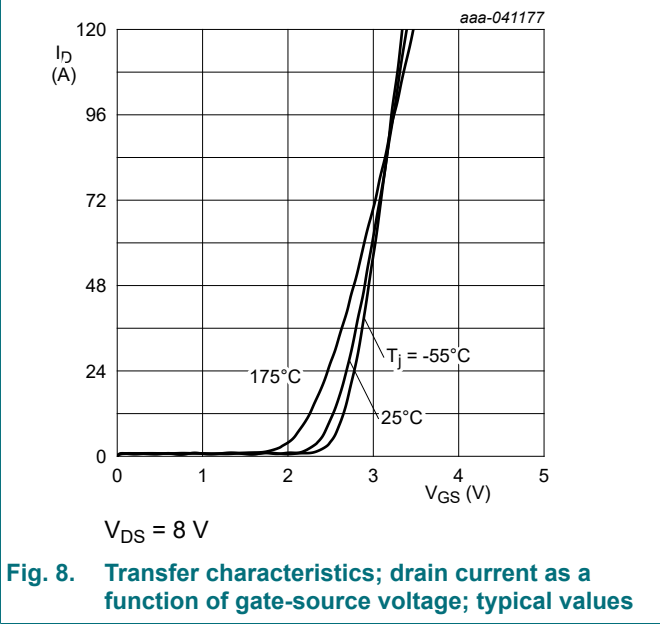


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

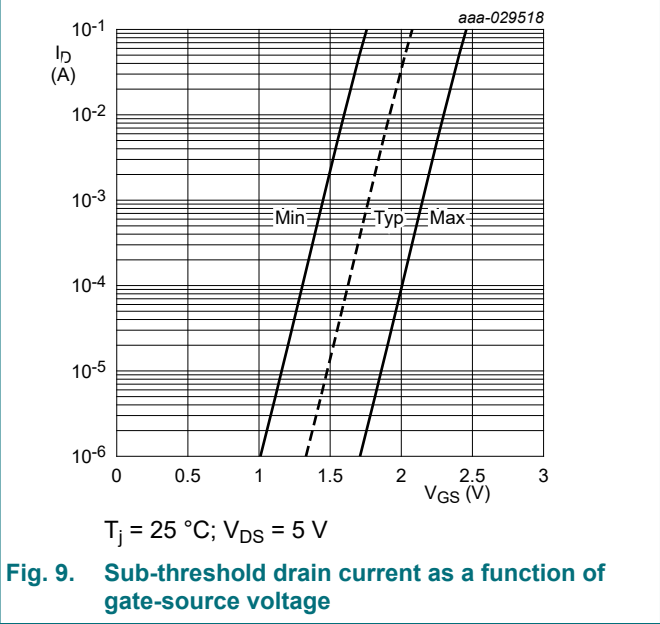


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

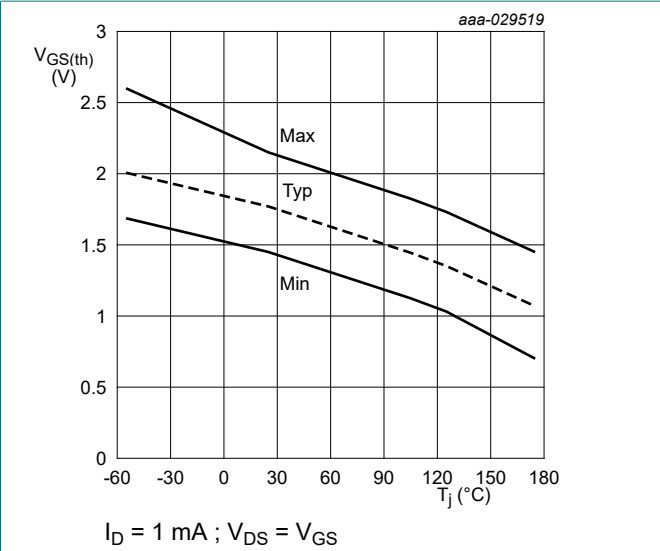


Fig. 10. Gate-source threshold voltage as a function of junction temperature

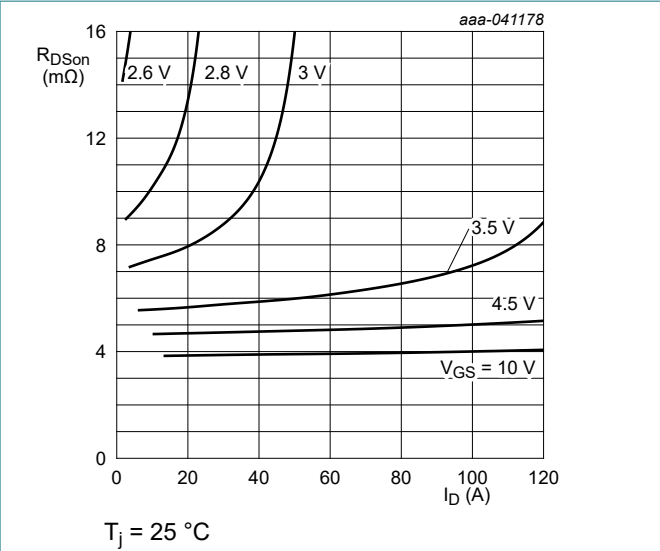


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

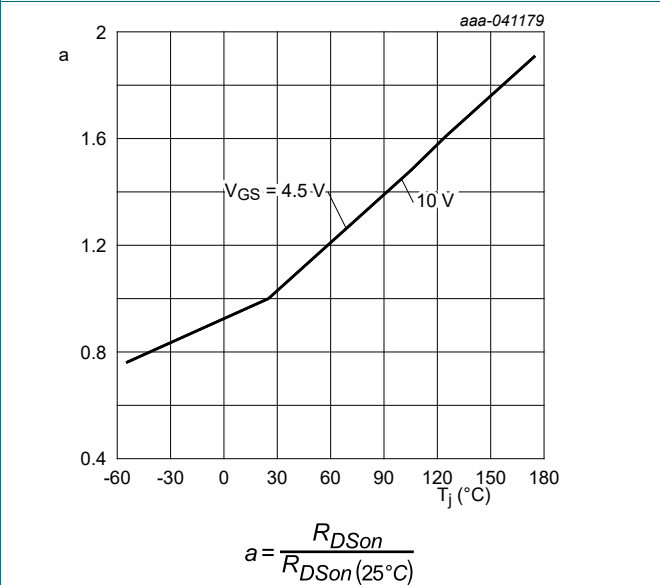


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

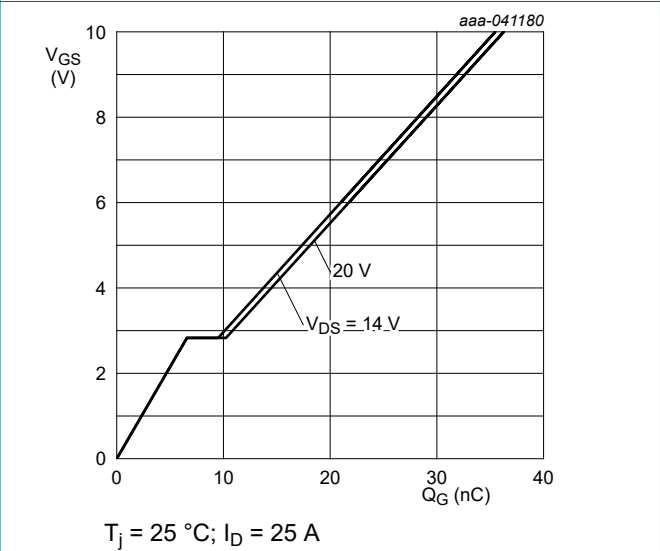


Fig. 13. Gate-source voltage as a function of gate charge; typical values

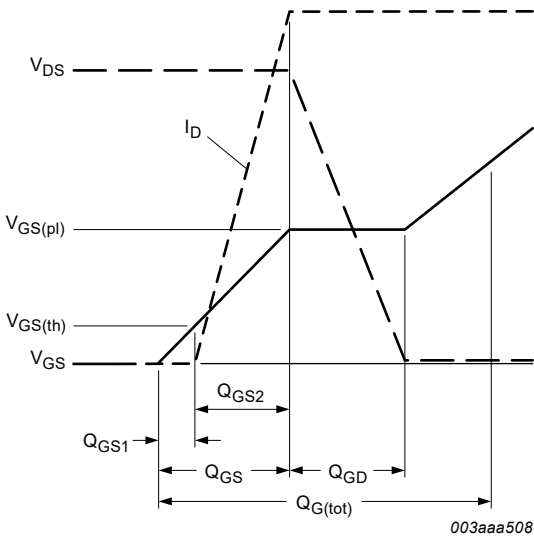


Fig. 14. Gate charge waveform definitions

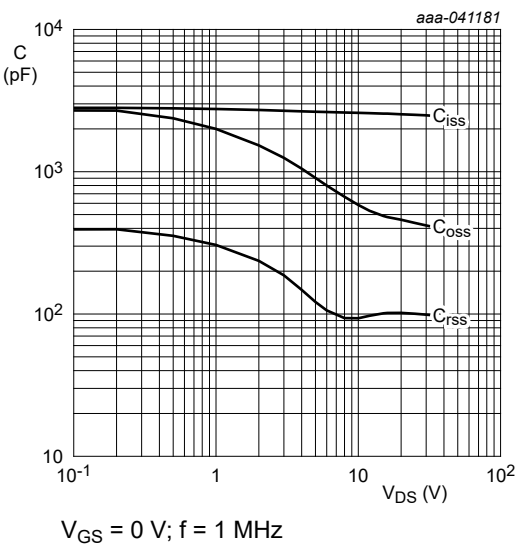


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

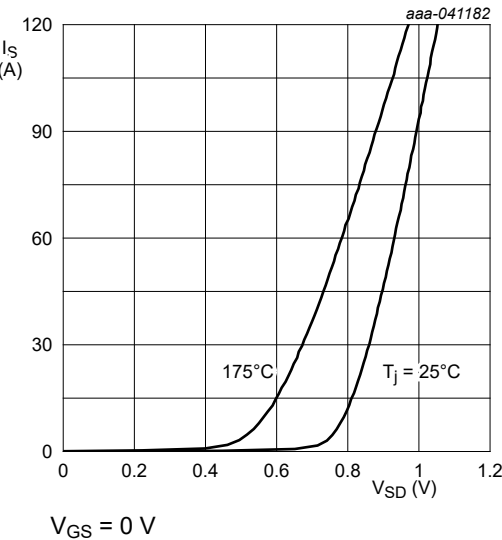


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

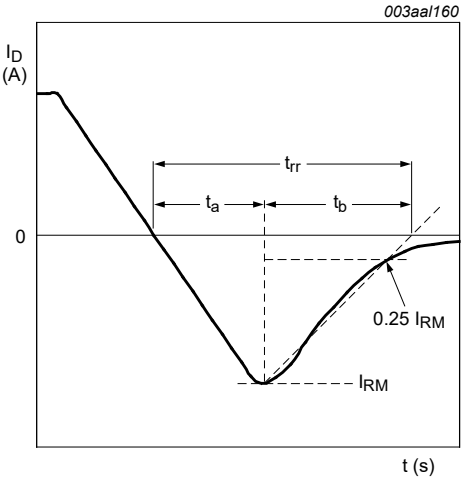


Fig. 17. Reverse recovery timing definition

11. Package outline

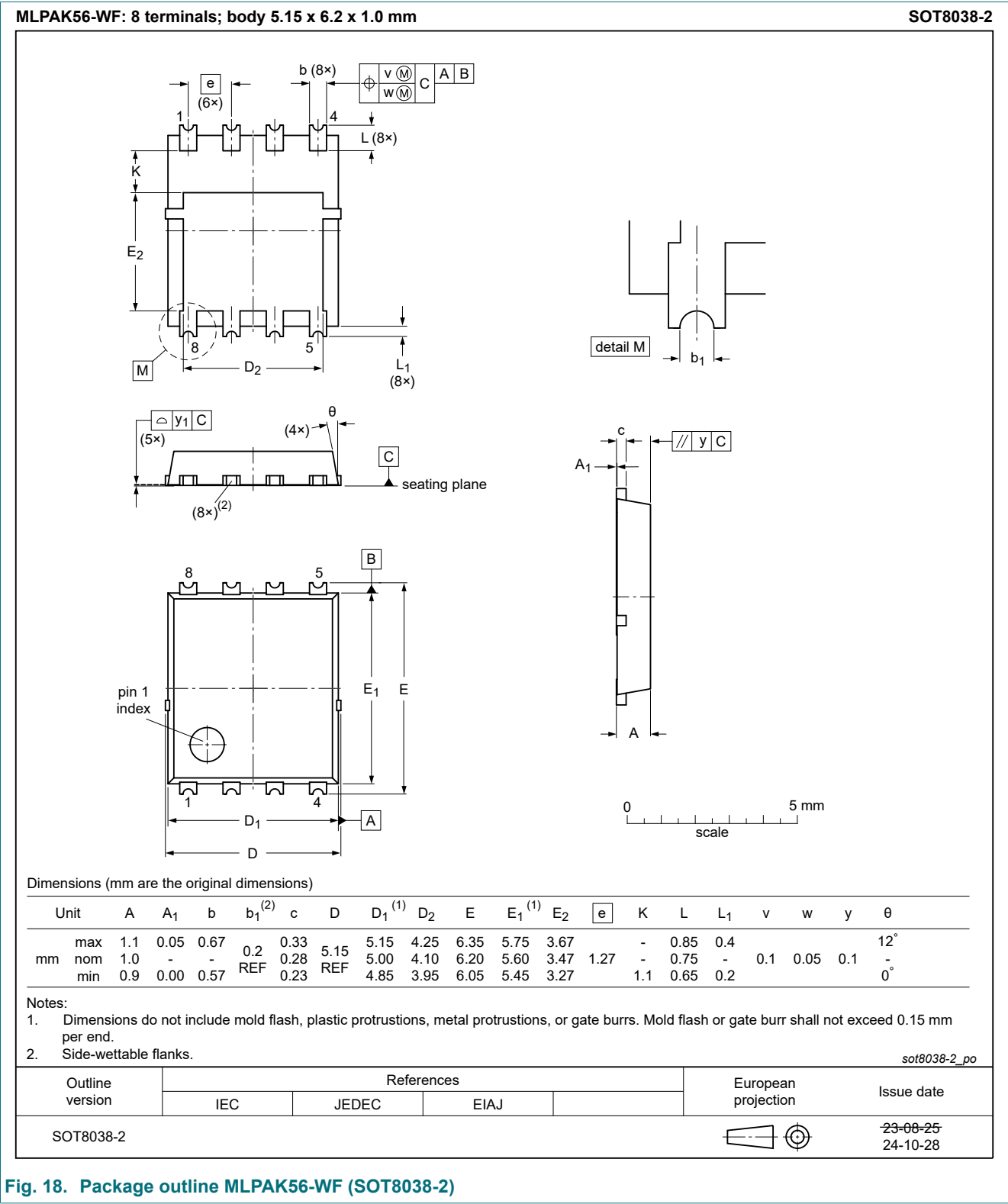


Fig. 18. Package outline MLPAK56-WF (SOT8038-2)

12. Soldering

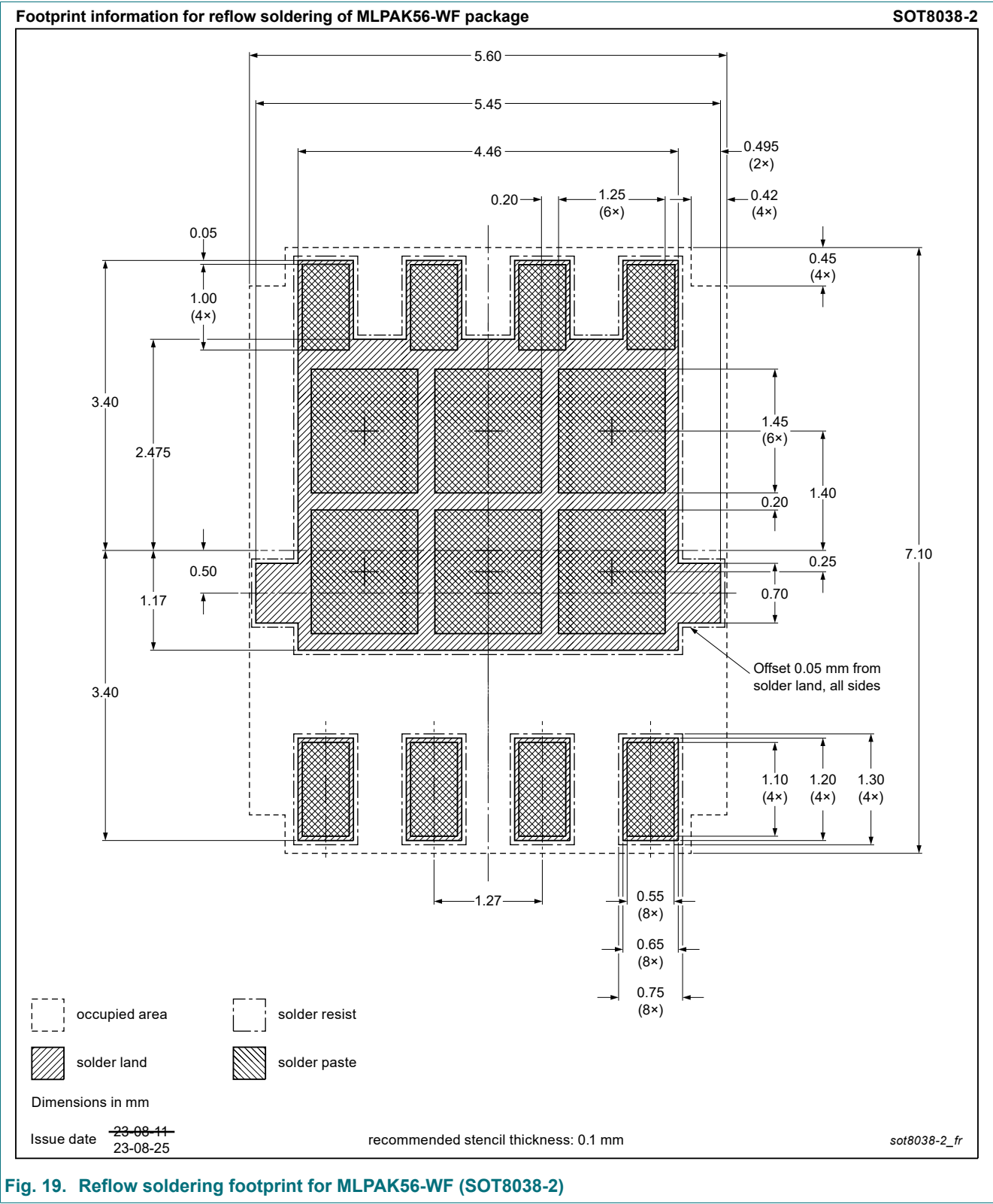


Fig. 19. Reflow soldering footprint for MLPAK56-WF (SOT8038-2)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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