



BUK9M60-100L

N-channel 100 V, 60 mOhm logic level MOSFET in LPAK33

14 January 2025

Product data sheet

1. General description

Logic level N-channel MOSFET in a LPAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Logic level compatible
- Trench 12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Qualified to AEC-Q101 at 175 °C
- Side wettable flanks for robust solder joints and Automated Optical Inspection (AOI)

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- LED lighting/circuit protection

4. Quick reference data

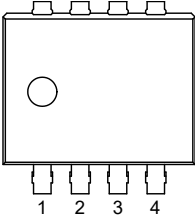
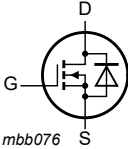
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	19	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	50.4	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		32.5	45.9	60	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		0.6	1.9	4.2	nC

[1] 19 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M60-100L	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M60-100L	9601HL

8. Limiting values

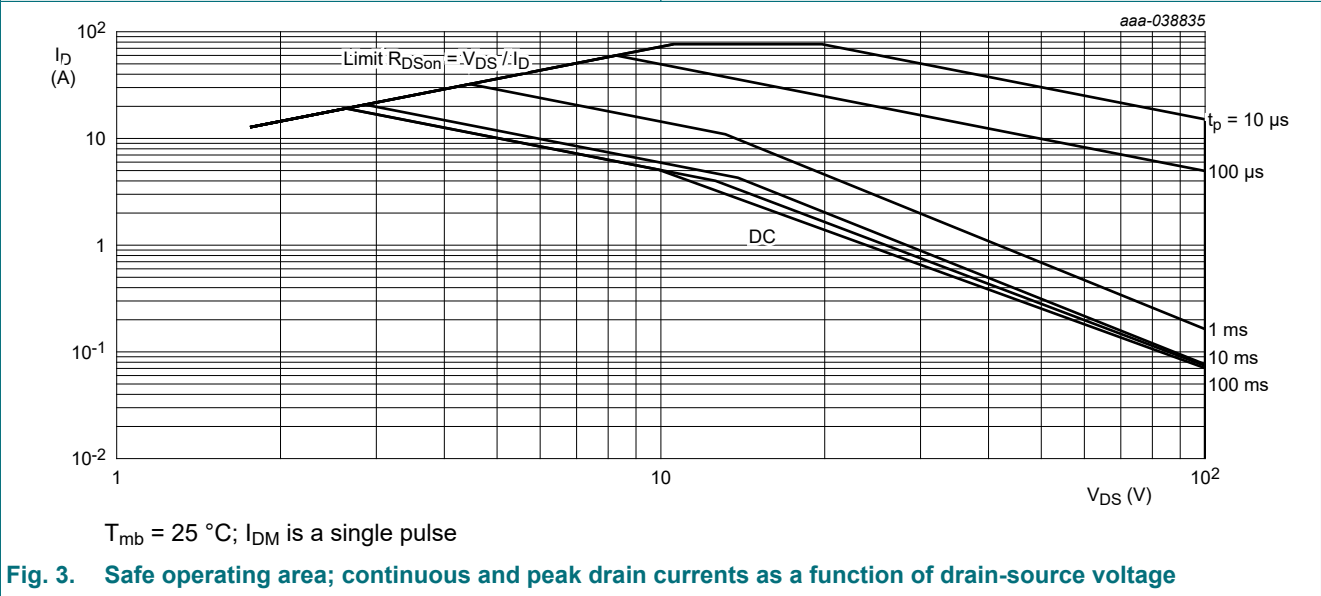
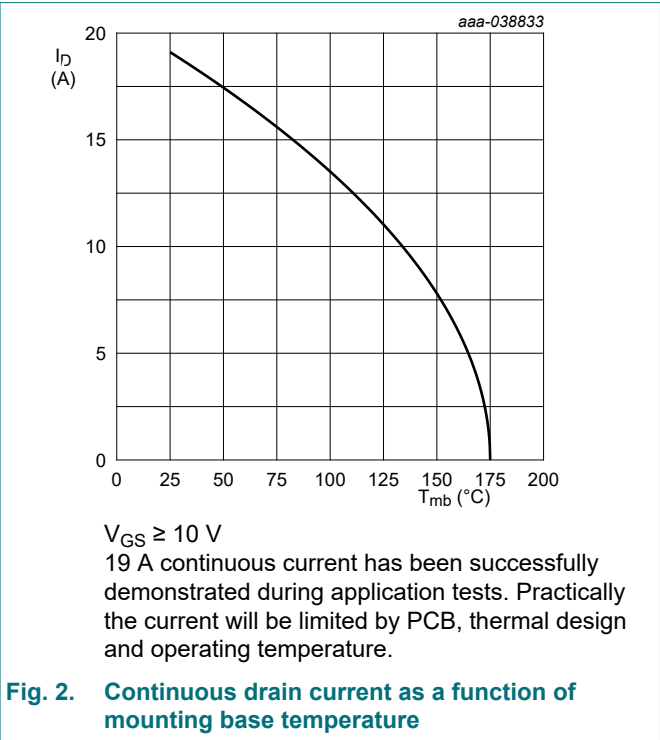
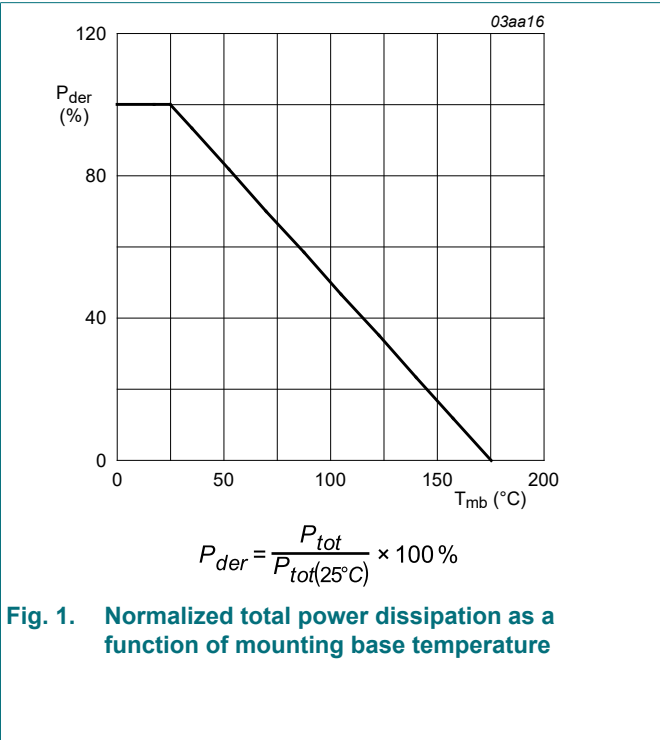
Table 5. Limiting values

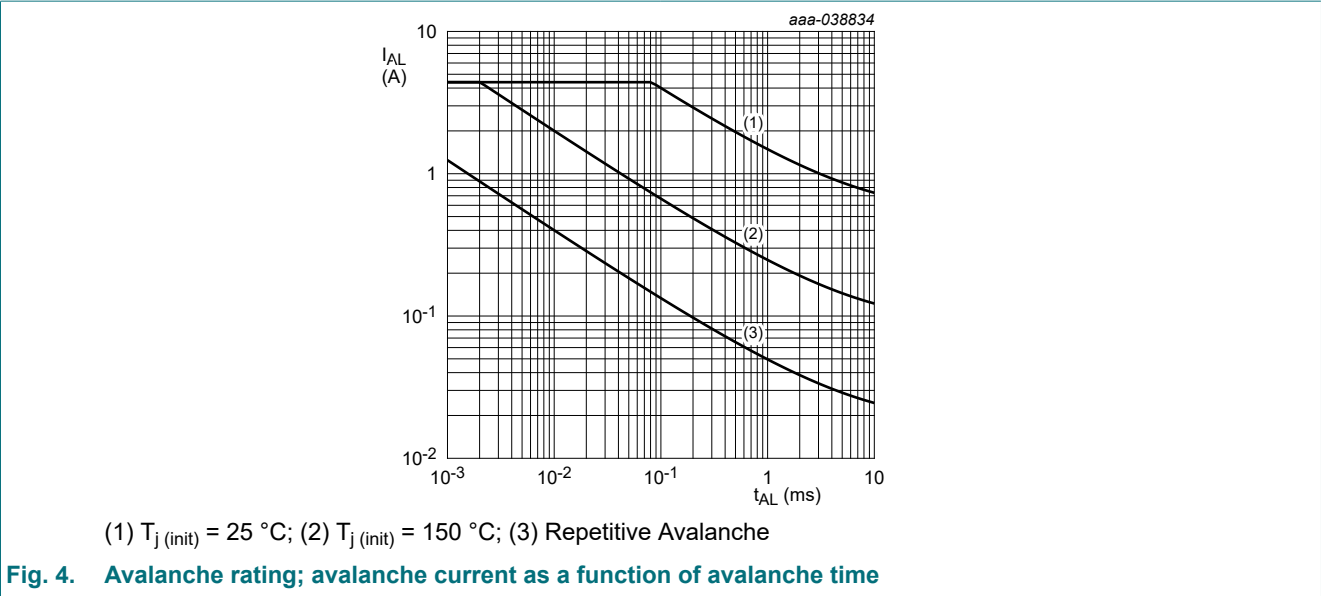
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	100	V
V _{GS}	gate-source voltage		[1]	-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	50.4	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[2]	-	19	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	13.5	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	76	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	19	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	76	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 4.4 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; t _{AL} = 83 μs; Fig. 4	[3] [4]	-	23.5	mJ

Symbol	Parameter	Conditions		Min	Max	Unit
I _{AS}	non-repetitive avalanche current	V _{sup} = 100 V; V _{GS} = 5 V; T _j (init) = 25 °C; R _{GS} = 50 Ω; Fig. 4	[3] [4]	-	4.4	A

- [1] Refer to application note AN90001 for further information.
- [2] 19 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

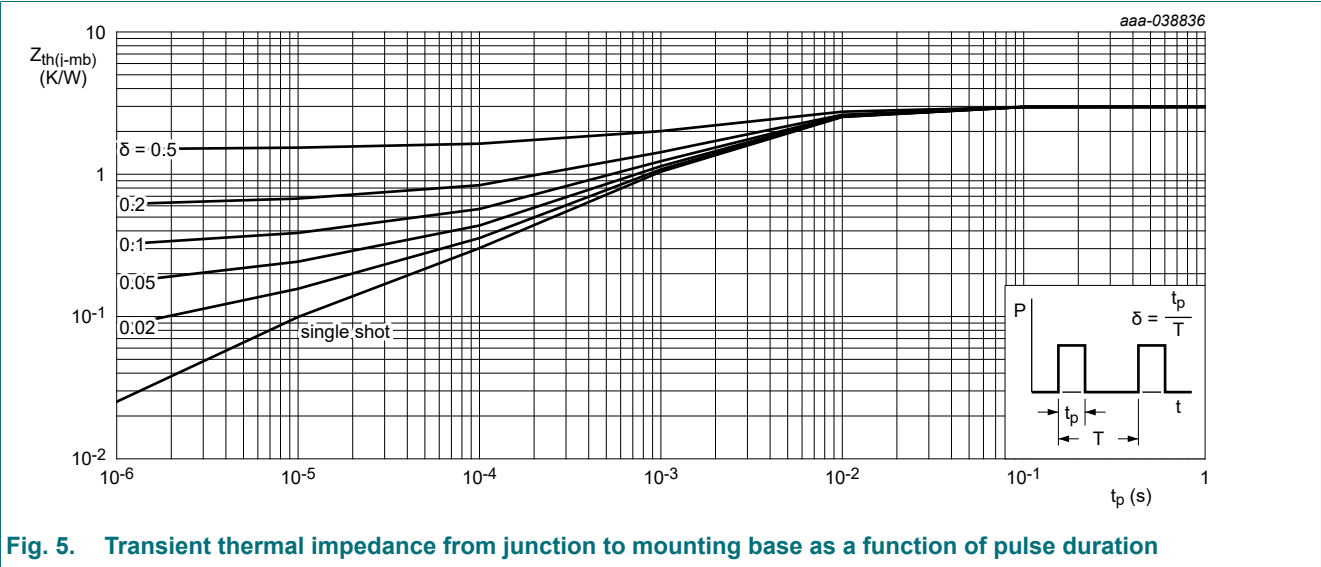




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	2.75	2.98	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	100	117.7	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_J = -40\ ^\circ\text{C}$	92	110	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_J = -55\ ^\circ\text{C}$	90	108.3	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.03\ \text{mA}$; $V_{DS}=V_{GS}$; $T_J = 25\ ^\circ\text{C}$; Fig. 9 ; Fig. 10	1.4	1.7	2.05	V
		$I_D = 0.03\ \text{mA}$; $V_{DS}=V_{GS}$; $T_J = 175\ ^\circ\text{C}$; Fig. 10	0.5	-	-	V
		$I_D = 0.03\ \text{mA}$; $V_{DS}=V_{GS}$; $T_J = -55\ ^\circ\text{C}$; Fig. 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 100\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	-	0.005	1	μA
		$V_{DS} = 100\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_J = 125\ ^\circ\text{C}$	-	0.5	100	μA
		$V_{DS} = 100\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_J = 175\ ^\circ\text{C}$	-	20	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 25\ ^\circ\text{C}$; Fig. 11	32.5	45.9	60	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 100\ ^\circ\text{C}$; Fig. 12	47.8	70.6	96.4	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 125\ ^\circ\text{C}$; Fig. 12	51.2	77.6	106.6	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 175\ ^\circ\text{C}$; Fig. 12	63.4	97.3	137.3	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 25\ ^\circ\text{C}$; Fig. 11	41.6	60.6	89.2	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 100\ ^\circ\text{C}$; Fig. 12	61.2	93.3	143.3	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 125\ ^\circ\text{C}$; Fig. 12	66.7	102.5	158.5	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 5\ \text{A}$; $T_J = 175\ ^\circ\text{C}$; Fig. 12	81.2	128.5	204	m Ω
R_G	gate resistance	$f = 1\ \text{MHz}$; $T_J = 25\ ^\circ\text{C}$	0.9	1.7	3.4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5\ \text{A}$; $V_{DS} = 50\ \text{V}$; $V_{GS} = 5\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	3.2	6.5	9.8	nC
		$I_D = 5\ \text{A}$; $V_{DS} = 50\ \text{V}$; $V_{GS} = 10\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	6	12	18	nC
Q_{GS}	gate-source charge	$I_D = 5\ \text{A}$; $V_{DS} = 50\ \text{V}$; $V_{GS} = 5\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	1.4	2.3	3.2	nC
Q_{GD}	gate-drain charge	$T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	0.6	1.9	4.2	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5\ \text{A}$; $V_{DS} = 80\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	-	2.9	-	V
C_{iss}	input capacitance	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_J = 25\ ^\circ\text{C}$; Fig. 15	439	731	1023	pF
C_{oss}	output capacitance		123	205	328	pF
C_{rss}	reverse transfer capacitance		9.6	24	36.4	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 80 V; R _L = 16 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6.4	-	ns
t _r	rise time			-	7.3	-	ns
t _{d(off)}	turn-off delay time			-	9.1	-	ns
t _f	fall time			-	7.1	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.88	1	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;		-	39	-	ns
Q _r	recovered charge	V _{DS} = 50 V; T _j = 25 °C; Fig. 17		-	23	-	nC

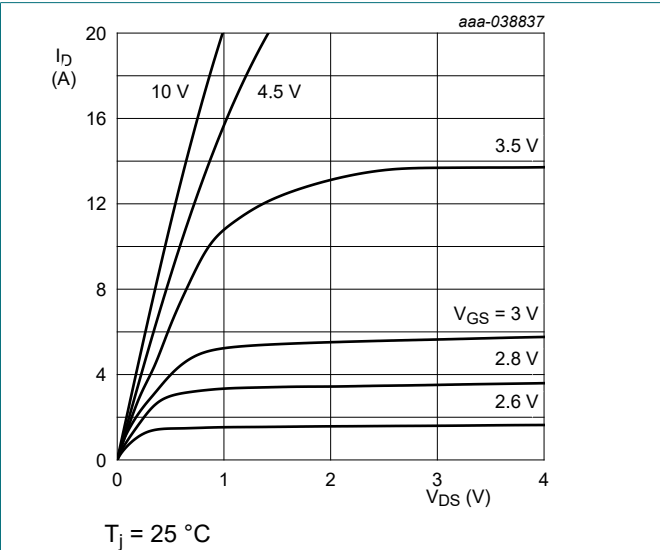


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

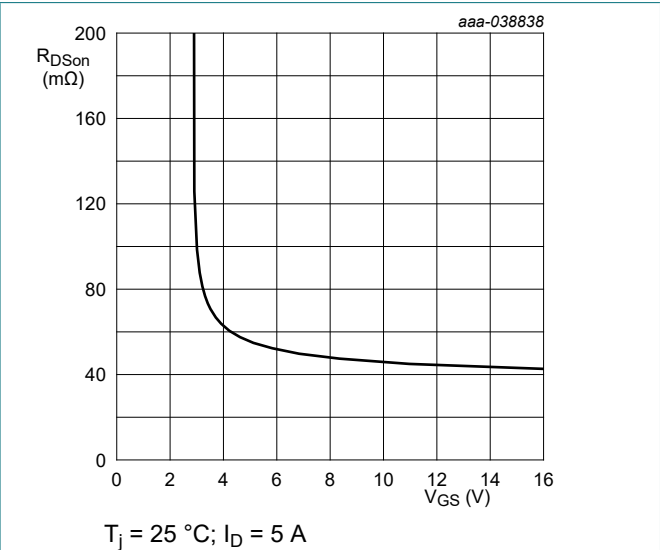


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

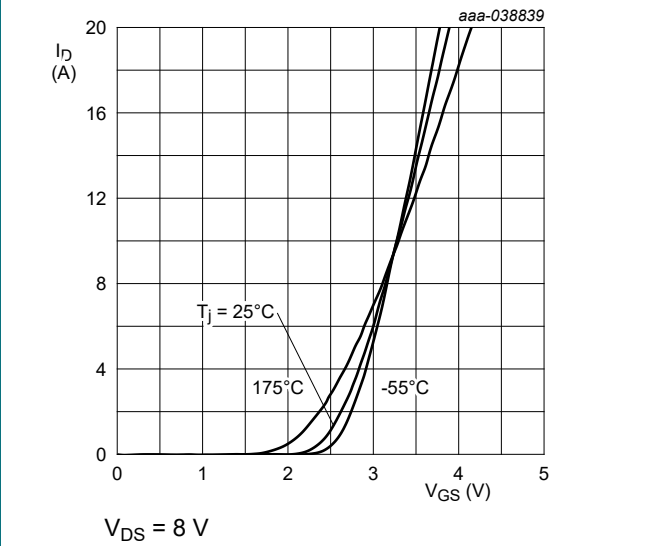


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

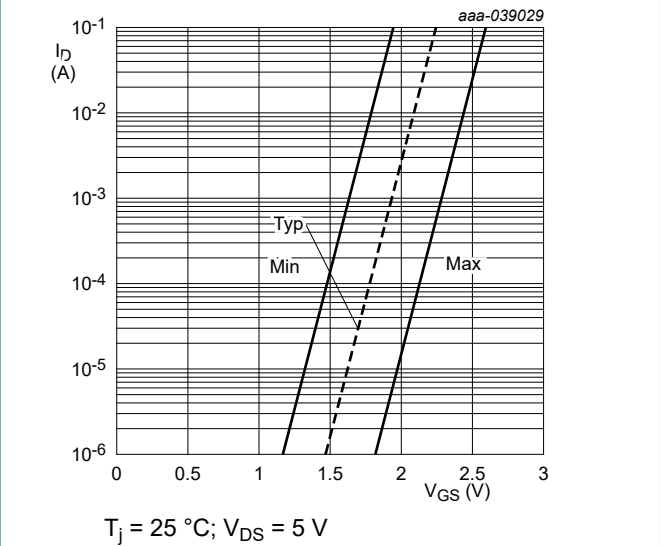


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

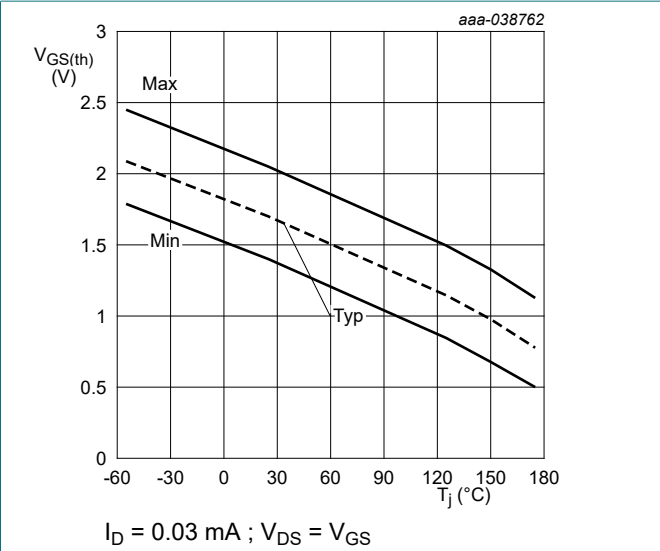


Fig. 10. Gate-source threshold voltage as a function of junction temperature

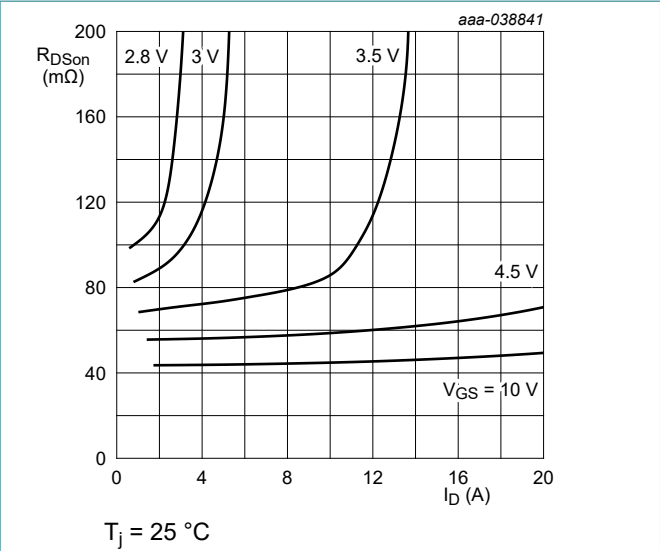


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

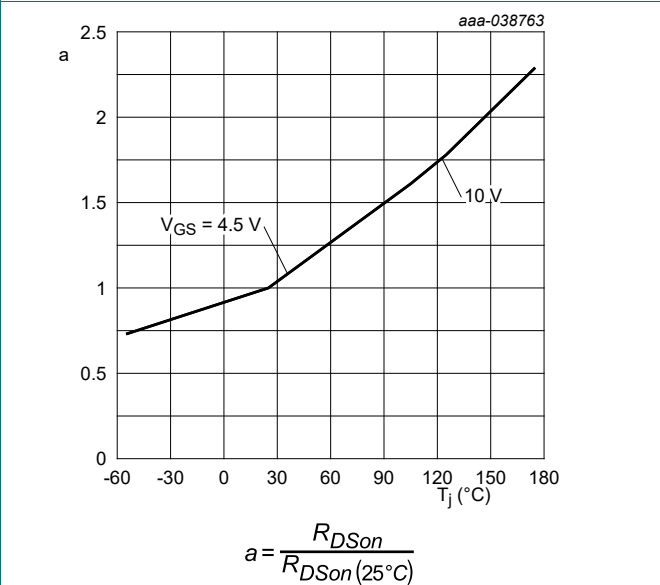


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

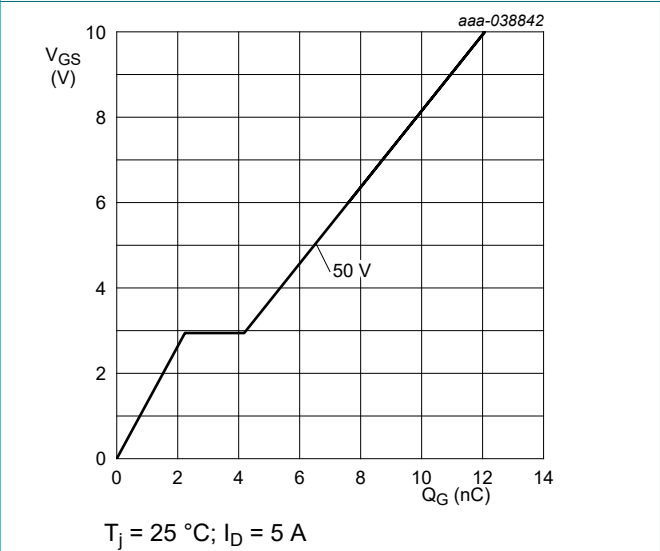


Fig. 13. Gate-source voltage as a function of gate charge; typical values



Fig. 14. Gate charge waveform definitions

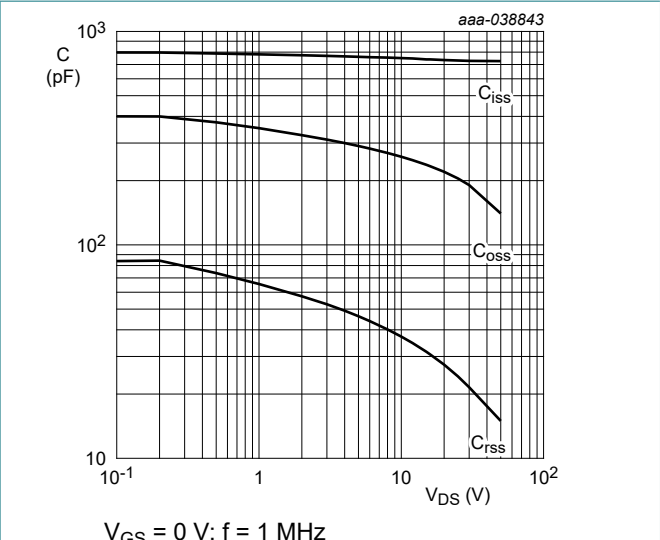


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

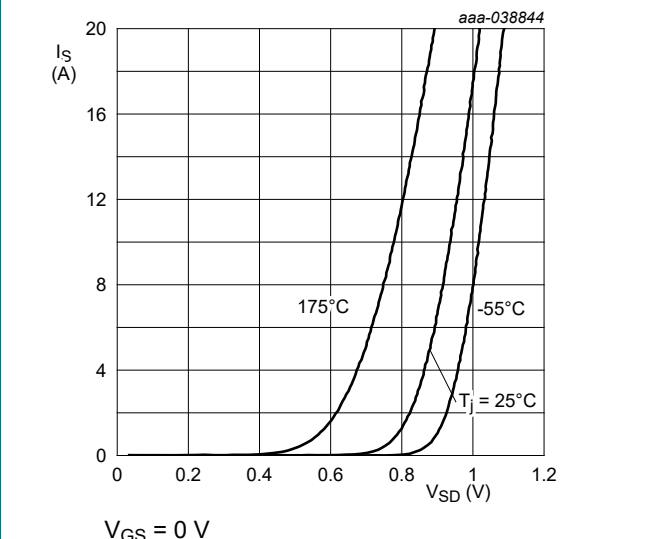


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

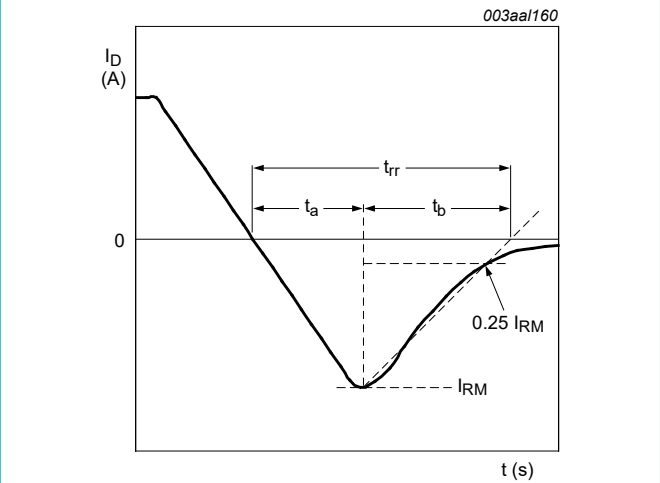


Fig. 17. Reverse recovery timing definition

11. Package outline

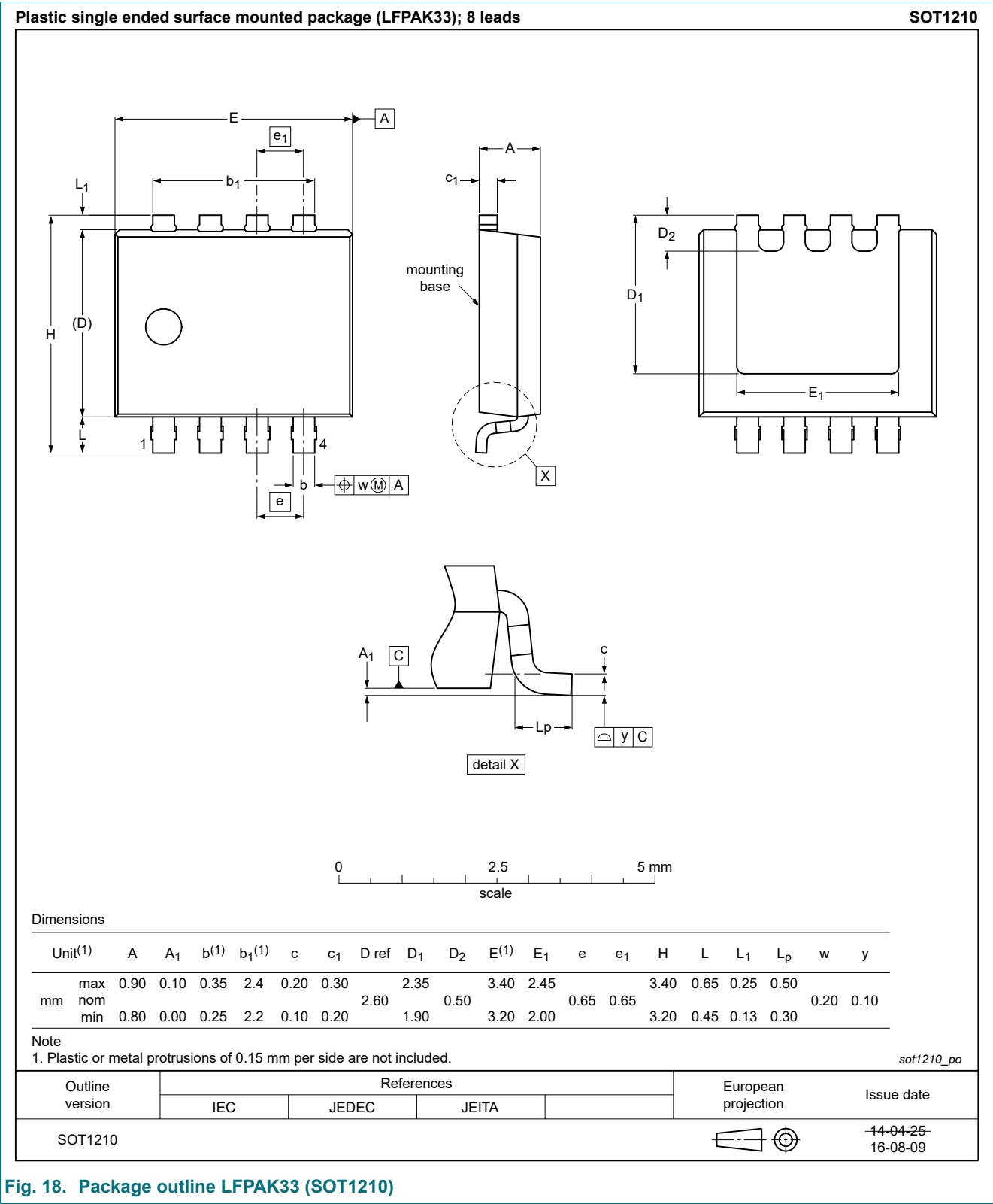


Fig. 18. Package outline LPAK33 (SOT1210)

12. Soldering

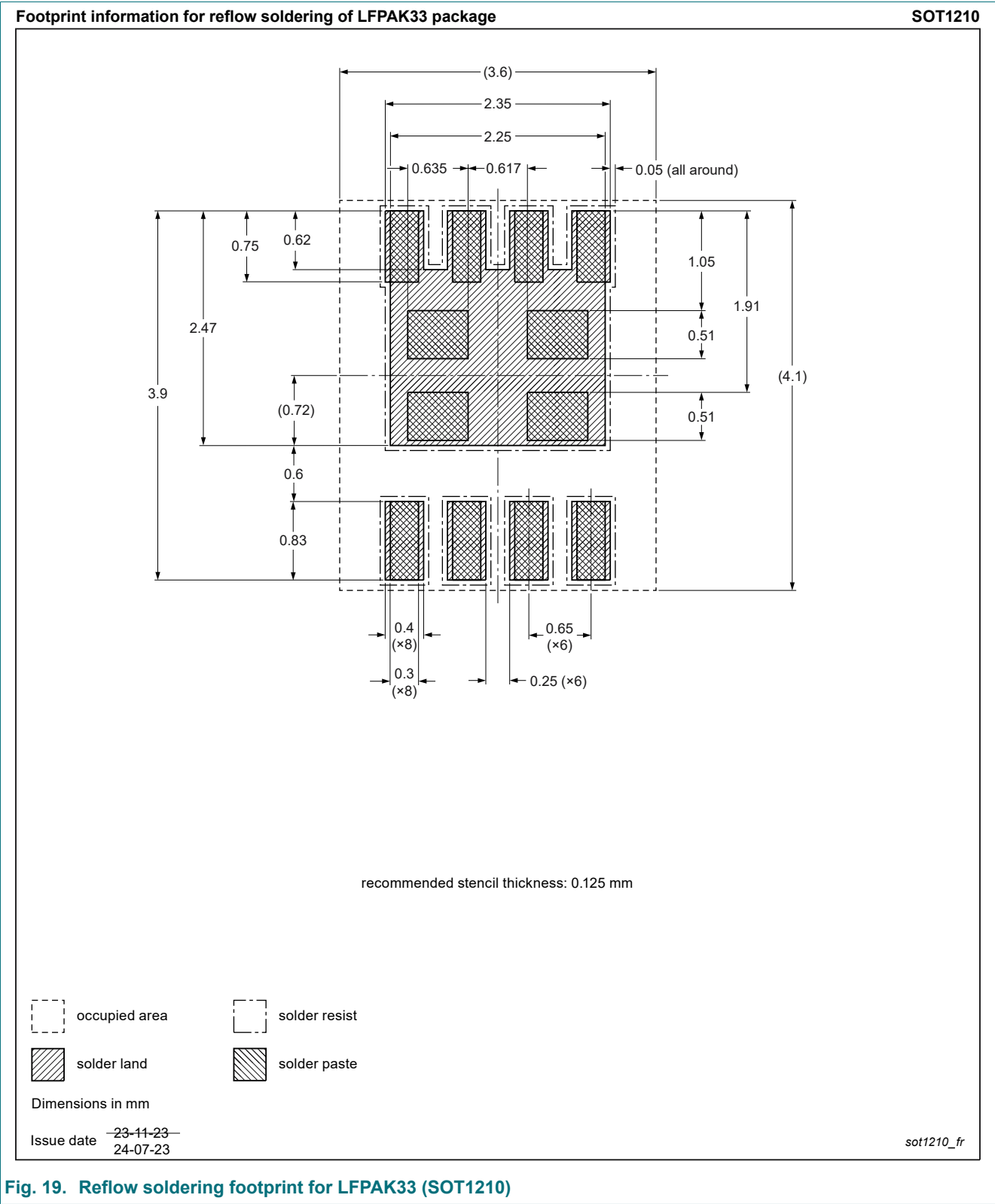


Fig. 19. Reflow soldering footprint for LPAK33 (SOT1210)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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