



PSMN1R4-100ASE

N-channel, 100 V, 1.36 mOhm, MOSFET with enhanced SOA in CCPAK1212 package

20 October 2025

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a CCPAK1212 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN1R4-100ASE delivers very low $R_{DS(on)}$ and enhanced safe operating area performance in a high-reliability copper-clip package (CCPAK1212).

PSMN1R4-100ASE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low $R_{DS(on)}$ to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DS(on)}$ for low I^2R conduction losses
- CCPAK1212 package for applications that demand the highest performance and reliability
- CCPAK1212 is JEDEC listed package for open market and 2nd source compatibility

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

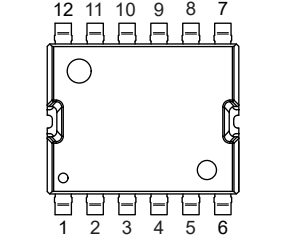
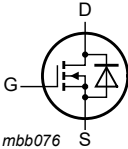
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	340	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	935	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	1.07	1.36	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	122	244	366	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/μs}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17	-	84	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 CCPAK1212 (SOT8000A)	 mbb076
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R4-100ASE	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A

7. Marking

Table 4. Marking codes

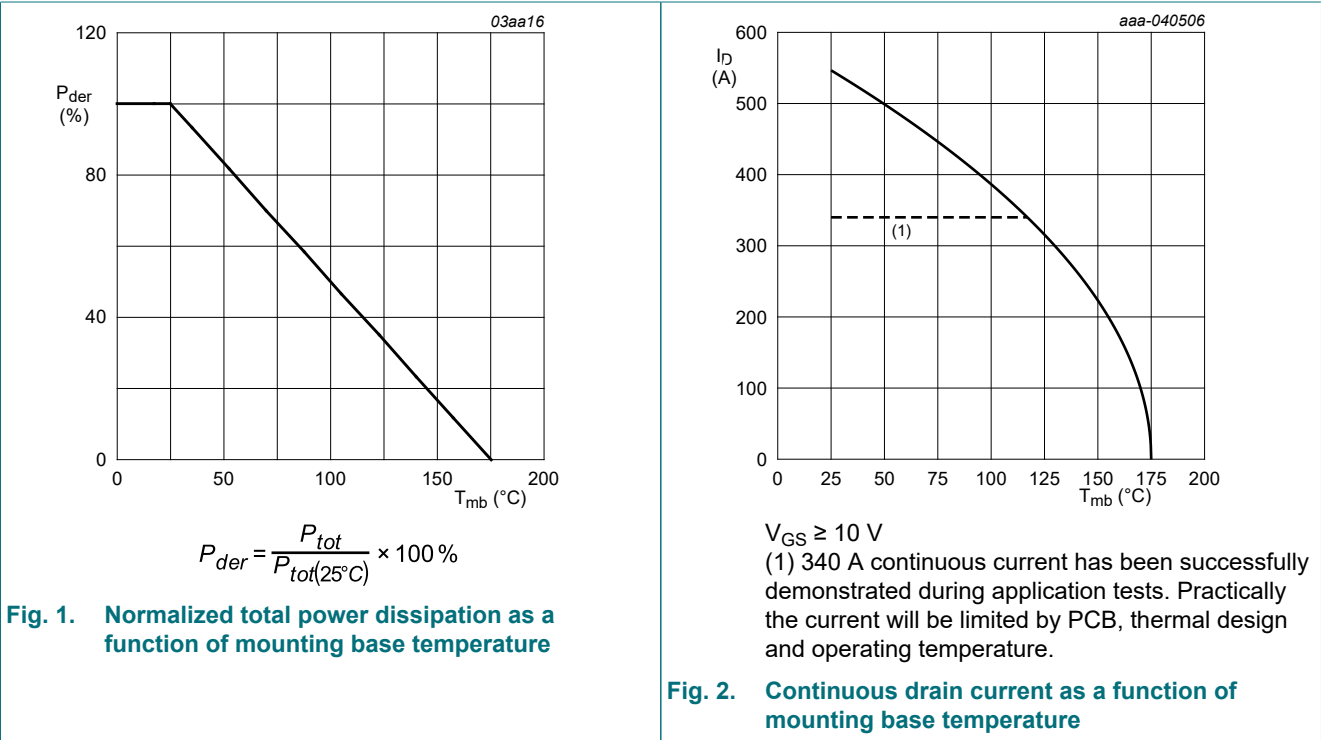
Type number	Marking code
PSMN1R4-100ASE	XP1E4S10A

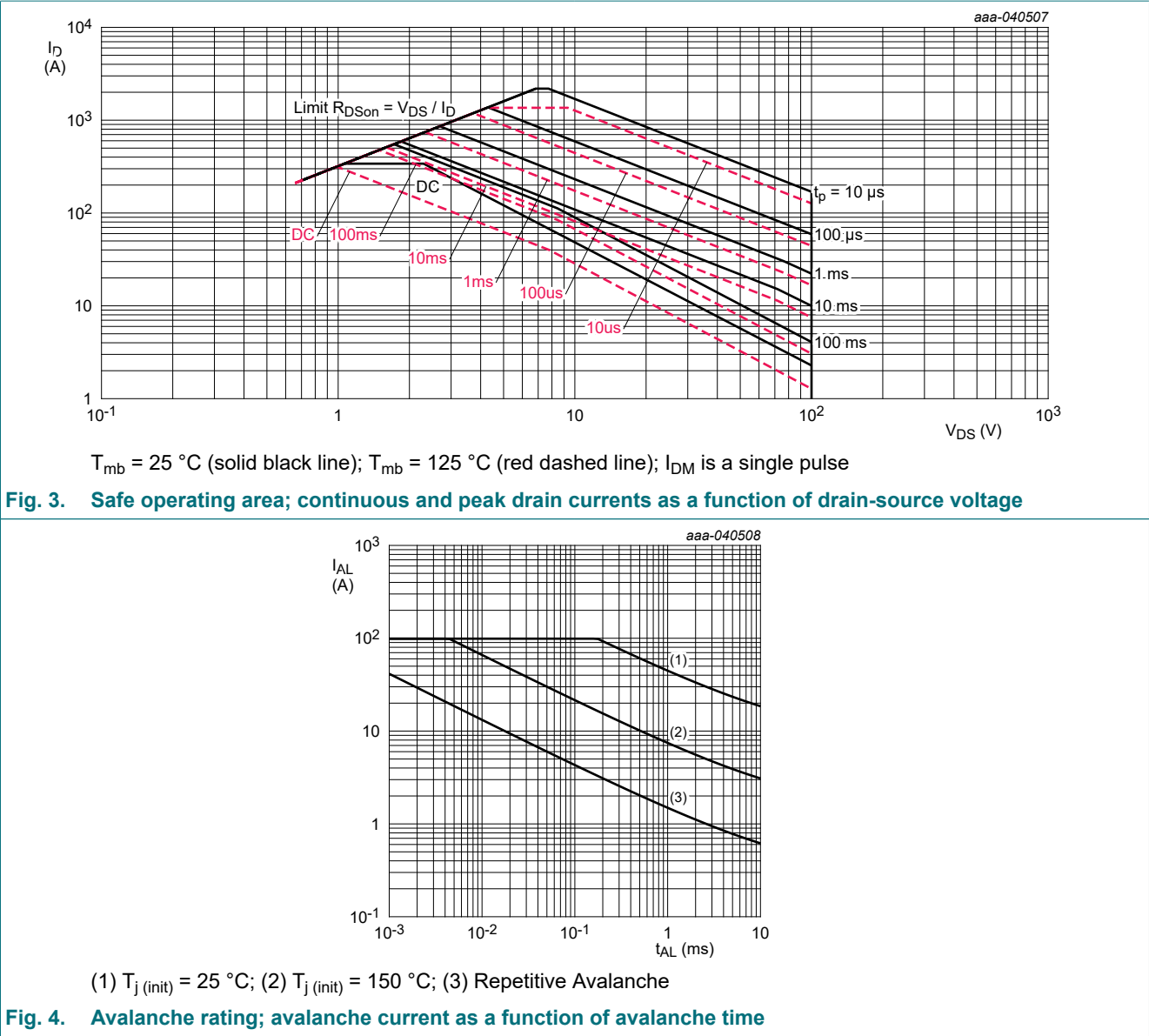
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	935	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	340	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	340	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	2186	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	340	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	2186	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 98.95 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 175 μs; Fig. 4	[1]	-	1130	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	98.95	A

[1] Protected by 100% test





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.123	0.16	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	58	-	K/W
		Fig. 7	-	29	-	K/W

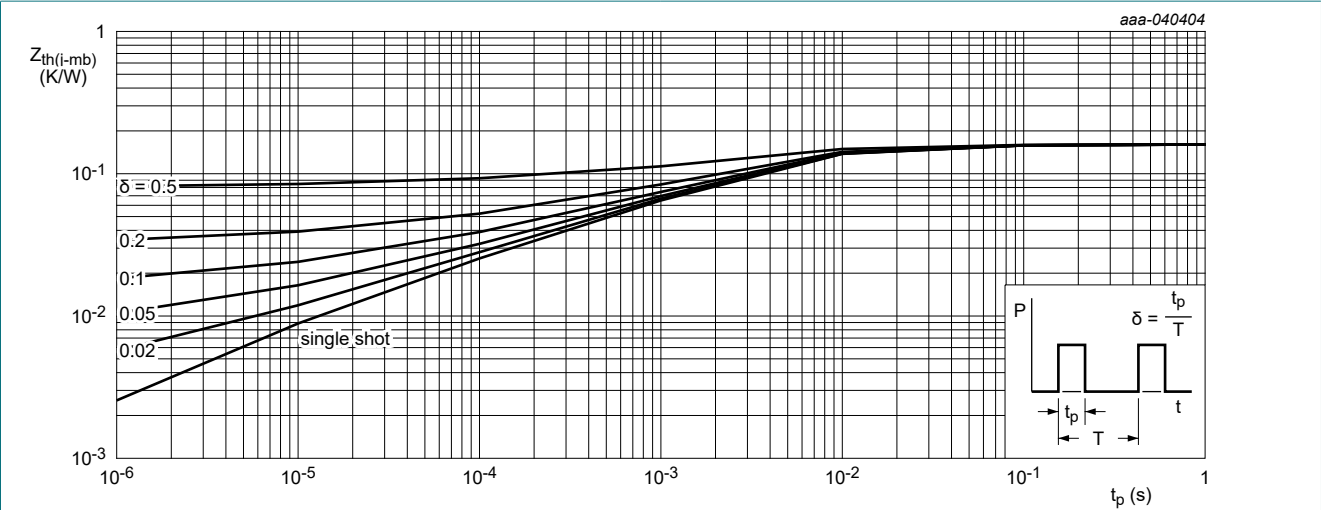


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

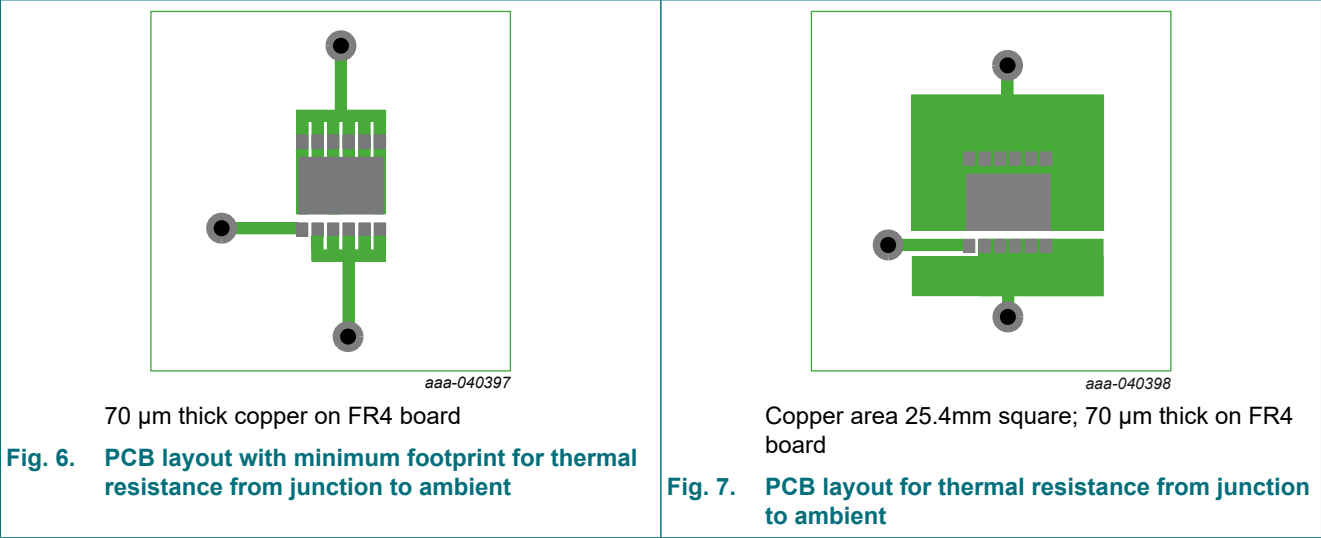


Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

Fig. 7. PCB layout for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C		2	2.64	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C		-	1.6	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C		-	3	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C		-	-6.55	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C		-	0.1	1.6	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C		-	34	160	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11		-	1.07	1.36	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 12		-	1.8	2.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12		-	2.6	3.1	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.5	1.01	2.01	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13 ; Fig. 14		122	244	366	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	218	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13 ; Fig. 14		49	81.5	114	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	53	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	29	-	nC
Q _{GD}	gate-drain charge			11	36.5	84	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 13 ; Fig. 14		-	4.5	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 0.5 MHz; T _j = 25 °C; Fig. 15		11153	18588	26023	pF
C _{oss}	output capacitance			2453	4089	6542	pF
C _{rss}	reverse transfer capacitance			11	115	299	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	65	-	ns
t _r	rise time			-	66	-	ns
t _{d(off)}	turn-off delay time			-	142	-	ns
t _f	fall time			-	86	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.77	1	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	62	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17		-	84	-	nC

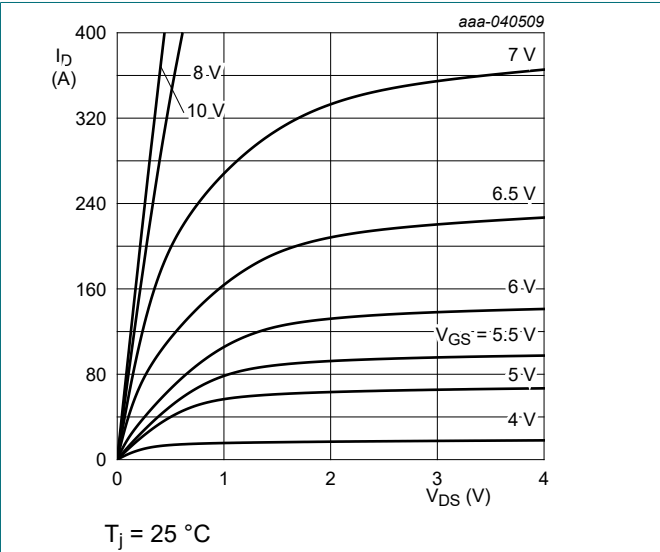


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

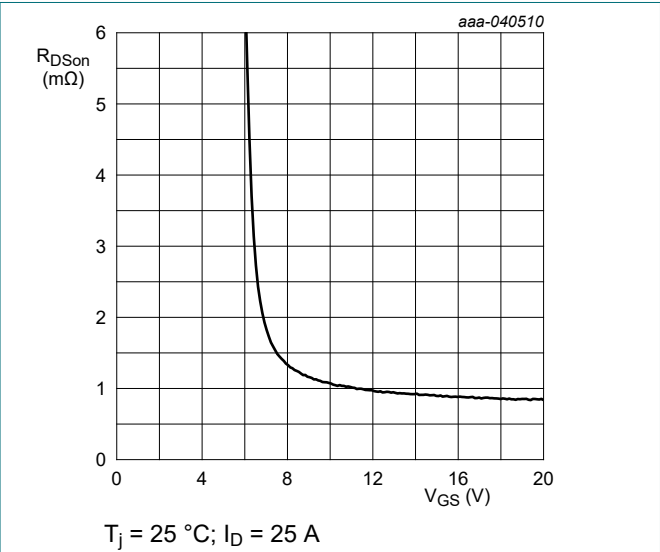


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

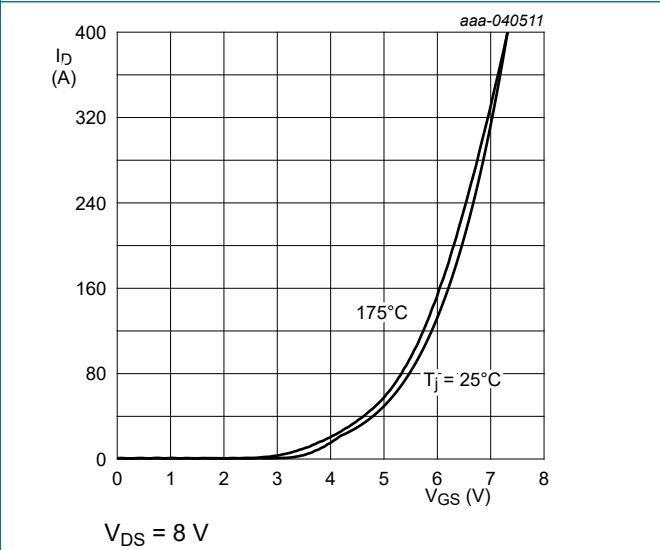


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

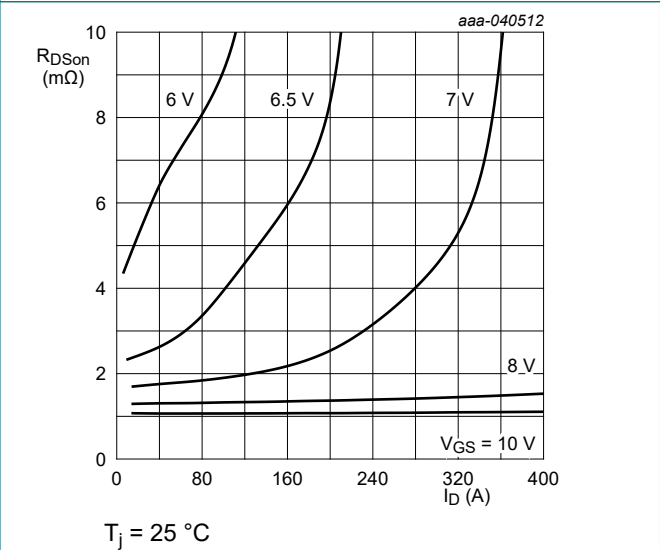


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

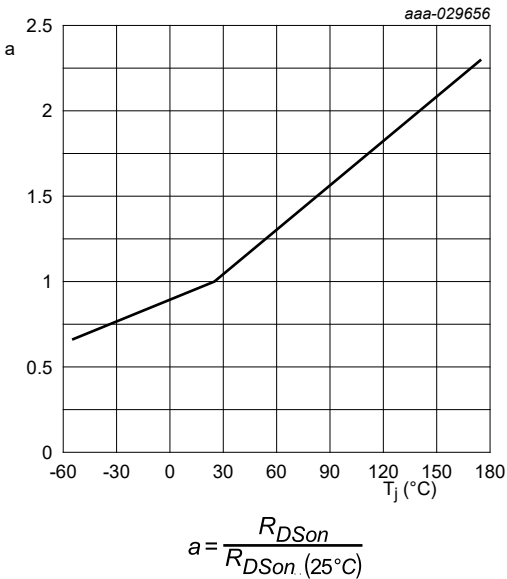


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

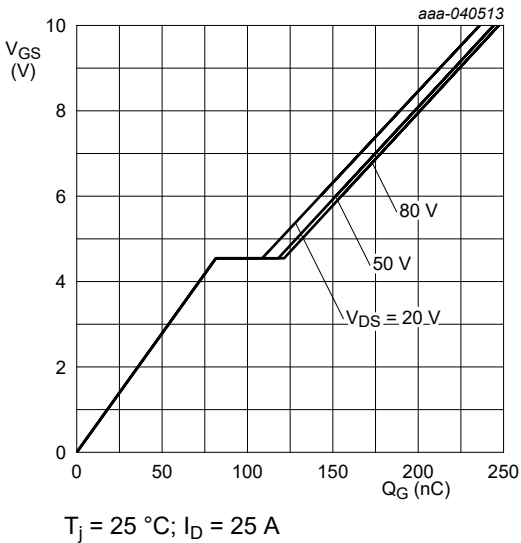


Fig. 13. Gate-source voltage as a function of gate charge; typical values

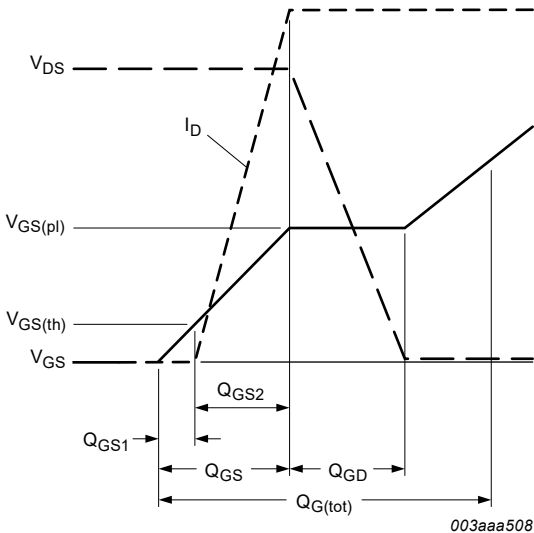


Fig. 14. Gate charge waveform definitions

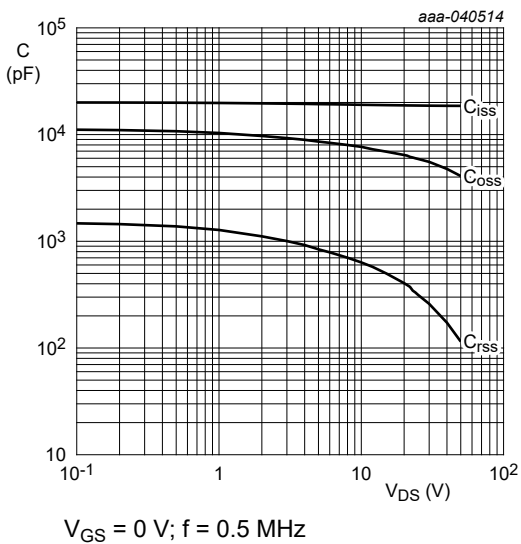
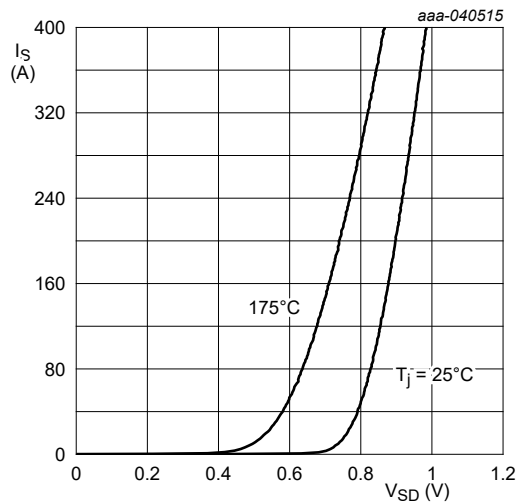


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

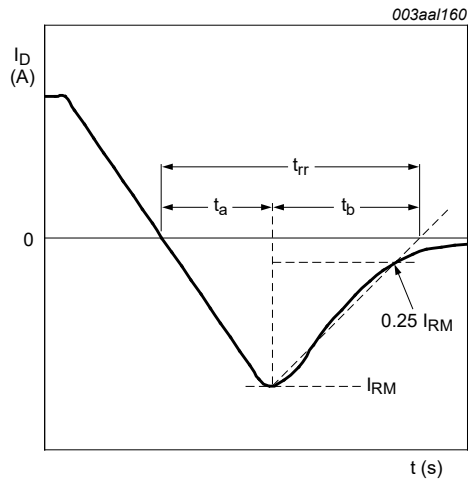


Fig. 17. Reverse recovery timing definition

11. Package outline

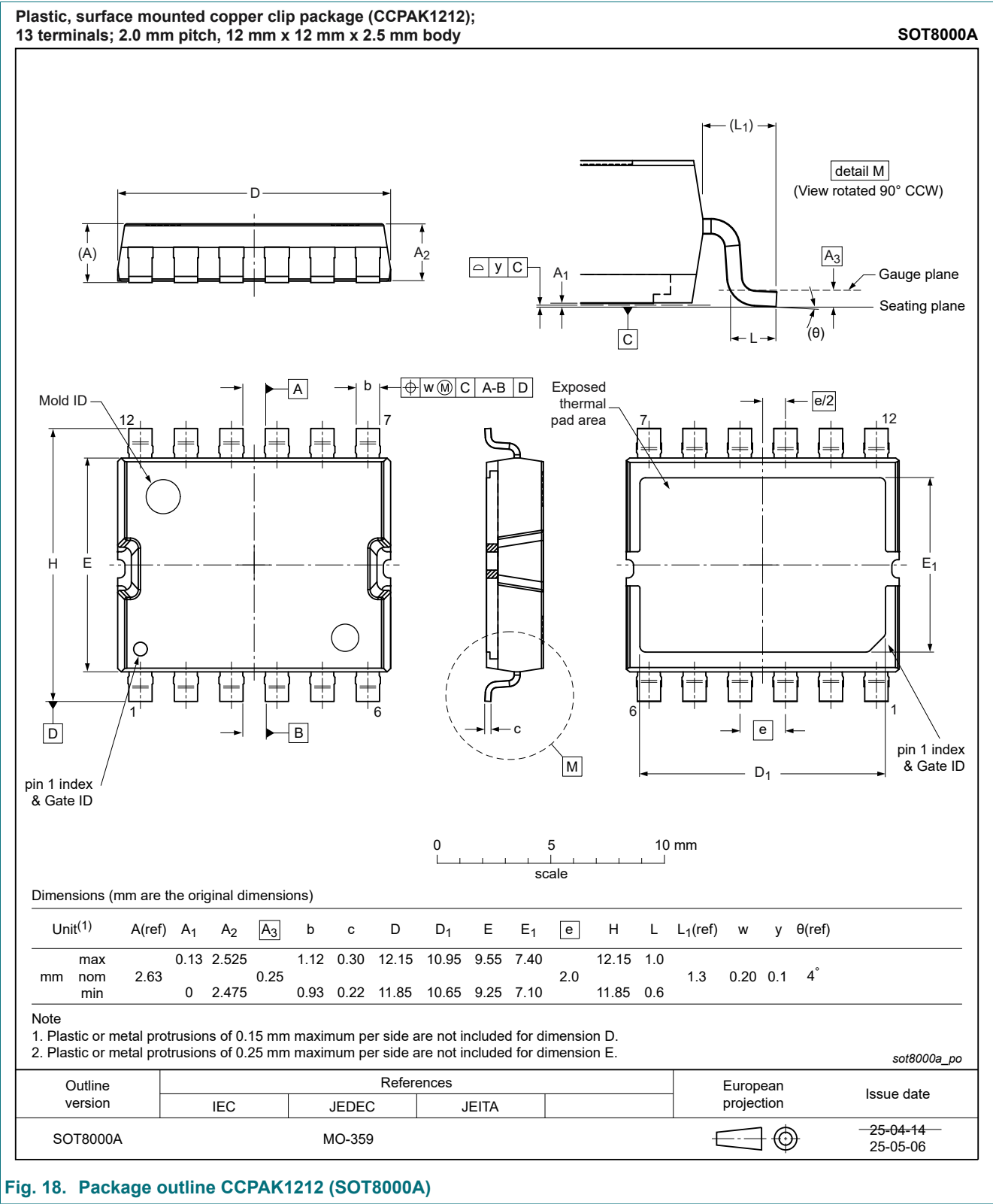
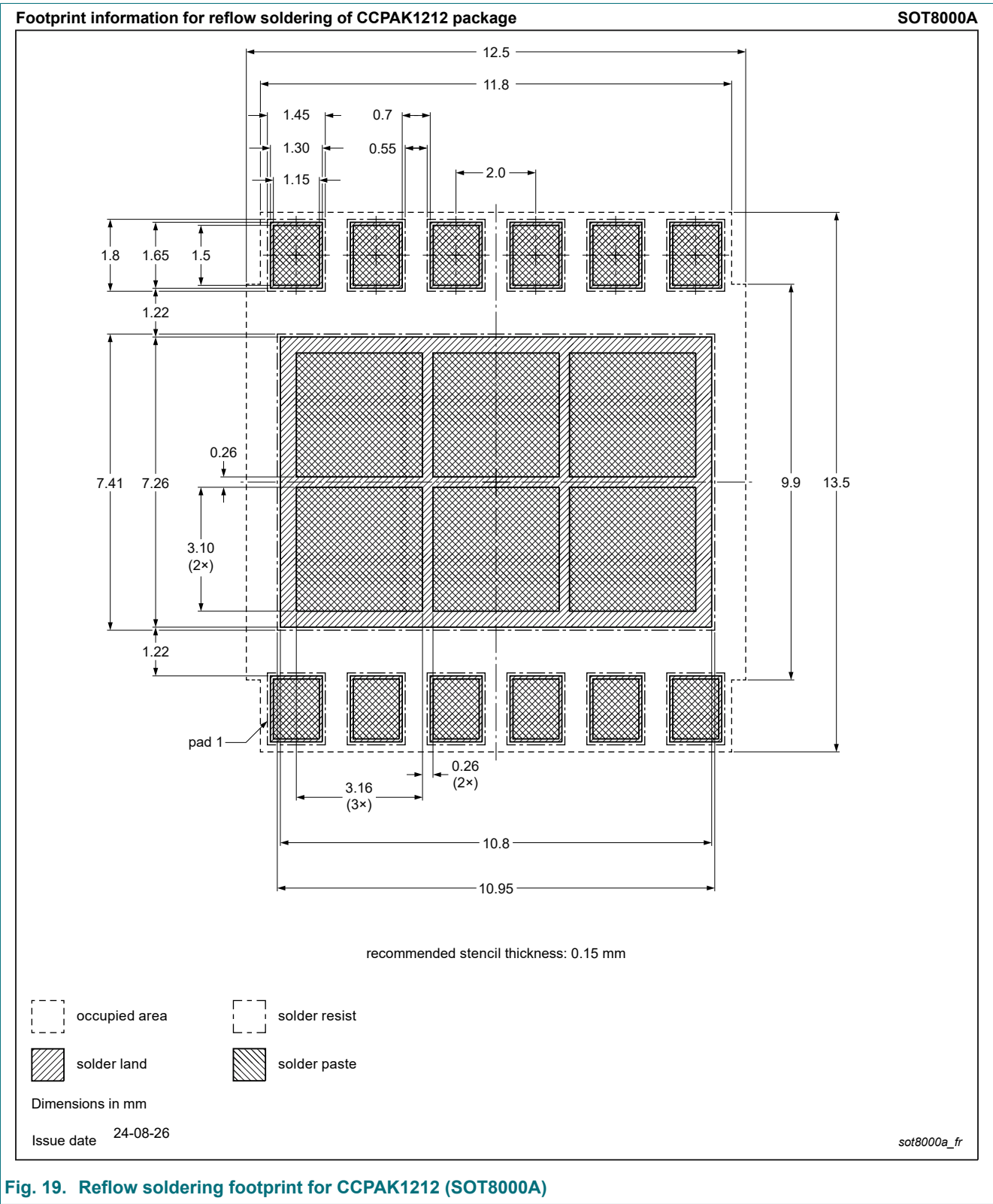


Fig. 18. Package outline CCPAK1212 (SOT8000A)

12. Soldering



13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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