



PSMN1R3-100ASF

NextPower 100 V, 1.3 mOhm, N-channel MOSFET in
CCPAK1212 package

20 October 2025

Product data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for high power industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 355 Amps $I_{D(max)}$ continuous current rating
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant CCPAK1212 package
- CCPAK1212 is JEDEC listed package for open market and 2nd source compatibility

3. Applications

- Battery protection
- High power full and half-bridge configurations
- BLDC motor control
- OR-ing

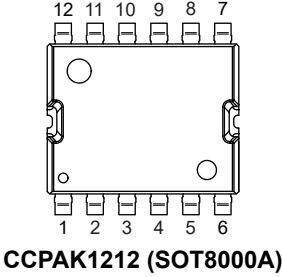
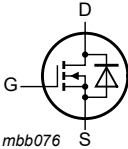
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	355	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	935	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	1.02	1.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	14	46	106	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/μs}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17	-	74	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 CCPAK1212 (SOT8000A)	 mbb076
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R3-100ASF	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R3-100ASF	XP1F3S10A

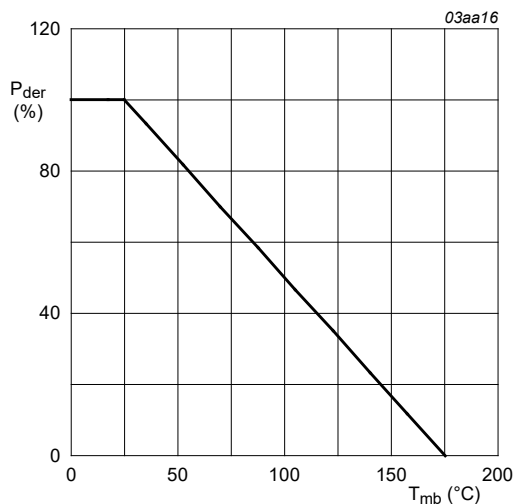
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

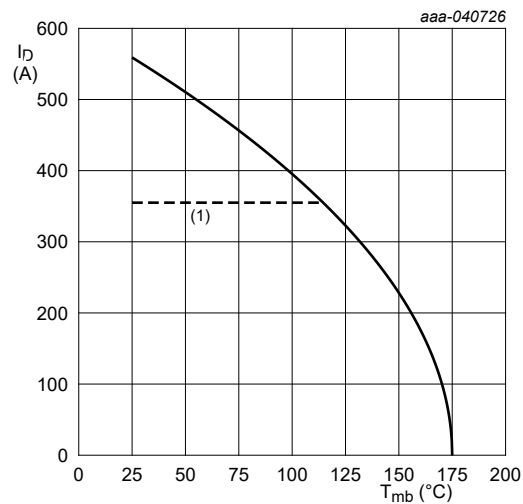
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	935	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	355	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	355	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	2236	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	355	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	2236	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 99\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; $t_p = 175\text{ }\mu\text{s}$; Fig. 4	[1]	-	1126 mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[1]	-	99 A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$

(1) 355 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

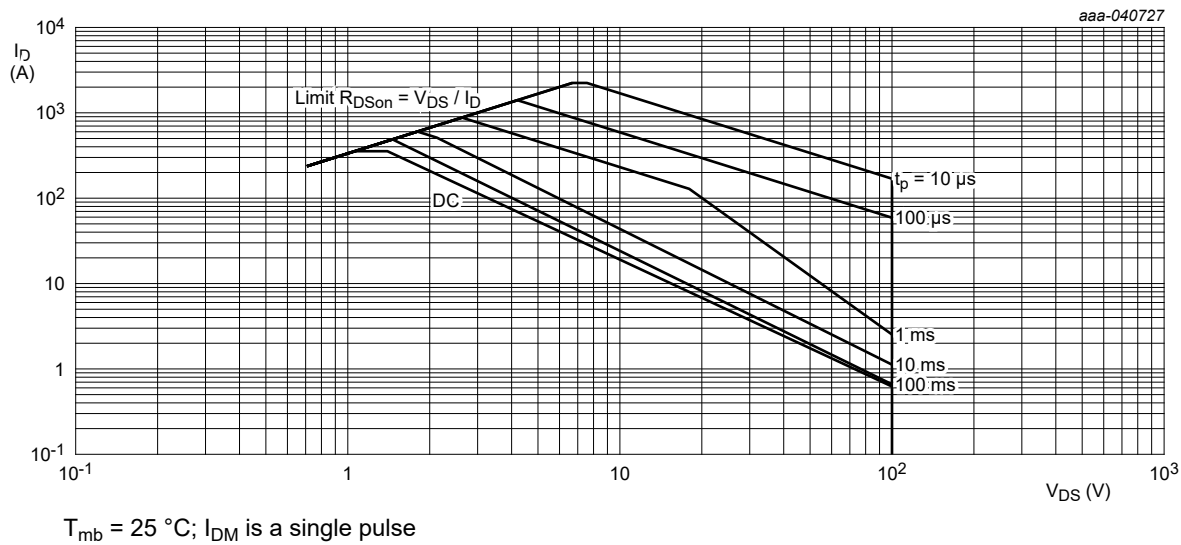
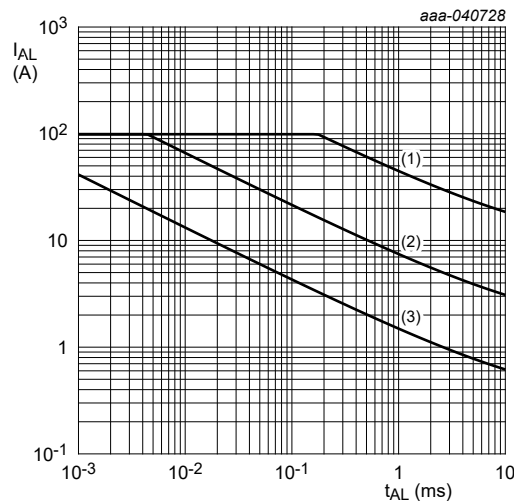


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j \text{ (init)}} = 25 \text{ }^\circ\text{C}$; (2) $T_{j \text{ (init)}} = 150 \text{ }^\circ\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.123	0.16	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	58	-	K/W
		Fig. 7	-	29	-	K/W

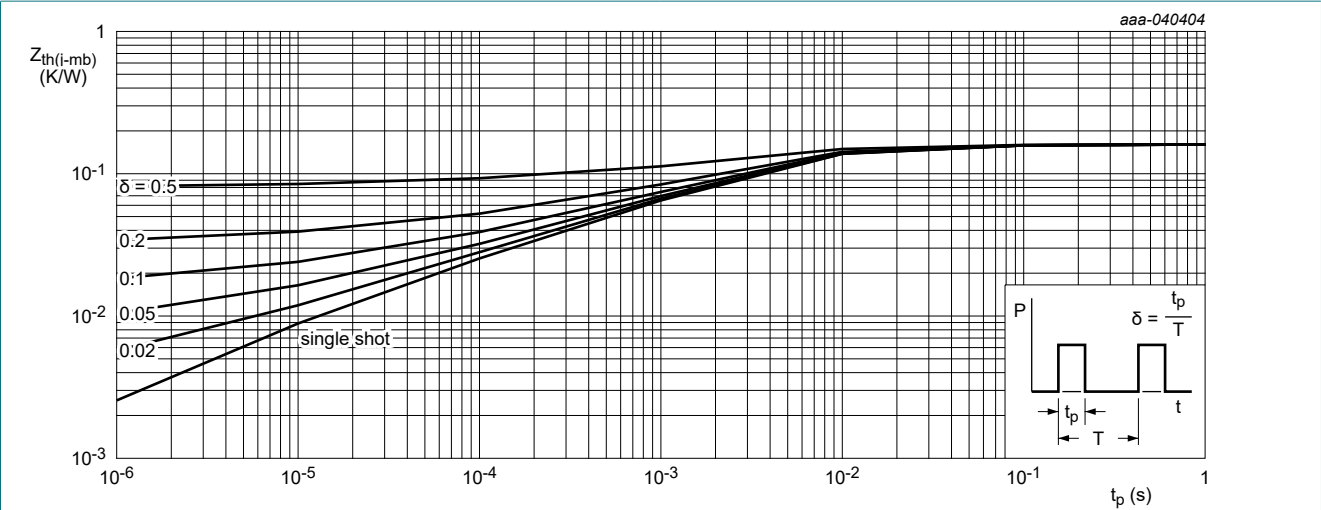


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

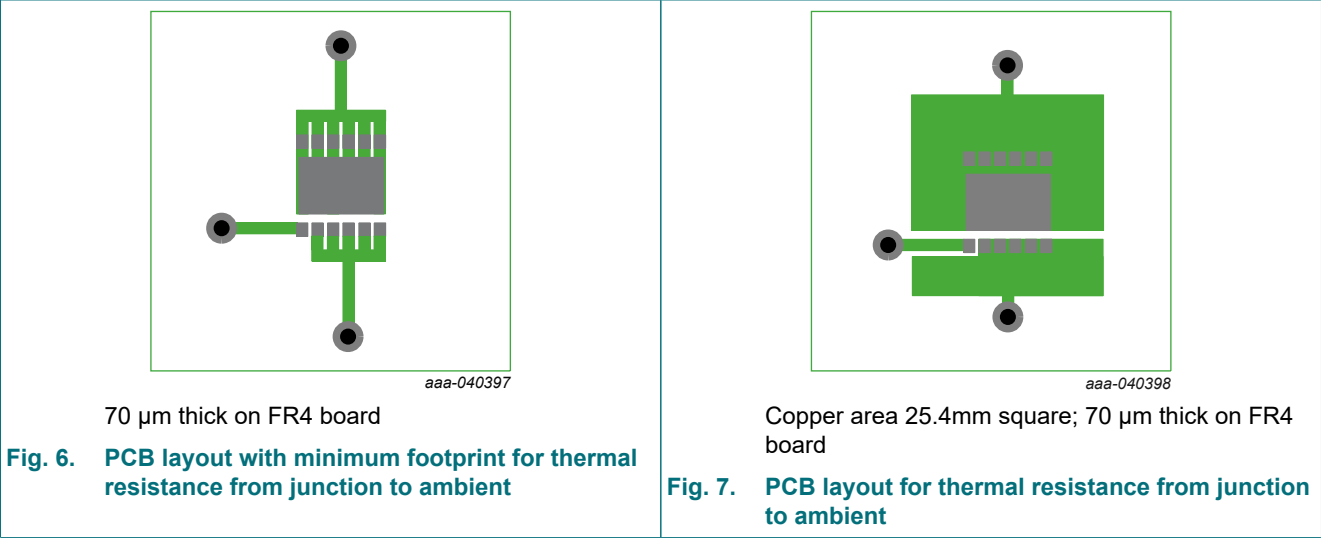


Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

Fig. 7. PCB layout for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C		2	3.08	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C		-	1.58	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C		-	3.6	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C		-	-9.32	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C		-	0.08	1.6	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C		-	31	160	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11		-	1.02	1.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 12		-	1.7	2.1	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12		-	2.4	3	mΩ
		V _{GS} = 7 V; I _D = 25 A; T _j = 25 °C; Fig. 11		-	1.28	1.92	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.54	1.08	2.16	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13 ; Fig. 14		128	255	383	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	228	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13 ; Fig. 14		46	76.5	107	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	51	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	25.4	-	nC
Q _{GD}	gate-drain charge			14	46	106	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 13 ; Fig. 14		-	4.4	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		10901	18168	25436	pF
C _{oss}	output capacitance			2494	4157	6652	pF
C _{rss}	reverse transfer capacitance			9	92	239	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	67	-	ns
t _r	rise time			-	63	-	ns
t _{d(off)}	turn-off delay time			-	157	-	ns
t _f	fall time			-	84	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.76	1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	62	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17	-	74	-	nC

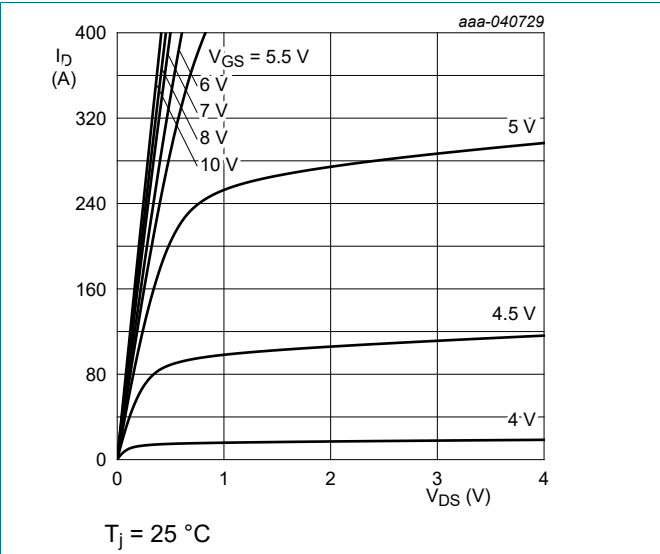


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

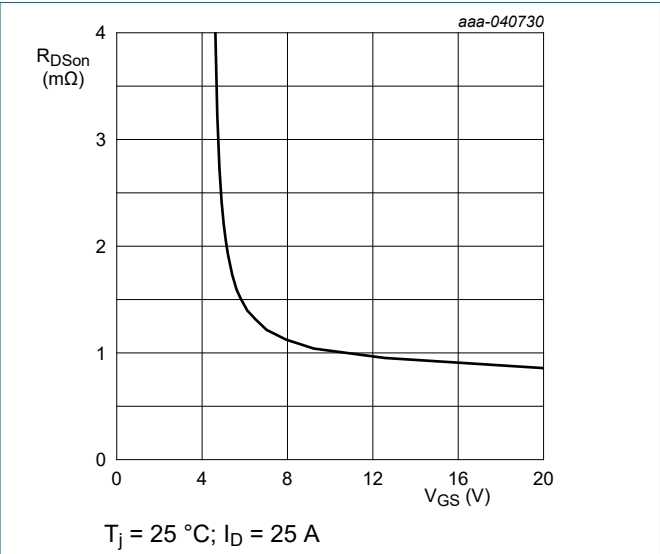


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

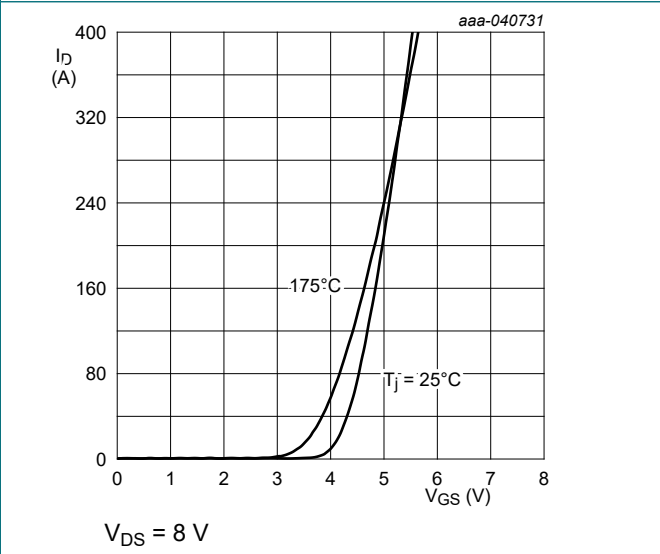


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

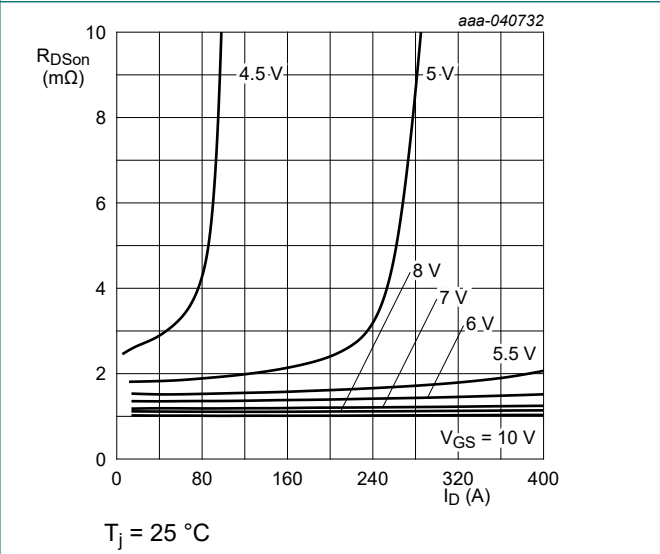


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

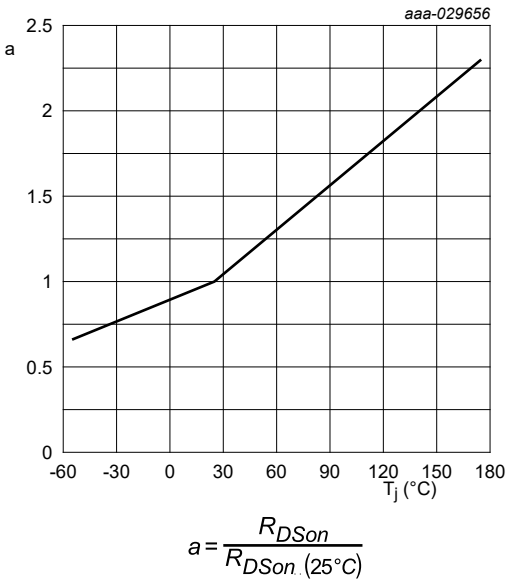


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

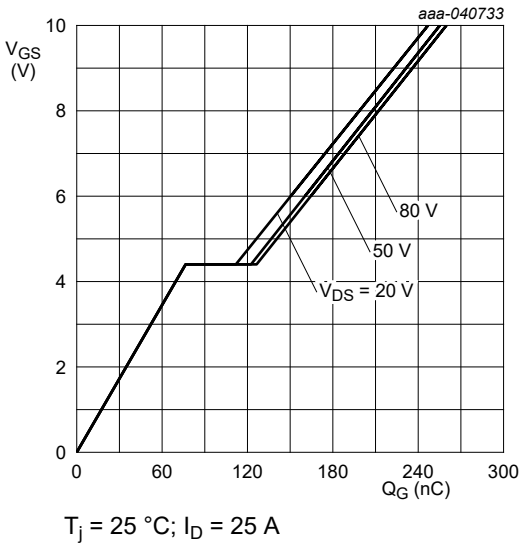


Fig. 13. Gate-source voltage as a function of gate charge; typical values

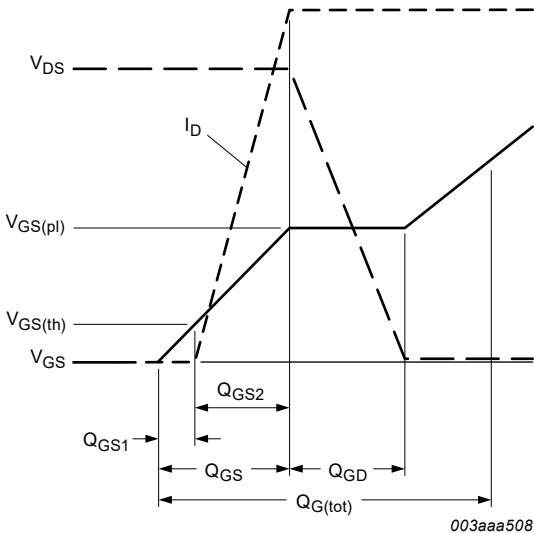


Fig. 14. Gate charge waveform definitions

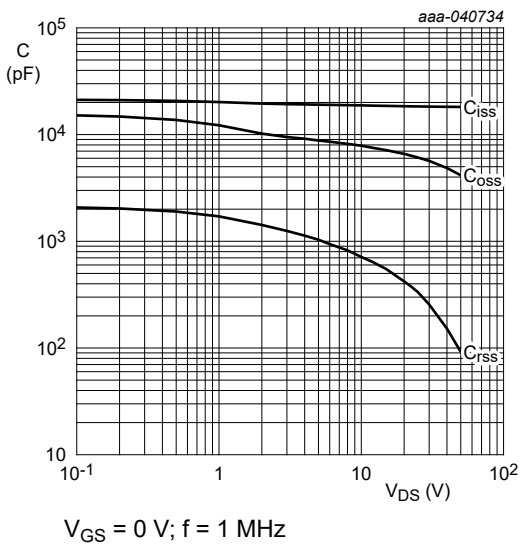


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

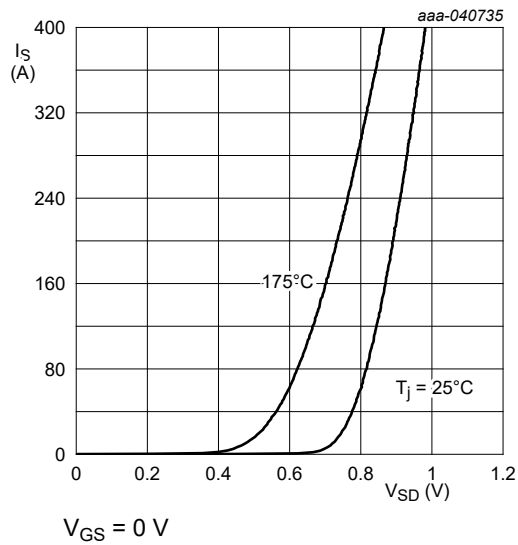


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

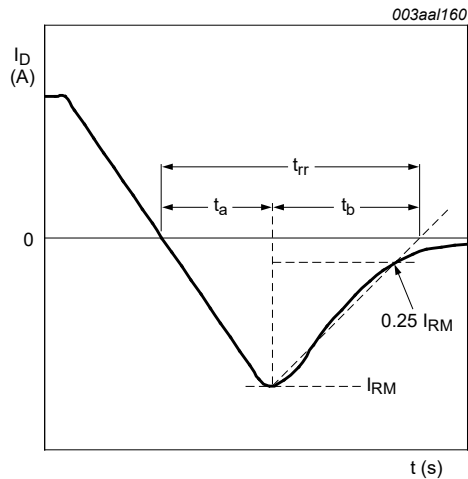


Fig. 17. Reverse recovery timing definition

11. Package outline

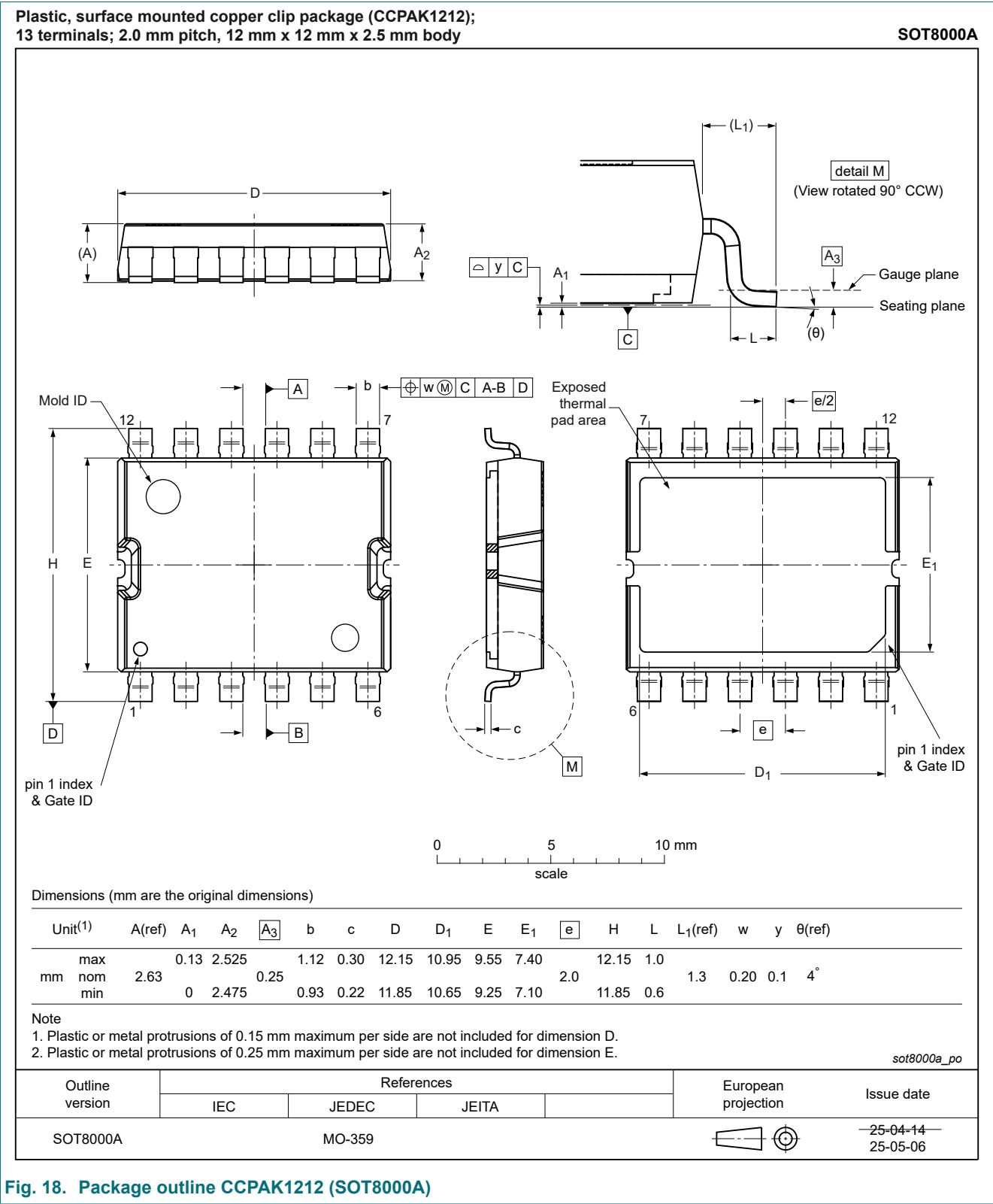


Fig. 18. Package outline CCPAK1212 (SOT8000A)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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