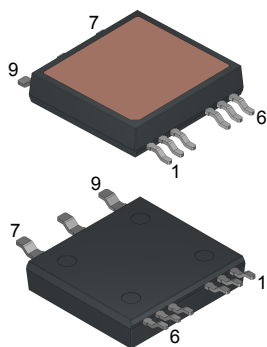
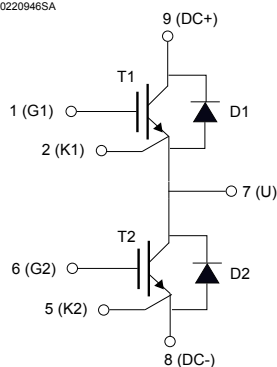


ACEPACK SMIT half-bridge topology 1200 V, 50 A, M series IGBT with diode



ACEPACK SMIT

GADG031120220946SA



Features

- Low-loss and short-circuit rugged IGBTs
- Maximum junction temperature: $T_J = 175\text{ }^{\circ}\text{C}$
- $V_{CE(sat)} = 1.8\text{ V (typ.) @ } I_C = 50\text{ A}$
- Minimized tail current
- Tight parameter distribution
- Low thermal resistance
- Positive $V_{CE(sat)}$ temperature coefficient
- Soft and fast-recovery antiparallel diode
- Isolation rating of 3.4 kVrms/min

Applications

- Motor drives
- Industrial motor control

Description

This device combines two IGBTs and diodes in half-bridge topology mounted on a very compact and rugged easily surface-mounted package. The device is optimized both in conduction and switching losses for hard switching commutation, where short-circuit ruggedness is an essential feature. A freewheeling diode with a low drop forward voltage is included in every switch. The result is a product specifically designed to maximize efficiency and power density in industrial drives.



Product status link

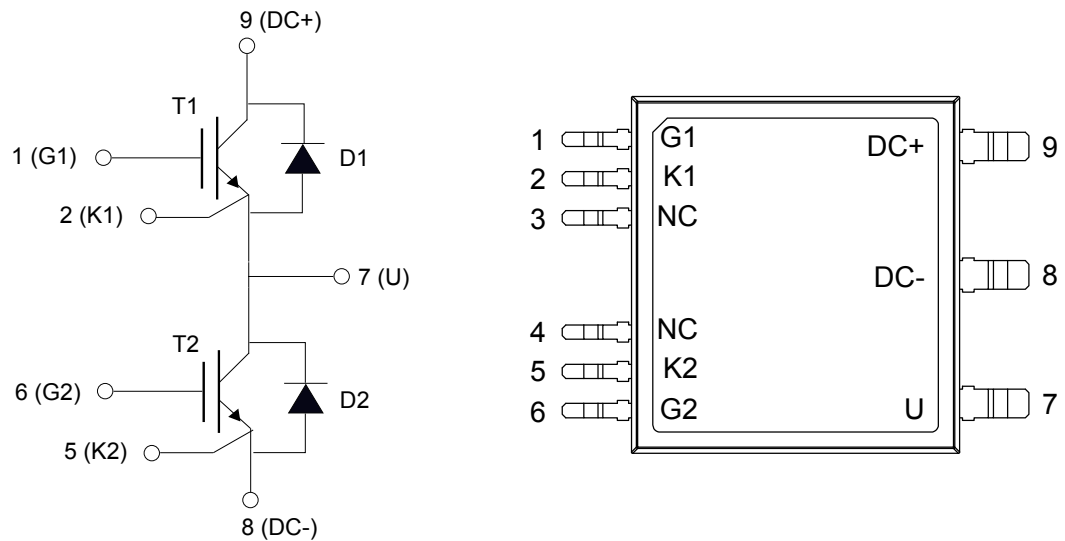
[STGSH50M120D](#)

Product summary

Order code	STGSH50M120D
Marking	GSH50M120D
Package	ACEPACK SMIT
Packing	Tape and reel

1 Internal schematic and pin description

Figure 1. Electrical topology and pin positioning



GADG170820230949FF

Table 1. Pin description

Pin	Symbol	Description
1	G1	Gate of high-side IGBT
2	K1	Kelvin emitter of high-side IGBT
3	NC	Not connected
4	NC	Not connected
5	K2	Kelvin emitter of low-side IGBT
6	G2	Gate of low-side IGBT
7	U	Phase output
8	DC-	Negative DC input
9	DC+	Positive DC input

2 Electrical ratings

Data referred to each IGBT with co-packed diode.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$ V)	1200	V
$I_C^{(1)}$	Continuous collector current at $T_C = 100$ °C	69	A
$I_{CP}^{(2)}$	Pulsed collector current ($t_p = 1$ ms)	240	A
V_{GE}	Gate-emitter voltage	±20	V
$I_F^{(1)}$	Continuous forward current at $T_C = 100$ °C	40	A
$I_{FP}^{(2)}$	Pulsed forward current ($t_p = 1$ ms)	136	A
P_{TOT}	Total power dissipation at $T_C = 25$ °C	536	W

1. Current limited by package.
2. Pulse width is limited by maximum junction temperature.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case IGBT	0.28	°C/W
	Thermal resistance, junction-to-case diode	0.7	

Table 4. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage 50/60 Hz, $t = 60$ s)	3.4	kVrms
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	°C

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 5. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}$, $I_C = 2\text{ mA}$	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 50\text{ A}$		1.8	2.3	V
		$V_{GE} = 15\text{ V}$, $I_C = 50\text{ A}$, $T_J = 125\text{ °C}$		2.0		
		$V_{GE} = 15\text{ V}$, $I_C = 50\text{ A}$, $T_J = 175\text{ °C}$		2.2		
V_F	Forward on-voltage	$I_F = 50\text{ A}$		2.8		V
		$I_F = 50\text{ A}$, $T_J = 125\text{ °C}$		2.3		
		$I_F = 50\text{ A}$, $T_J = 175\text{ °C}$		2.0		
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 2\text{ mA}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}$, $V_{CE} = 1200\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}$, $V_{GE} = \pm 20\text{ V}$			250	nA

Table 6. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GE} = 0\text{ V}$	-	3152	-	pF
C_{oes}	Output capacitance		-	310	-	pF
C_{res}	Reverse transfer capacitance		-	123	-	pF
Q_g	Total gate charge	$V_{CC} = 960\text{ V}$, $I_C = 50\text{ A}$, $V_{GE} = 0\text{ to }15\text{ V}$	-	194	-	nC

Table 7. Switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600\text{ V}$, $V_{GK} = -15\text{ to }15\text{ V}$, $R_G = 10\ \Omega$, $I_C = 50\text{ A}$	-	68	-	ns
t_r	Current rise time		-	13	-	ns
$E_{on}^{(1)}$	Turn-on switching energy		-	1.94	-	mJ
$t_{d(off)}$	Turn-off delay time		-	135	-	ns
t_f	Current fall time		-	197	-	ns
$E_{off}^{(2)}$	Turn-off switching energy		-	3.44	-	mJ
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600\text{ V}$, $V_{GK} = -15\text{ to }15\text{ V}$, $R_G = 10\ \Omega$, $I_C = 50\text{ A}$, $T_J = 175\text{ °C}$	-	69	-	ns
t_r	Current rise time		-	13	-	ns
$E_{on}^{(1)}$	Turn-on switching energy		-	3.98	-	mJ
$t_{d(off)}$	Turn-off delay time		-	152	-	ns
t_f	Current fall time		-	296	-	ns
$E_{off}^{(2)}$	Turn-off switching energy		-	4.6	-	mJ
t_{sc}	Short-circuit withstand time	$V_{CC} \leq 600\text{ V}$, $V_{GE} = 15\text{ V}$, $T_{Jstart} \leq 150\text{ °C}$	10			μs

1. Including the reverse recovery of the diode

2. Including the tail of the collector current

Table 8. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	$I_F = 50\text{ A}$, $V_R = 600\text{ V}$, $R_G = 10\ \Omega$	-	294	-	ns
Q_{rr}	Reverse recovery charge		-	2.79	-	μC
I_{rrm}	Reverse recovery current		-	67	-	A
E_{rr}	Reverse recovery energy		-	0.94	-	mJ
t_{rr}	Reverse recovery time	$I_F = 50\text{ A}$, $V_R = 600\text{ V}$, $R_G = 10\ \Omega$, $T_J = 175\text{ °C}$	-	382	-	ns
Q_{rr}	Reverse recovery charge		-	7.52	-	μC
I_{rrm}	Reverse recovery current		-	82	-	A
E_{rr}	Reverse recovery energy		-	2.66	-	mJ

3.1 Electrical characteristics (curves)

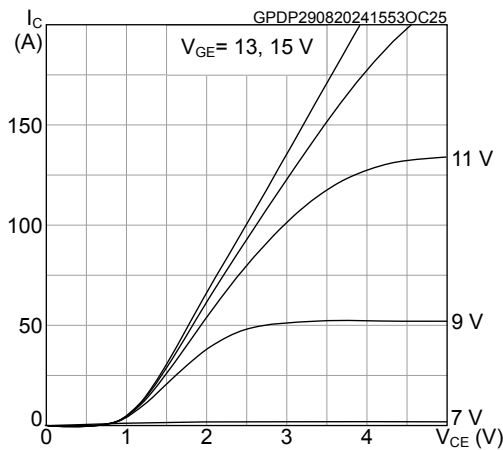
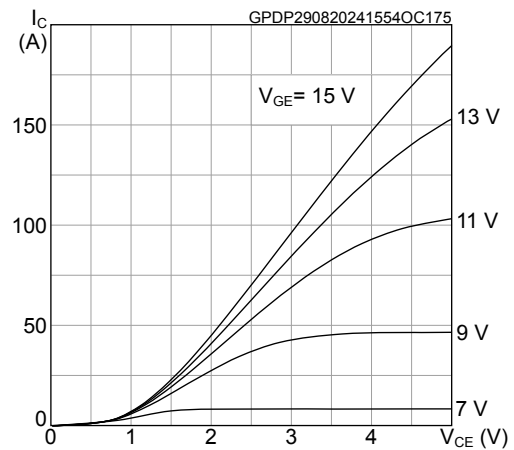
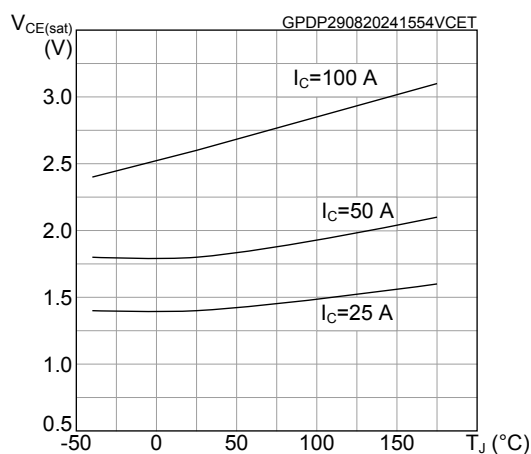
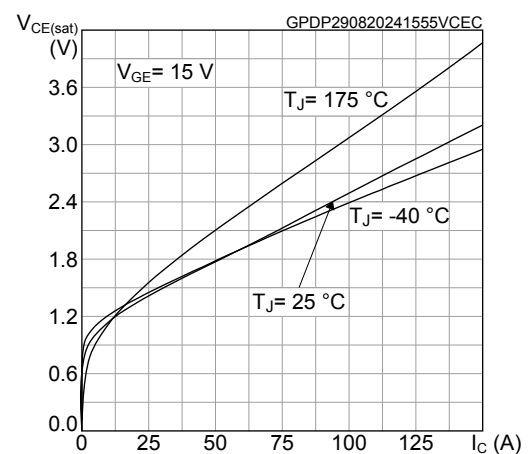
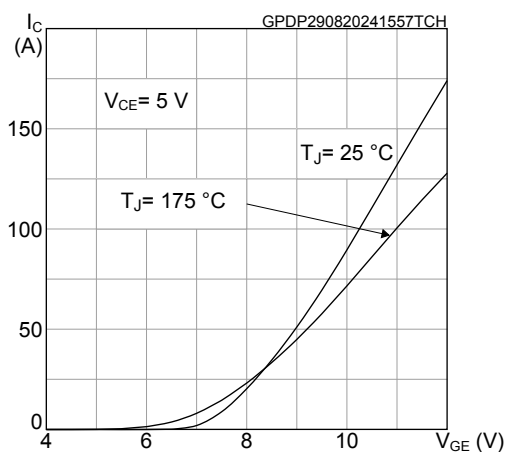
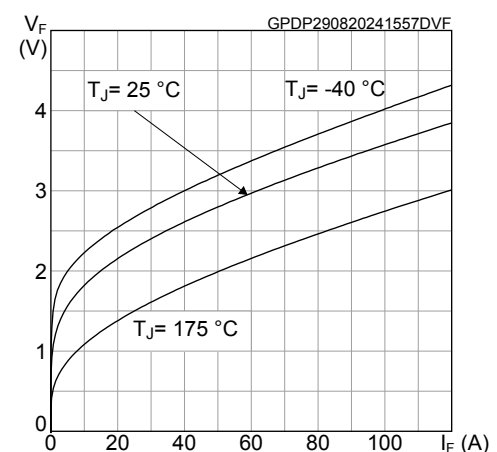
Figure 2. Typical output characteristics ($T_J = 25^\circ\text{C}$)

Figure 3. Typical output characteristics ($T_J = 175^\circ\text{C}$)

Figure 4. Normalized $V_{CE(sat)}$ vs temperature

Figure 5. Typical $V_{CE(sat)}$ vs collector current

Figure 6. Typical transfer characteristics

Figure 7. Typical diode V_F vs forward current


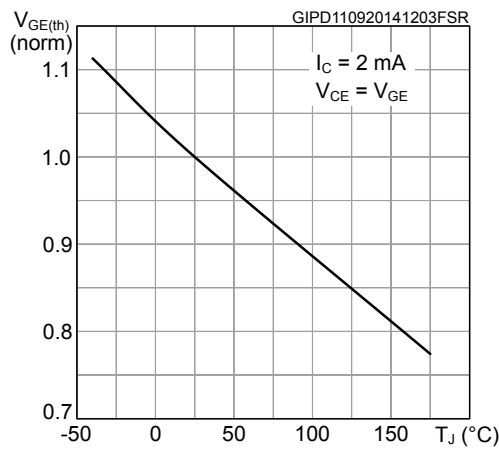
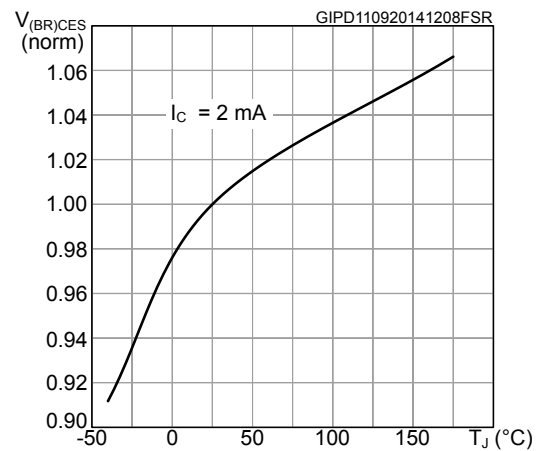
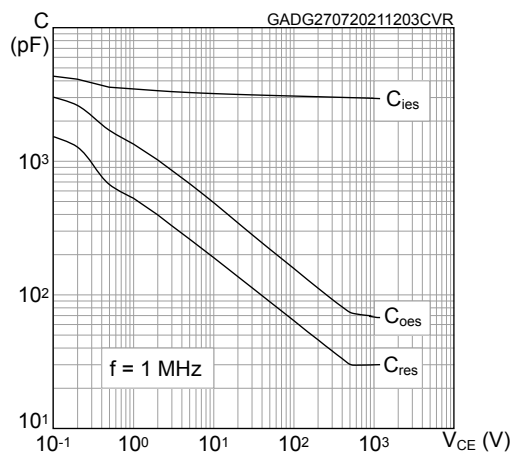
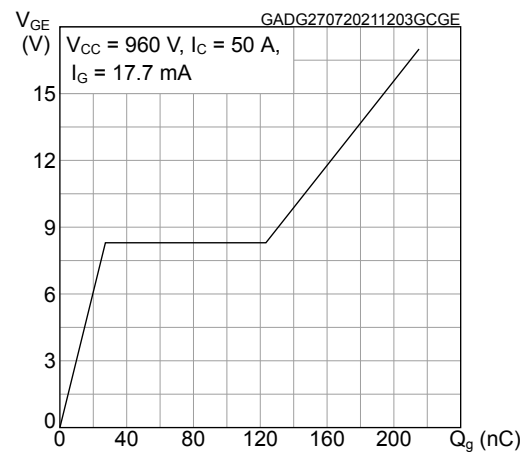
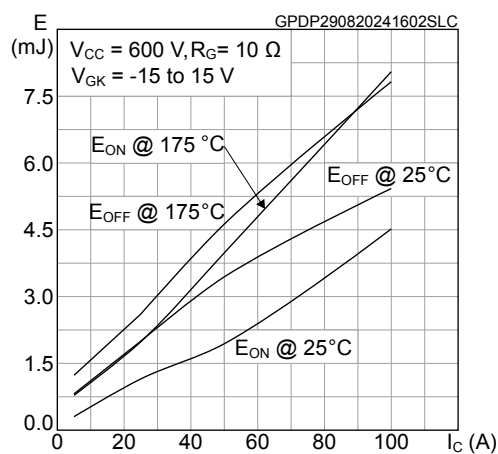
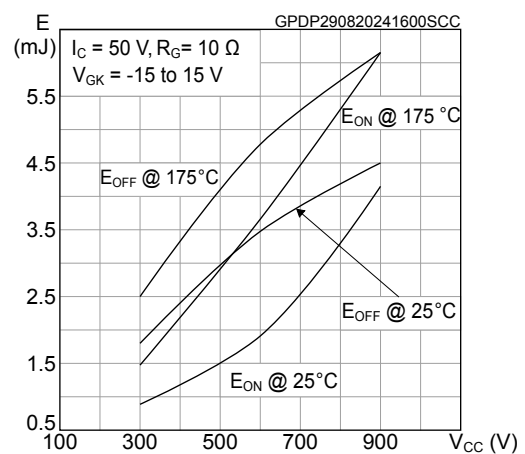
Figure 8. Normalized $V_{GE(th)}$ vs temperature

Figure 9. Normalized $V_{(BR)CES}$ vs temperature

Figure 10. Typical capacitance characteristics

Figure 11. Typical gate charge characteristics

Figure 12. Typical switching energy vs collector current

Figure 13. Typical switching energy vs supply voltage


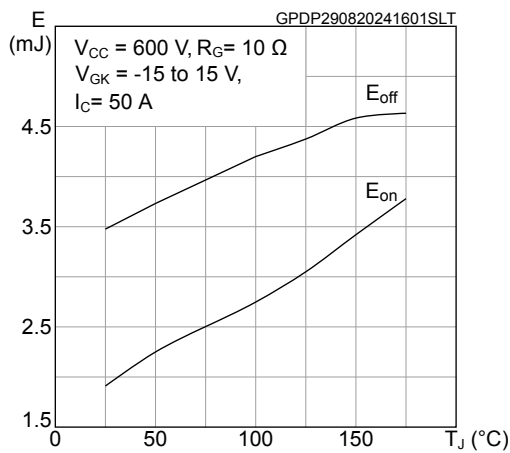
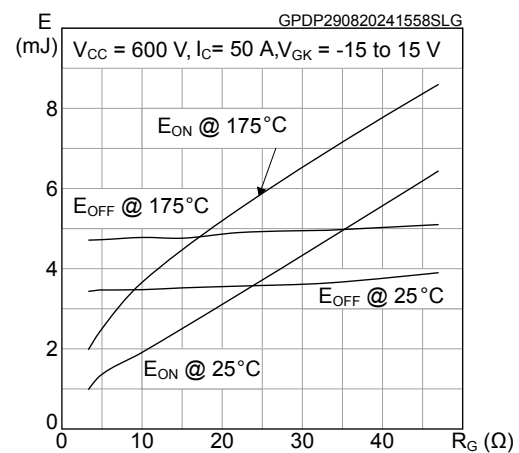
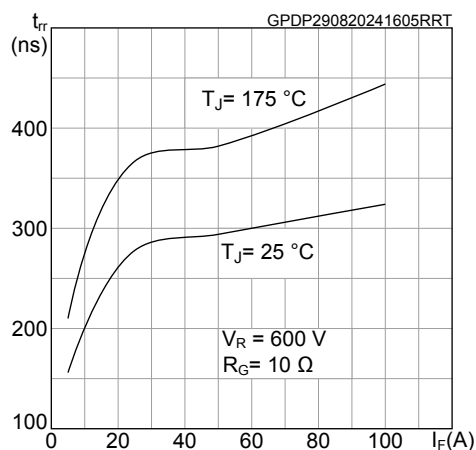
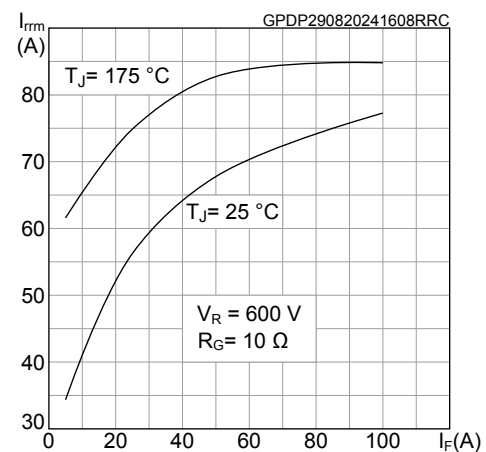
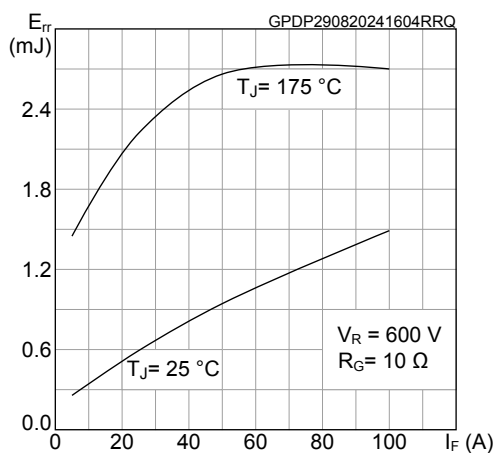
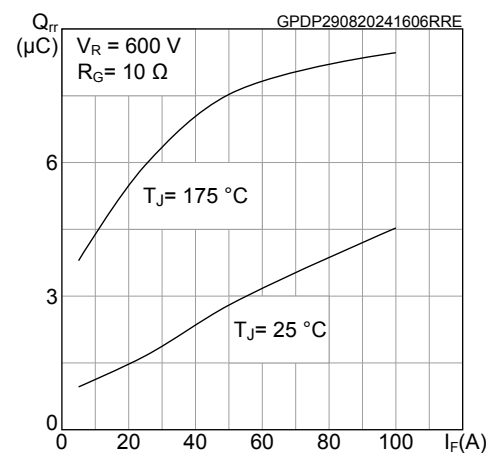
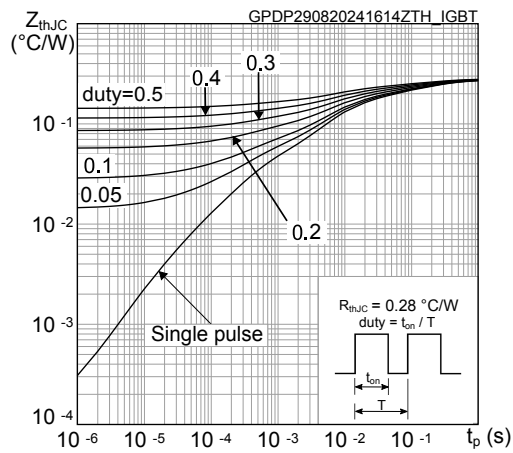
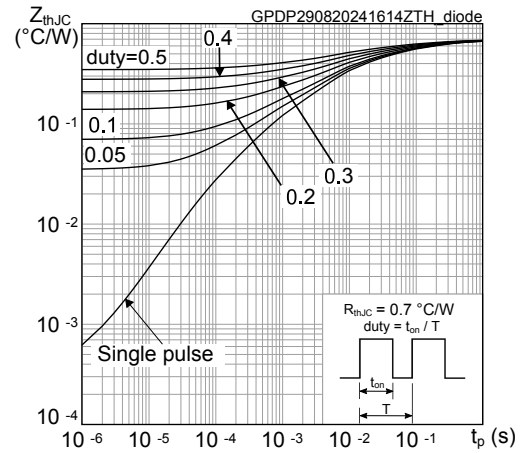
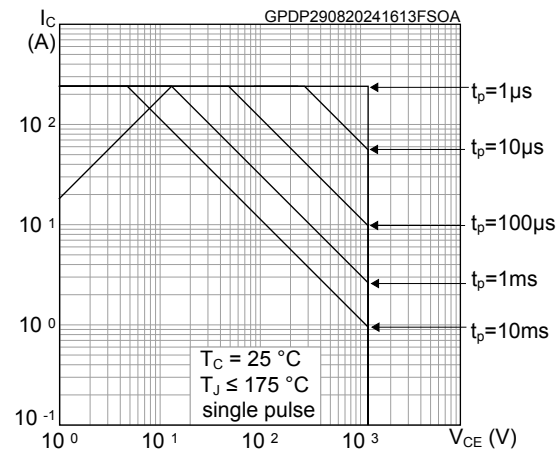
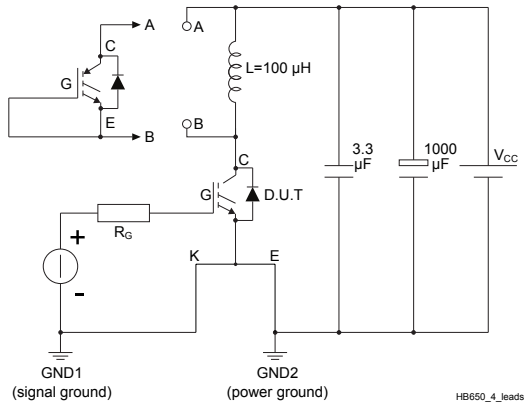
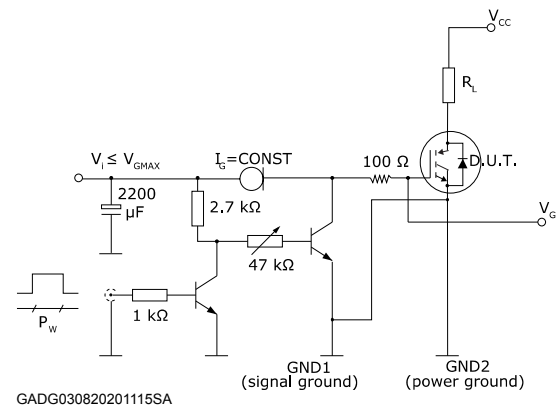
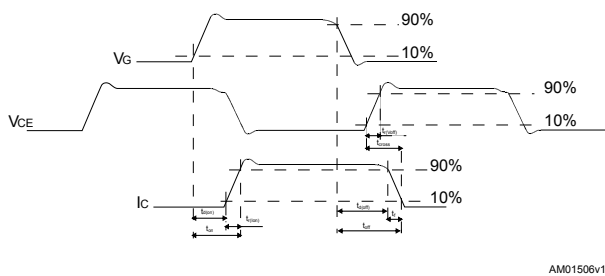
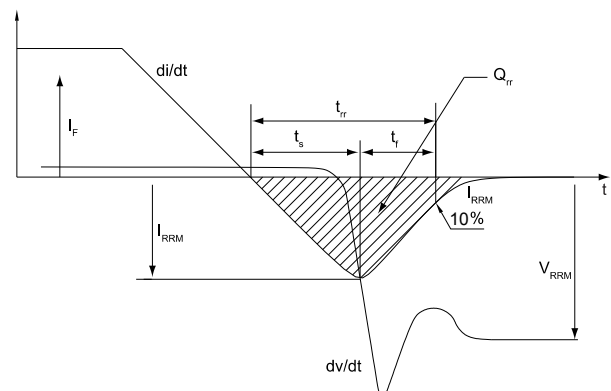
Figure 14. Typical switching energy vs temperature

Figure 15. Typical switching energy vs R_G

Figure 16. Diode reverse recovery time vs forward current

Figure 17. Diode reverse recovery current vs forward current

Figure 18. Diode reverse recovery energy vs forward current

Figure 19. Diode reverse recovery charge vs forward current


Figure 20. Maximum transient thermal impedance for IGBT

Figure 21. Maximum transient thermal impedance for diode

Figure 22. Forward bias safe operating area


4 Test circuits

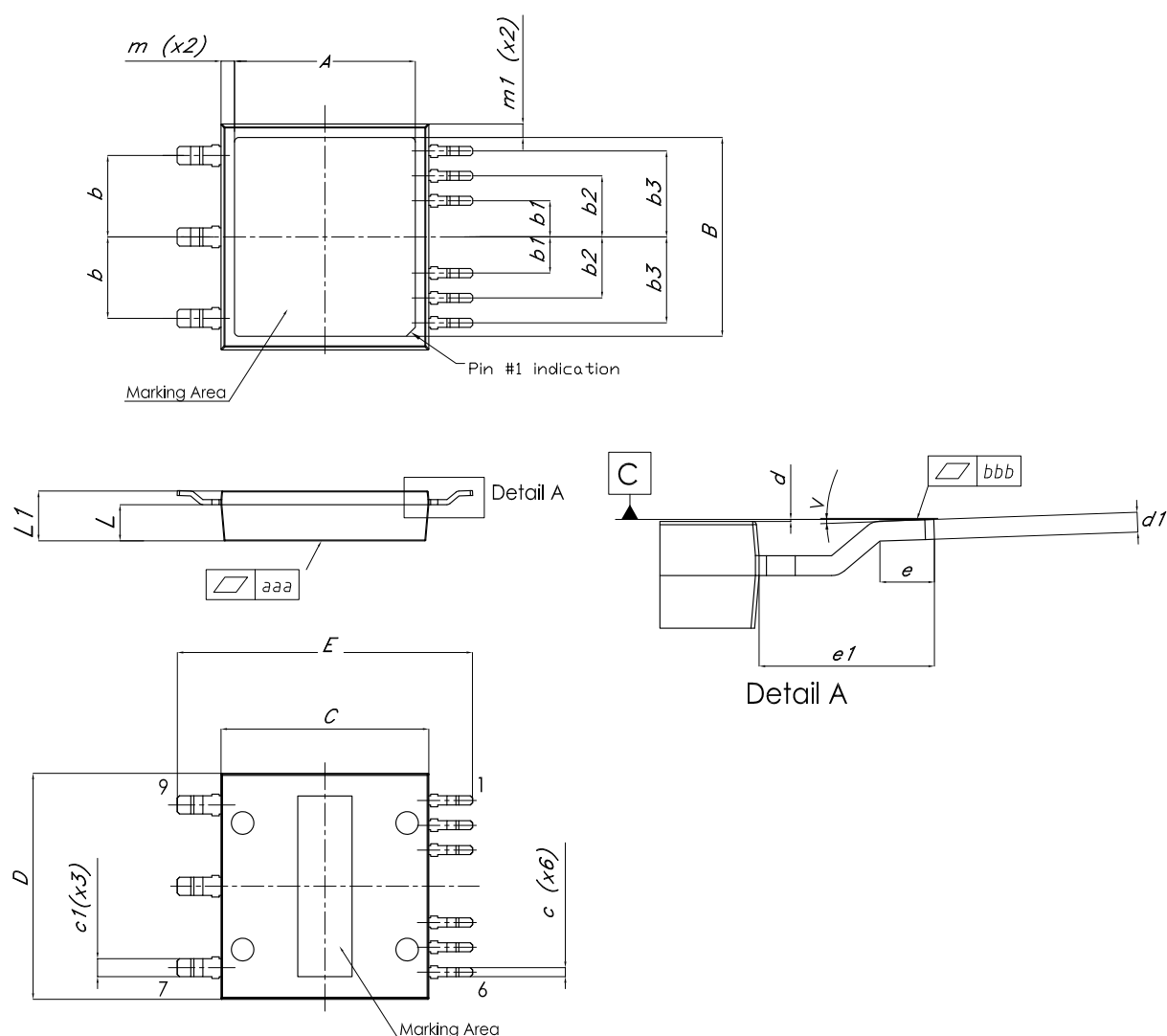
Figure 23. Test circuit for inductive load switching

Figure 24. Gate charge test circuit

Figure 25. Switching waveform

Figure 26. Diode reverse recovery waveform


5 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 ACEPACK SMIT package information

Figure 27. ACEPACK SMIT package outline

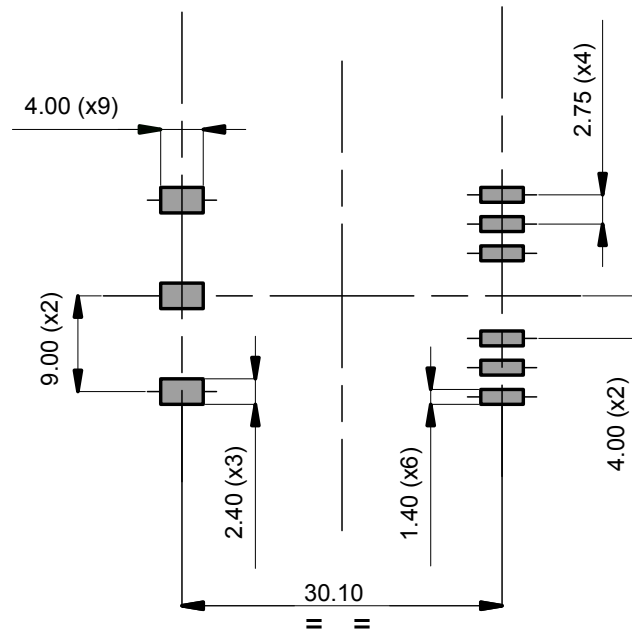


DM00447519_Rev.7

Table 9. ACEPACK SMIT package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	19.50	20.00	20.50
B	21.50	22.00	22.50
C	22.80	23.00	23.20
D	24.80	25.00	25.20
E	32.20	32.70	33.20
b		9.00	
b1		4.00	
b2		6.75	
b3		9.50	
c	0.95	1.00	1.10
c1	1.95	2.00	2.10
d	0.00		0.15
d1	0.45	0.55	0.65
e	1.30	1.50	1.70
e1	4.65	4.85	5.05
L	3.95	4.00	4.05
L1	5.40	5.50	5.60
m	1.30	1.50	1.80
m1	1.30	1.50	1.80
V	0°	2°	4°
aaa	0.01		0.05
bbb	0.00		0.10

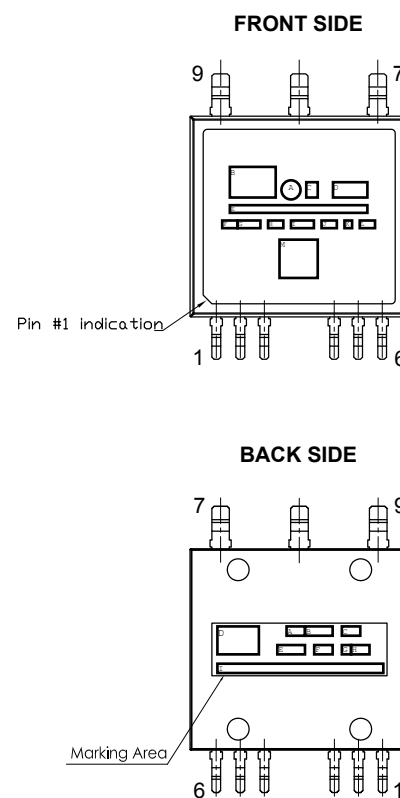
Figure 28. ACEPACK SMIT recommended footprint



DM00447519_FP_Rev.7

Note: Dimensions in mm.

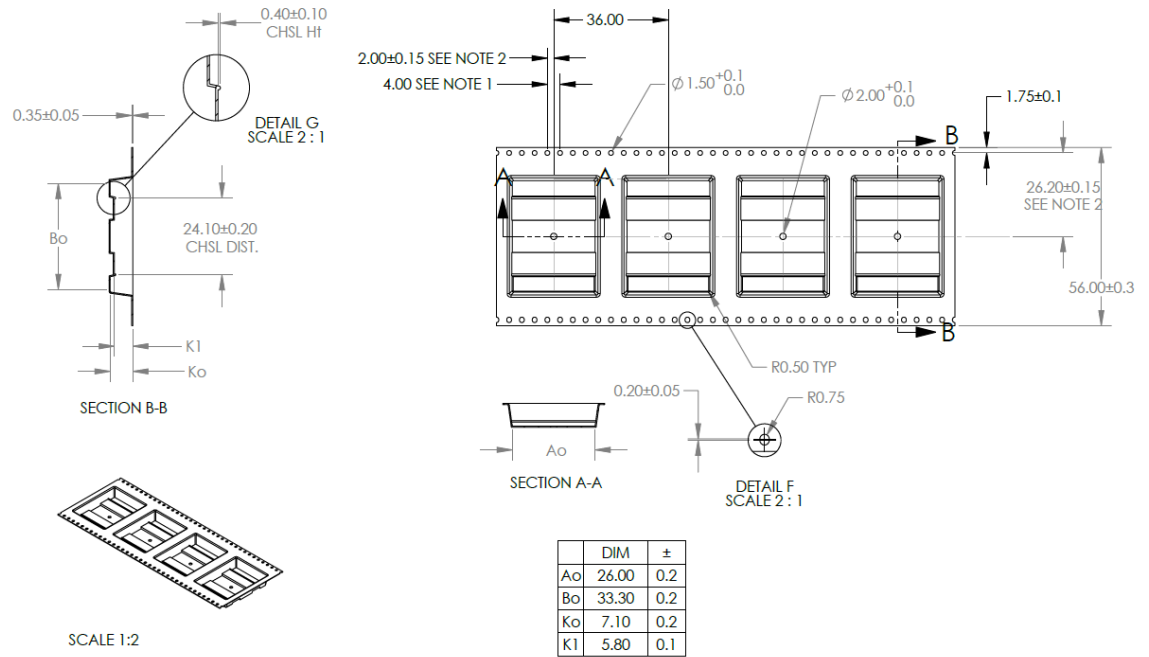
Figure 29. ACEPACK SMIT marking orientation vs pinout



DM00447519_MO_Rev.7

5.2 ACEPACK SMIT packing information

Figure 30. ACEPACK SMIT tape outline



- NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
 2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
 3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

DM00631393_Tape_Rev.1

Note: Dimensions in mm.

Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Sep-2024	1	First release.
11-Nov-2024	2	Updated Table 2. Absolute maximum ratings and Table 5. Static characteristics .

Contents

1	Internal schematic and pin description	2
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3	Electrical characteristics	4
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4	Test circuits	10
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