



PHPT610030NPK-Q

NPN/PNP high power double bipolar transistor

25 October 2024

Product data sheet

1. General description

NPN/PNP high power double bipolar transistor in a SOT1205 (LFPK56D) Surface-Mounted Device (SMD) power plastic package.

NPN/PNP complement: PHPT610030NK-Q

PNP/PNP complement: PHPT610030PK-Q

2. Features and benefits

- High thermal power dissipation capability
- Suitable for high temperature applications up to 175 °C
- Reduced Printed-Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Motor control
- Power management
- Load switch
- Linear mode voltage regulator
- Backlighting applications
- Relay replacement

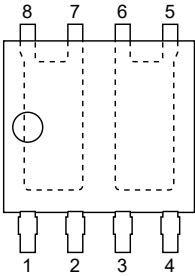
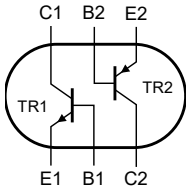
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CE0}	collector-emitter voltage	open base	-	-	100	V
I_C	collector current		-	-	3	A
TR1 (NPN)						
R_{CEsat}	collector-emitter saturation resistance	$I_C = 3\text{ A}$; $I_B = 300\text{ mA}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	75	110	m Ω
TR2 (PNP)						
R_{CEsat}	collector-emitter saturation resistance	$I_C = -2\text{ A}$; $I_B = -200\text{ mA}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	110	180	m Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 LPAK56D; Dual LPAK (SOT1205)	 sym139
2	B1	base TR1		
3	E2	emitter TR2		
4	B2	base TR2		
5	C2	collector TR2		
6	C2	collector TR2		
7	C1	collector TR1		
8	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHPT610030NPK-Q	LPAK56D; Dual LPAK	plastic, single ended surface mounted package (LPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

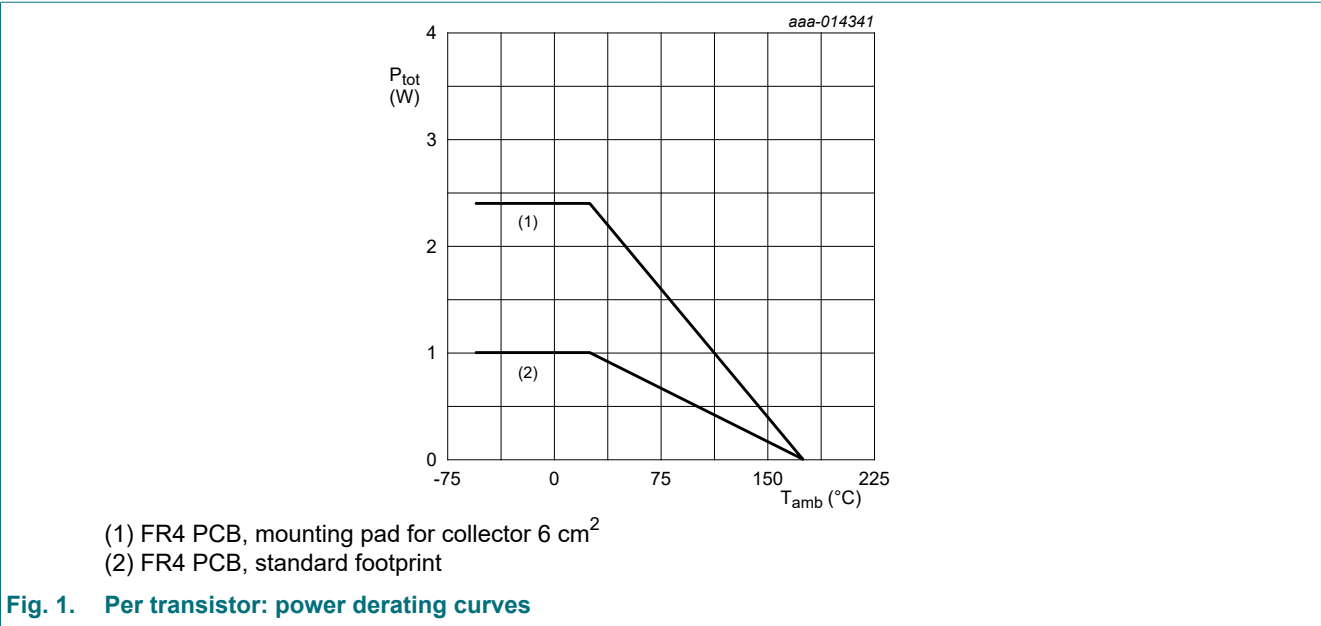
Type number	Marking code
PHPT610030NPK-Q	1003NPK

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	100	V
V _{CEO}	collector-emitter voltage	open base		-	100	V
V _{EBO}	emitter-base voltage	open collector		-	7	V
I _C	collector current			-	3	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	8	A
I _B	base current			-	0.5	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	1	W
			[2]	-	2.4	W
			[3]	-	25	W
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	1.25	W
			[2]	-	3	W
			[4]	-	5	W
T _j	junction temperature			-	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [3] Power dissipation from junction to mounting base.
- [4] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

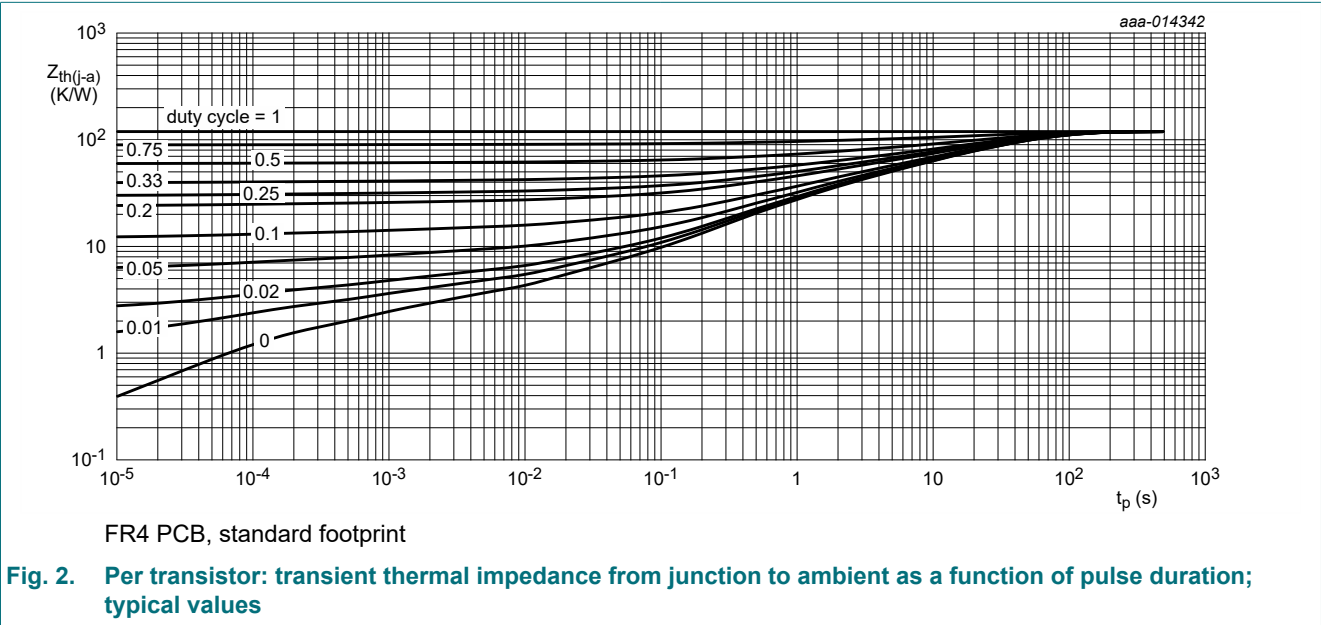


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	150	K/W
			[2]	-	-	62.5	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	6	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	120	K/W
			[2]	-	-	50	K/W
			[3]	-	-	30	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



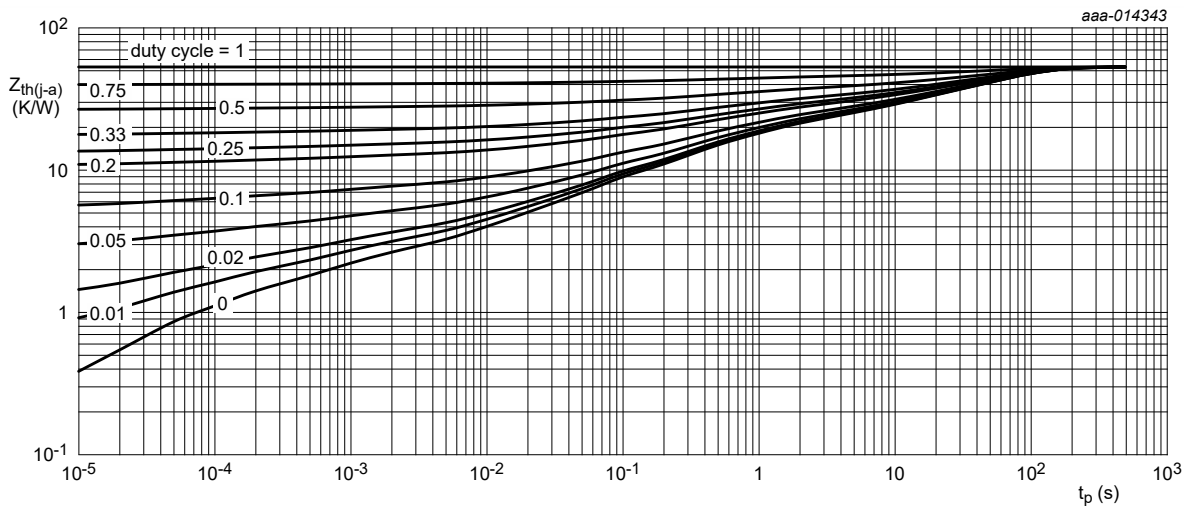


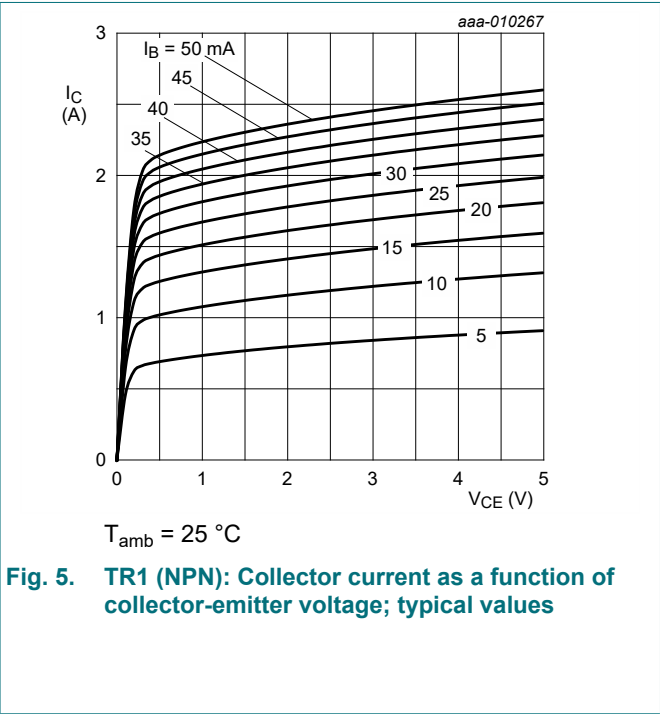
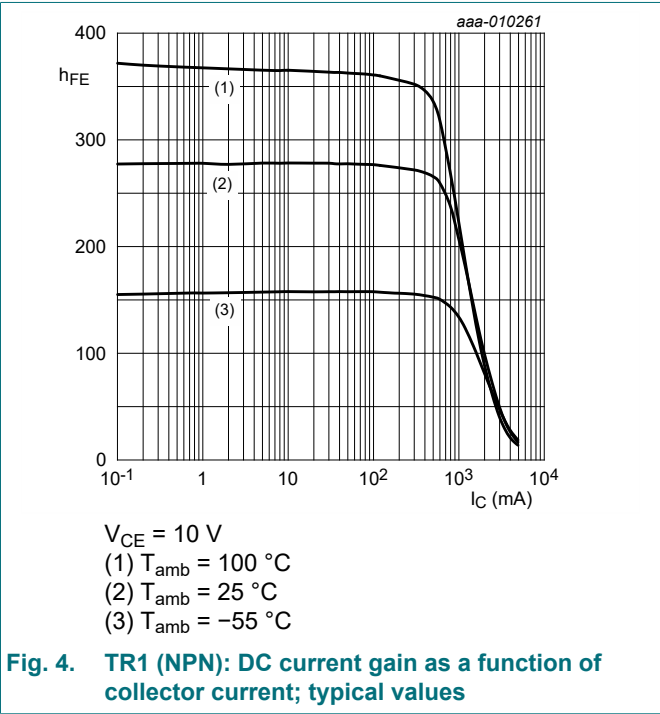
Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (NPN)							
I _{CBO}	collector-base cut-off current	V _{CB} = 80 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
		V _{CB} = 80 V; I _E = 0 A; T _j = 150 °C		-	-	50	µA
I _{CES}	collector-emitter cut-off current	V _{CE} = 80 V; V _{BE} = 0 V		-	-	100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = 7 V; I _C = 0 A; T _{amb} = 25 °C		-	-	100	nA
h _{FE}	DC current gain	V _{CE} = 10 V; I _C = 500 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		150	250	-	
		V _{CE} = 10 V; I _C = 1 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		80	250	-	
		V _{CE} = 10 V; I _C = 2 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		20	100	-	
		V _{CE} = 10 V; I _C = 3 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		10	40	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	90	150	mV
		I _C = 3 A; I _B = 0.3 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	225	330	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = 3 A; I _B = 300 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	75	110	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	0.86	1	V
		I _C = 2 A; I _B = 200 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	1	1.2	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = 2 V; I _C = 100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	0.67	0.85	V
t _d	delay time	V _{CC} = 12.5 V; I _C = 1 A; I _{Bon} = 50 mA; I _{Boff} = -50 mA; T _{amb} = 25 °C		-	20	-	ns
t _r	rise time			-	300	-	ns
t _{on}	turn-on time			-	320	-	ns
t _s	storage time			-	830	-	ns
t _f	fall time			-	470	-	ns
t _{off}	turn-off time			-	1300	-	ns
f _T	transition frequency	V _{CE} = 10 V; I _C = 100 mA; f = 100 MHz; T _{amb} = 25 °C		-	140	-	MHz
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	11	-	pF
TR2 (PNP)							
I _{CBO}	collector-base cut-off current	V _{CB} = -80 V; I _E = 0 A		-	-	-100	nA
		V _{CB} = -80 V; I _E = 0 A; T _j = 150 °C		-	-	-50	µA
I _{CES}	collector-emitter cut-off current	V _{CE} = -80 V; V _{BE} = 0 V		-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -7 V; I _C = 0 A		-	-	-100	nA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
h _{FE}	DC current gain	V _{CE} = -10 V; I _C = -500 mA; T _{amb} = 25 °C	150	200	-	
		V _{CE} = -10 V; I _C = -1 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	80	210	-	
		V _{CE} = -10 V; I _C = -2 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	20	100	-	
		V _{CE} = -10 V; I _C = -3 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	10	40	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -500 mA; I _B = -50 mA; T _{amb} = 25 °C	-	-70	-110	mV
		I _C = -2 A; I _B = -0.2 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-220	-360	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -2 A; I _B = -200 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	110	180	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.91	-1	V
		I _C = -2 A; I _B = -200 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-1.02	-1.2	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = -2 V; I _C = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.68	-0.9	V
t _d	delay time	V _{CC} = -12.5 V; I _C = -1 A; I _{Bon} = -50 mA; I _{Boff} = 50 mA; T _{amb} = 25 °C	-	20	-	ns
t _r	rise time		-	180	-	ns
t _{on}	turn-on time		-	200	-	ns
t _s	storage time		-	350	-	ns
t _f	fall time		-	220	-	ns
t _{off}	turn-off time		-	570	-	ns
f _T	transition frequency	V _{CE} = -10 V; I _C = -100 mA; f = 100 MHz; T _{amb} = 25 °C	-	125	-	MHz
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	30	-	pF



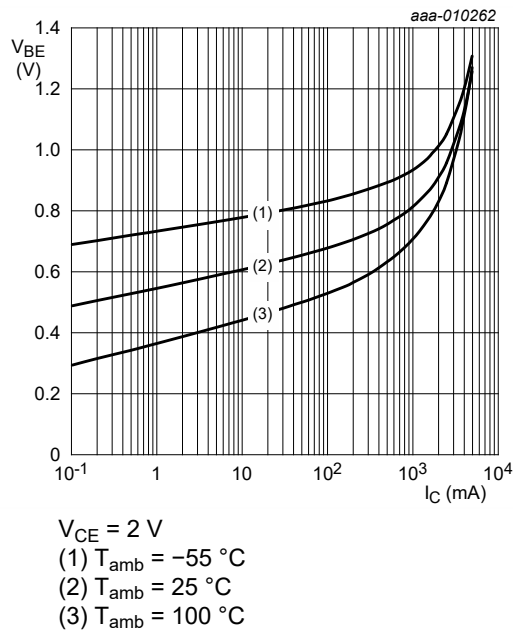


Fig. 6. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values

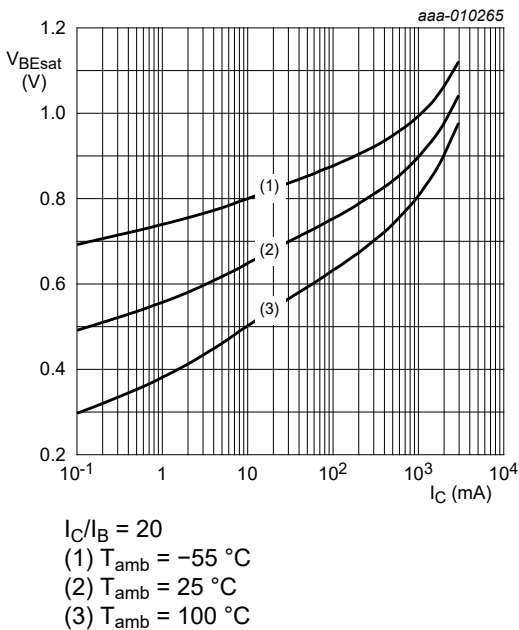


Fig. 7. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values

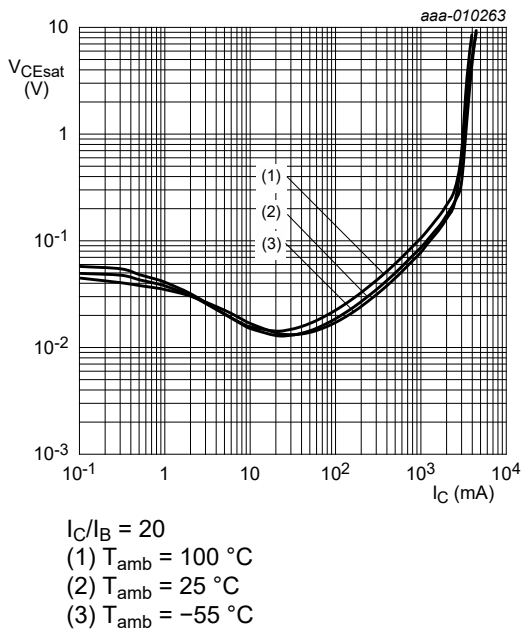


Fig. 8. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

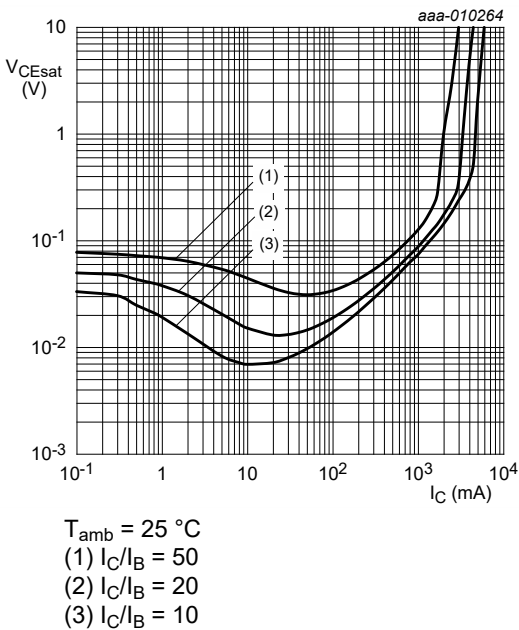


Fig. 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

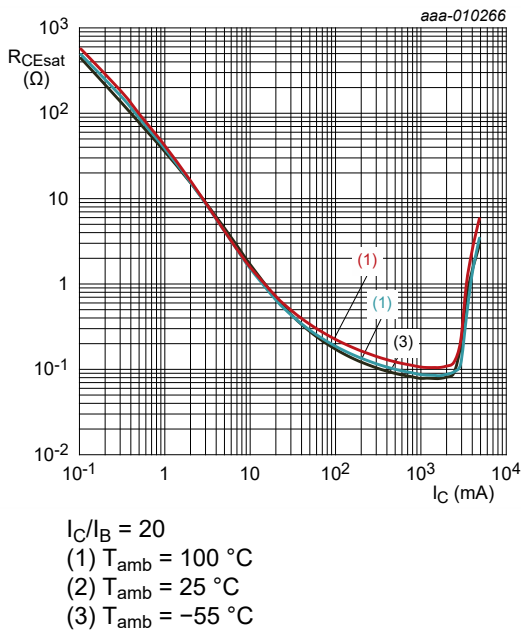


Fig. 10. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

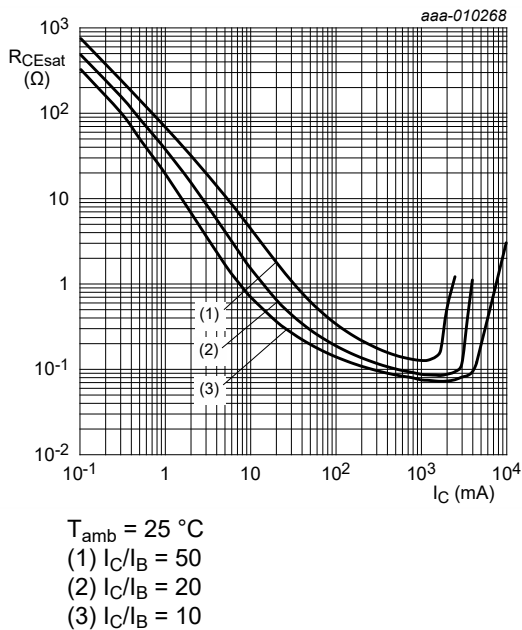


Fig. 11. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

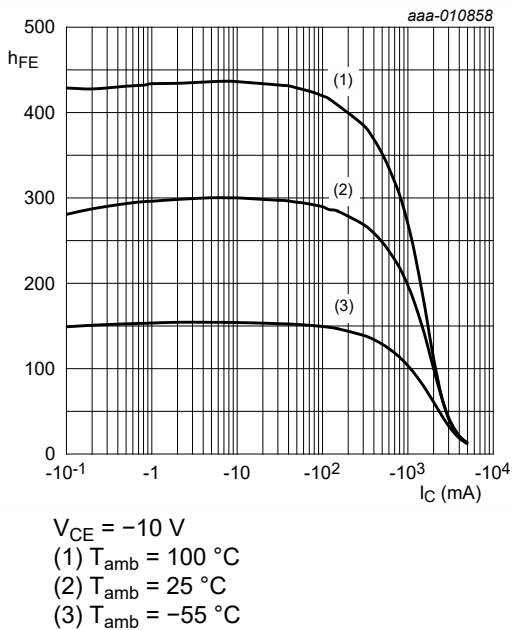


Fig. 12. TR2 (PNP): DC current gain as a function of collector current; typical values

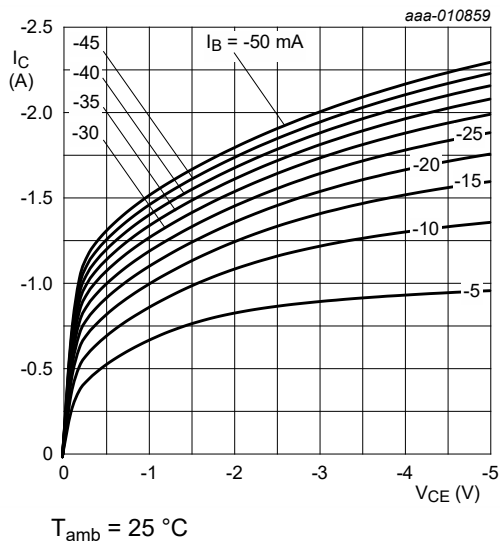


Fig. 13. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

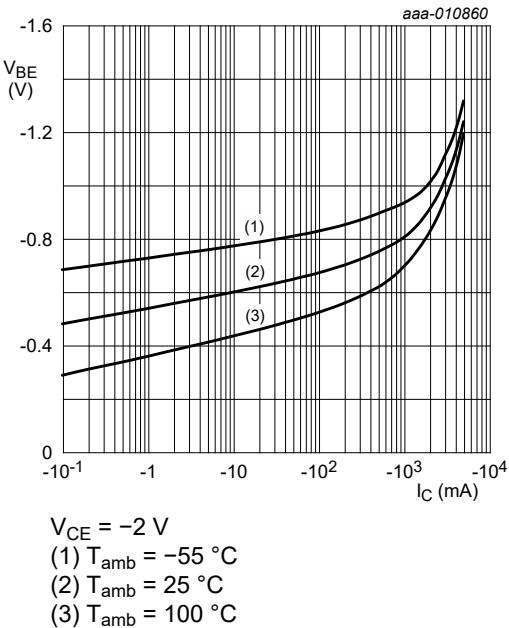


Fig. 14. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values

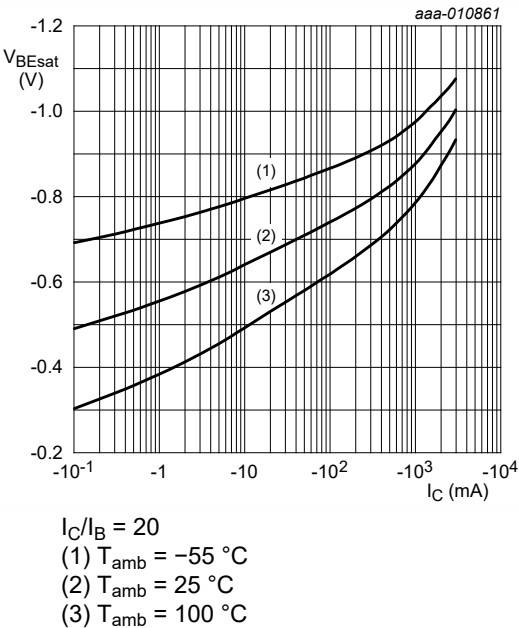


Fig. 15. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

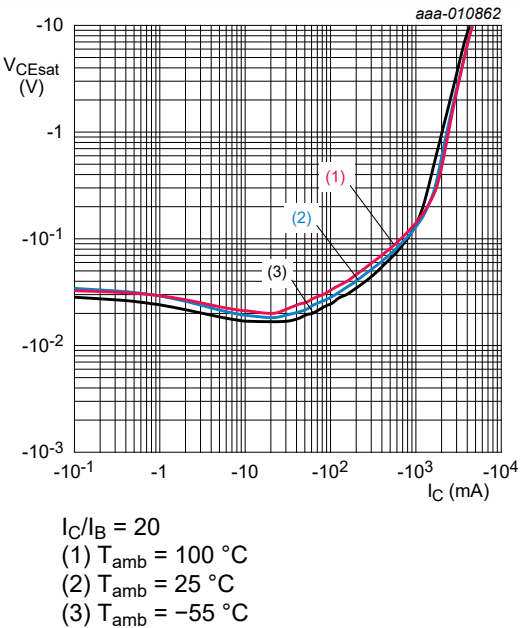


Fig. 16. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

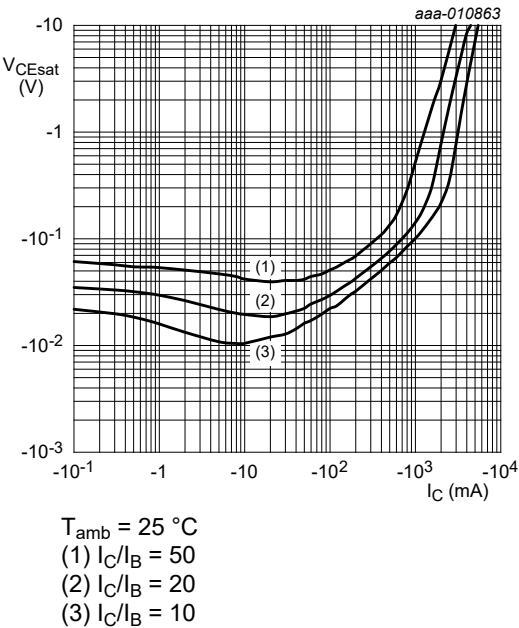


Fig. 17. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

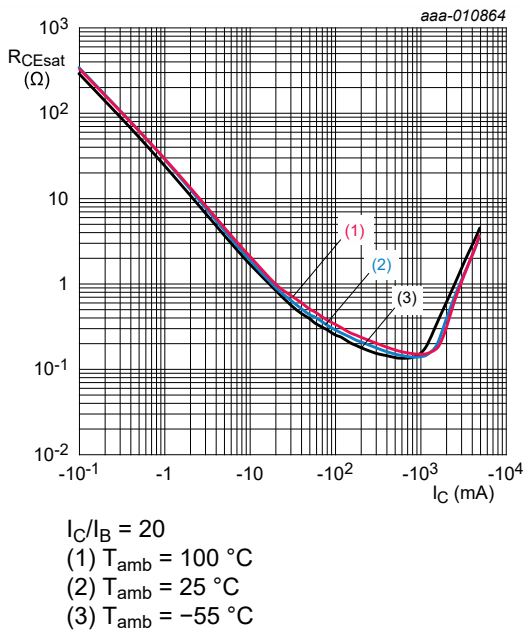


Fig. 18. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

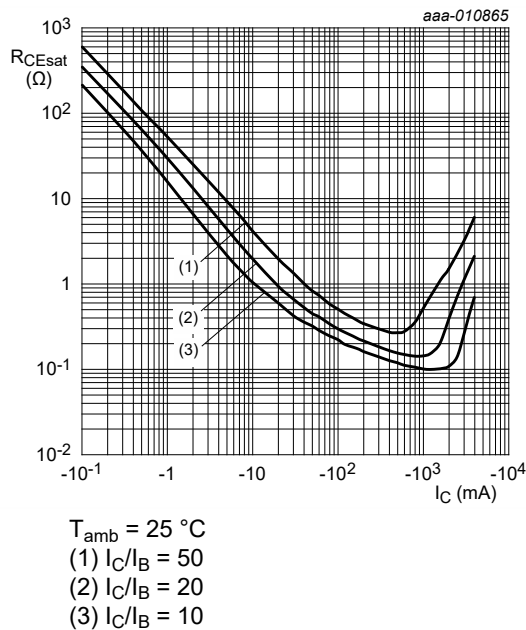


Fig. 19. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

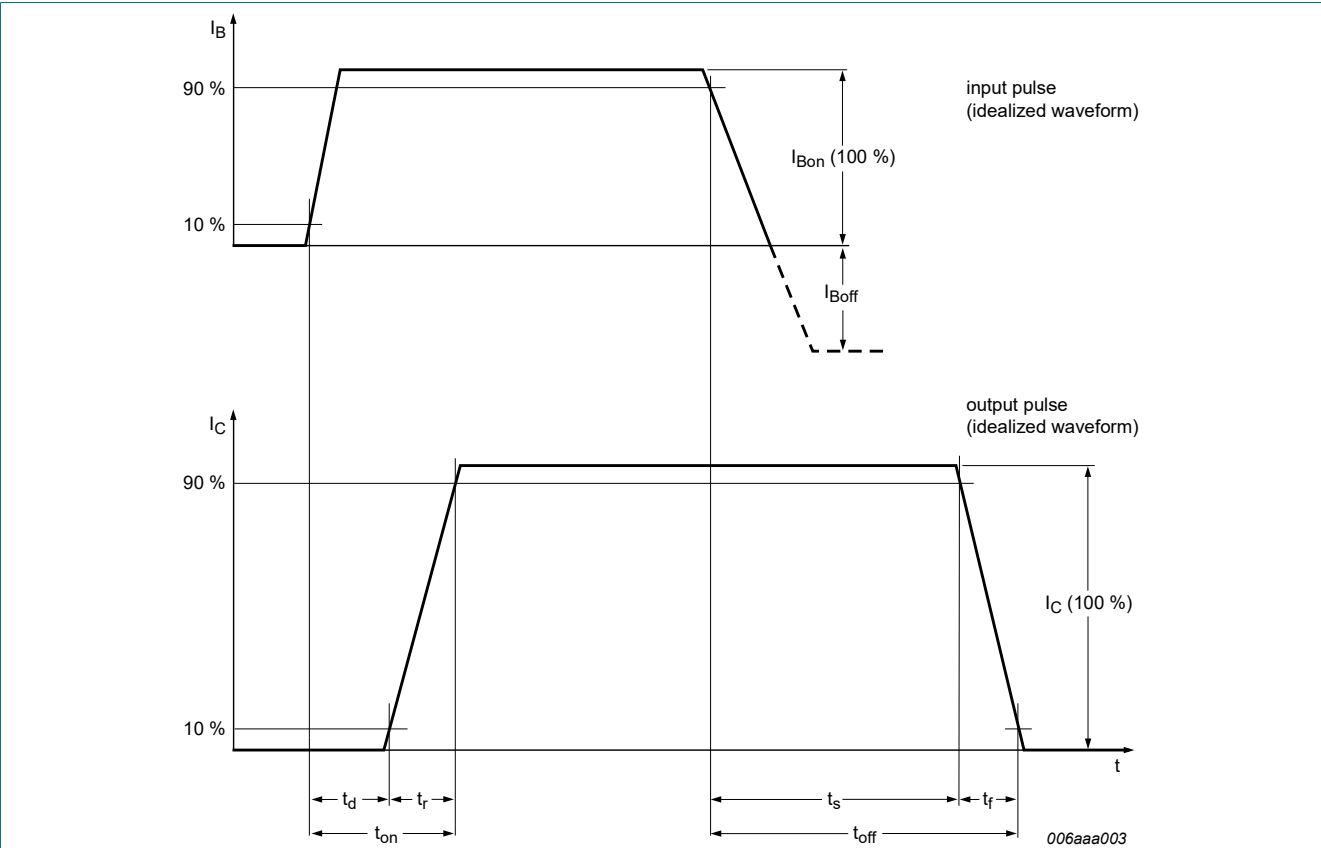


Fig. 20. TR1 (NPN): BISS transistor switching time definition

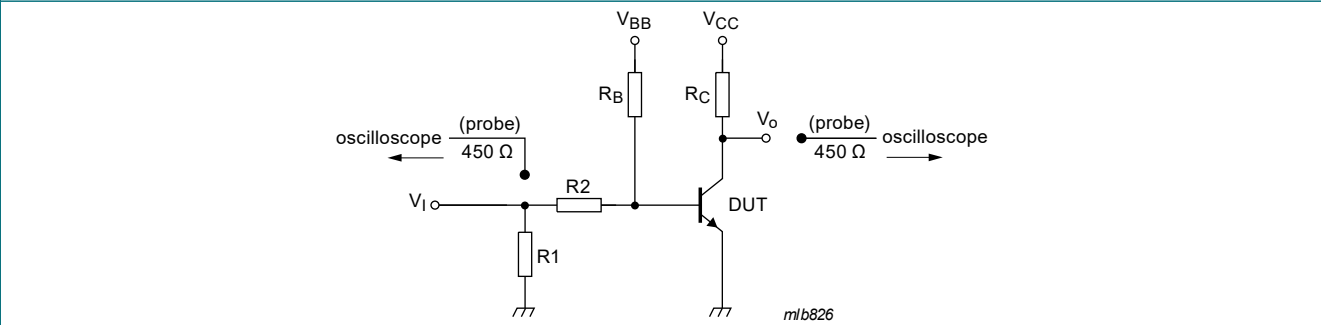


Fig. 21. TR1 (NPN): Test circuit for switching times

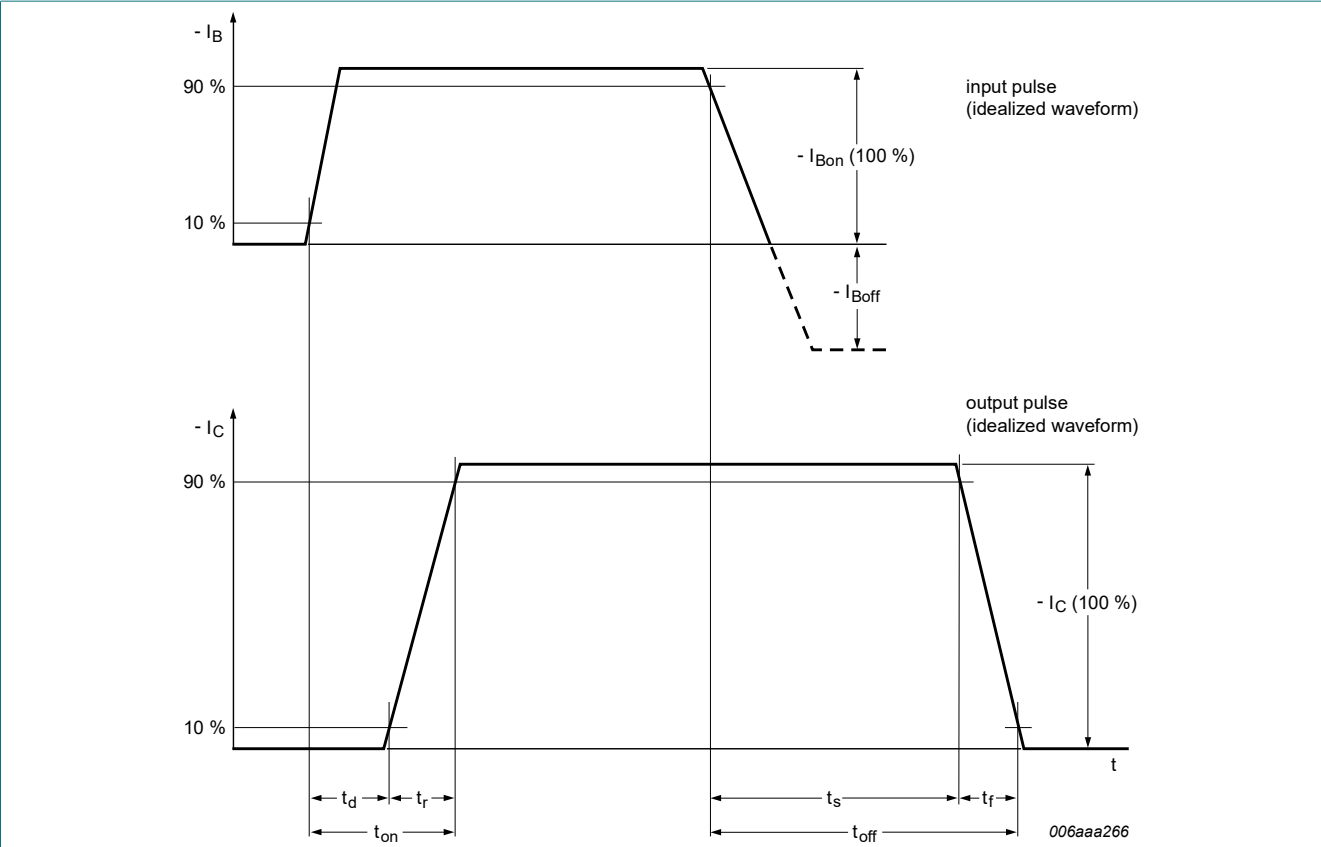


Fig. 22. TR2 (PNP): BISS transistor switching time definition

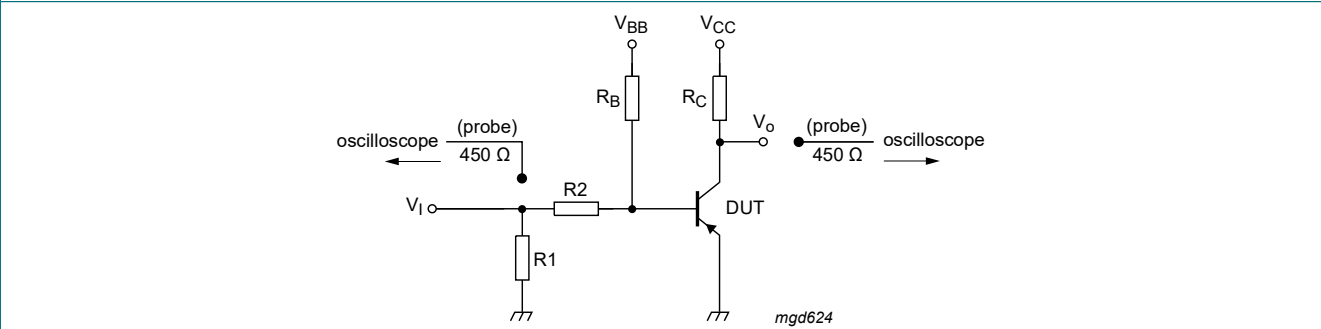
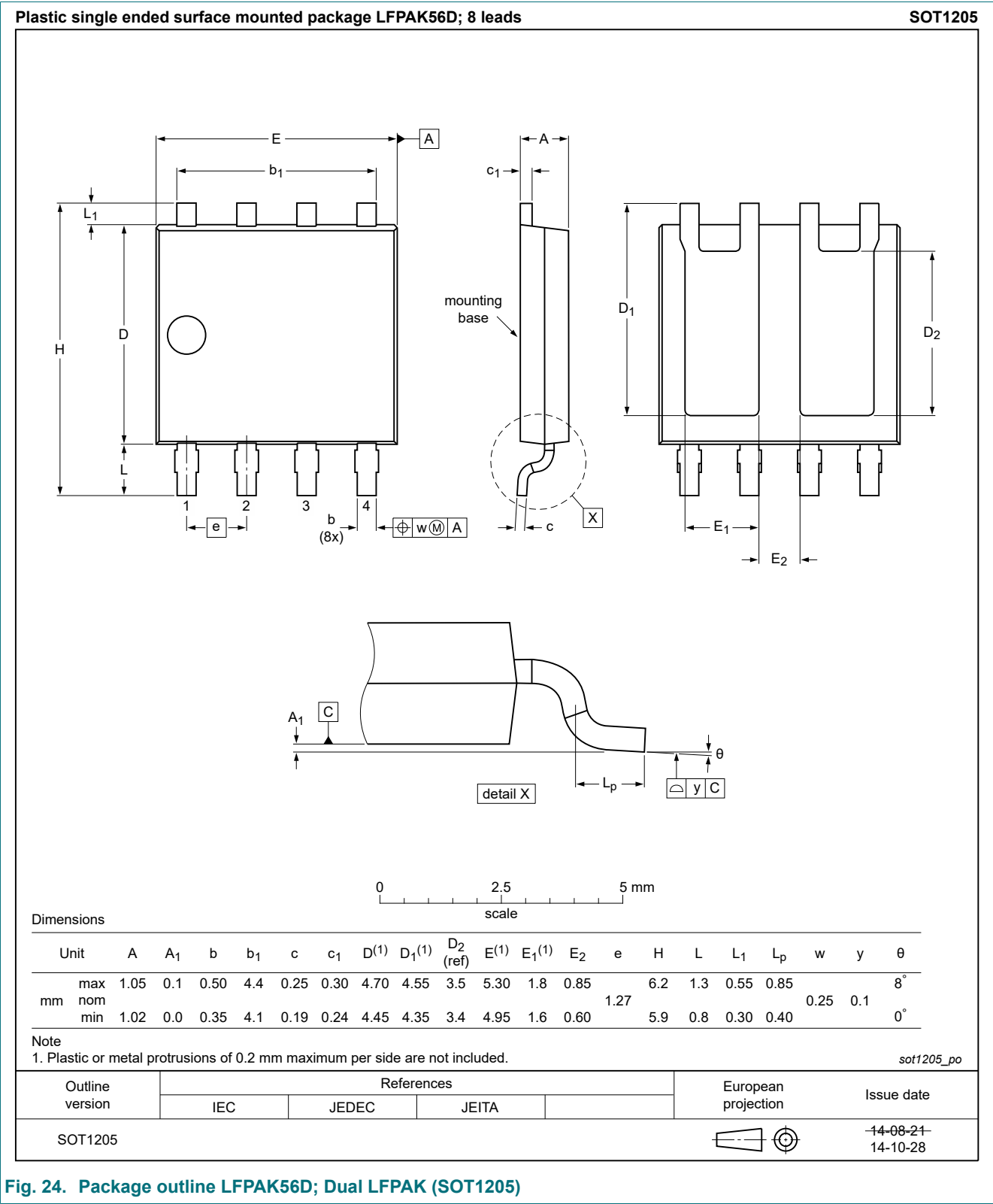


Fig. 23. TR2 (PNP): Test circuit for switching times

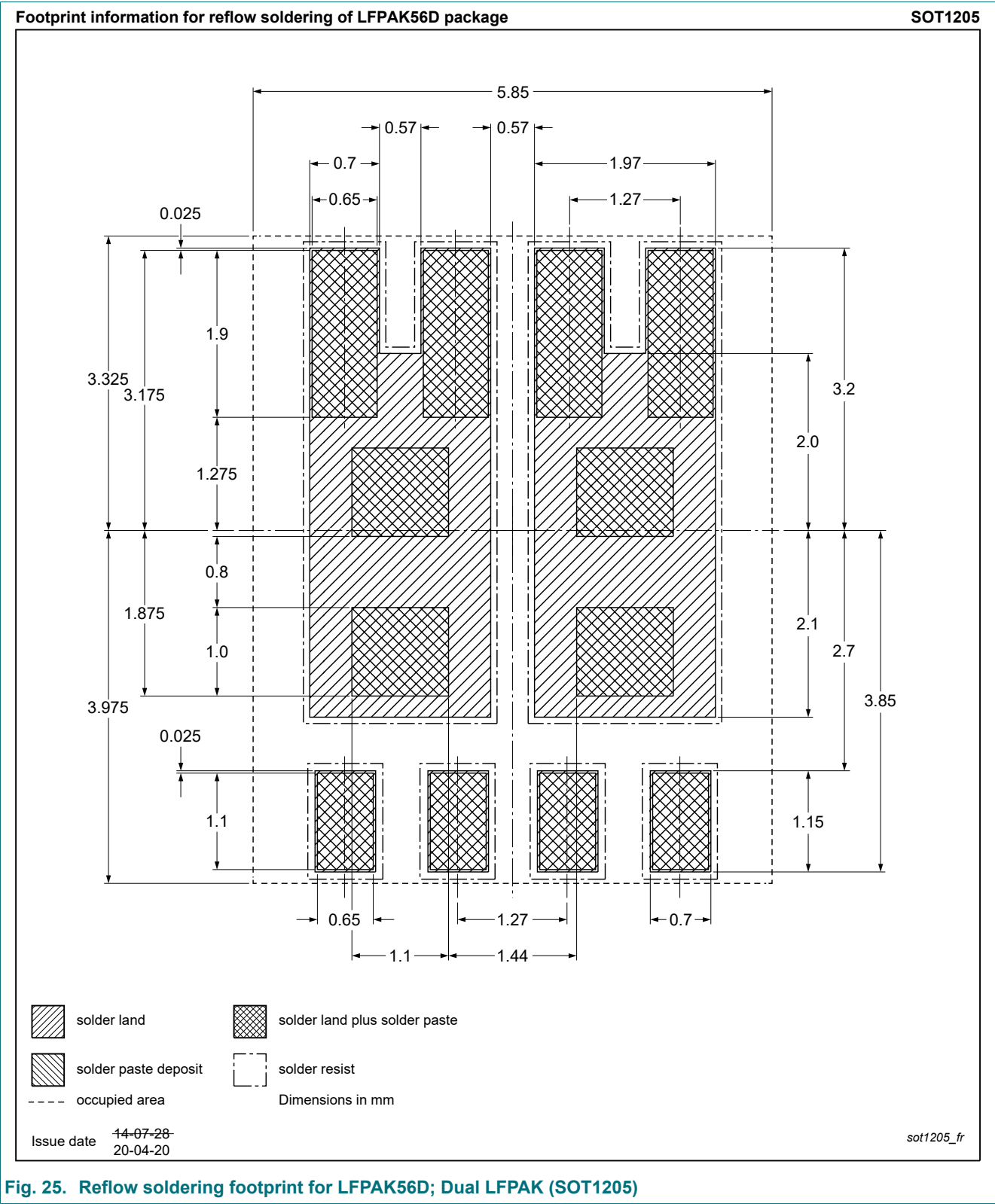
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT610030NPK-Q v.1	20241025	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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