



# PSMNR90-80ASF

NextPower 80 V, 0.85 mOhm, N-channel MOSFET in  
CCPAK1212 package

29 October 2024

Product data sheet

## 1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for high power industrial and consumer applications.

## 2. Features and benefits

- Low  $Q_{rr}$  for higher efficiency and lower spiking
- 505 Amps  $I_{D(max)}$  continuous current rating
- Low  $Q_G \times R_{DS(on)}$  FOM for high efficiency switching applications
- Strong avalanche energy rating ( $E_{as}$ )
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant CCPAK1212 package

## 3. Applications

- Battery protection
- High power full and half-bridge configurations
- BLDC motor control
- OR-ing

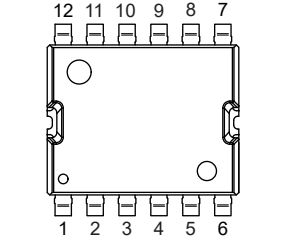
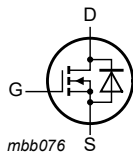
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	505	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	1.55	kW
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>	-	0.67	0.85	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	12	42	96	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 40\text{ V}; T_j = 25\text{ °C};$ <a href="#">Fig. 17</a>	-	94	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>CCPAK1212 (SOT8000A)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-80ASF	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-80ASF	XPF90S80A

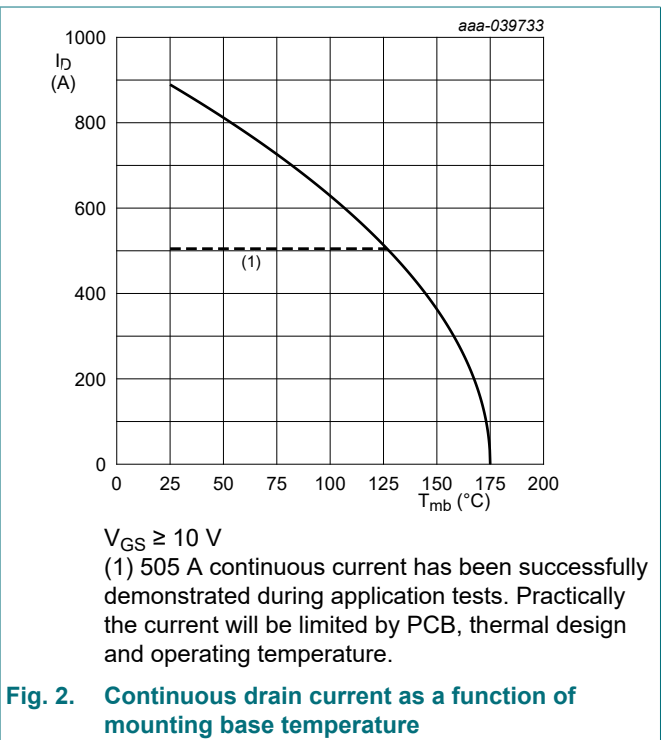
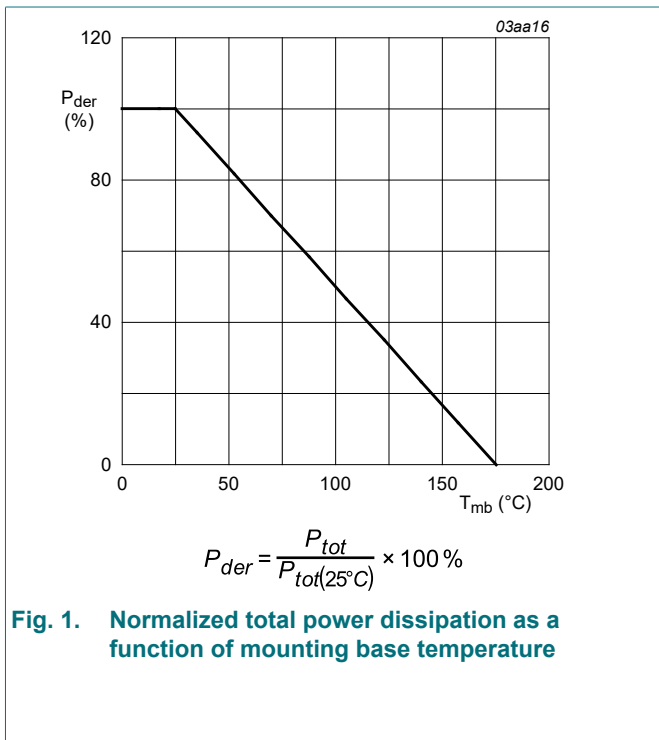
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	80	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	80	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1	-	1.55	kW
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	-	505	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2	-	505	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3	-	3558	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	505	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	3558	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 129 A; V <sub>sup</sub> ≤ 80 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 282 μs; Fig. 4	[1]	-	1890 mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 80 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω; Fig. 4	[1]	-	129 A

[1] Protected by 100% test



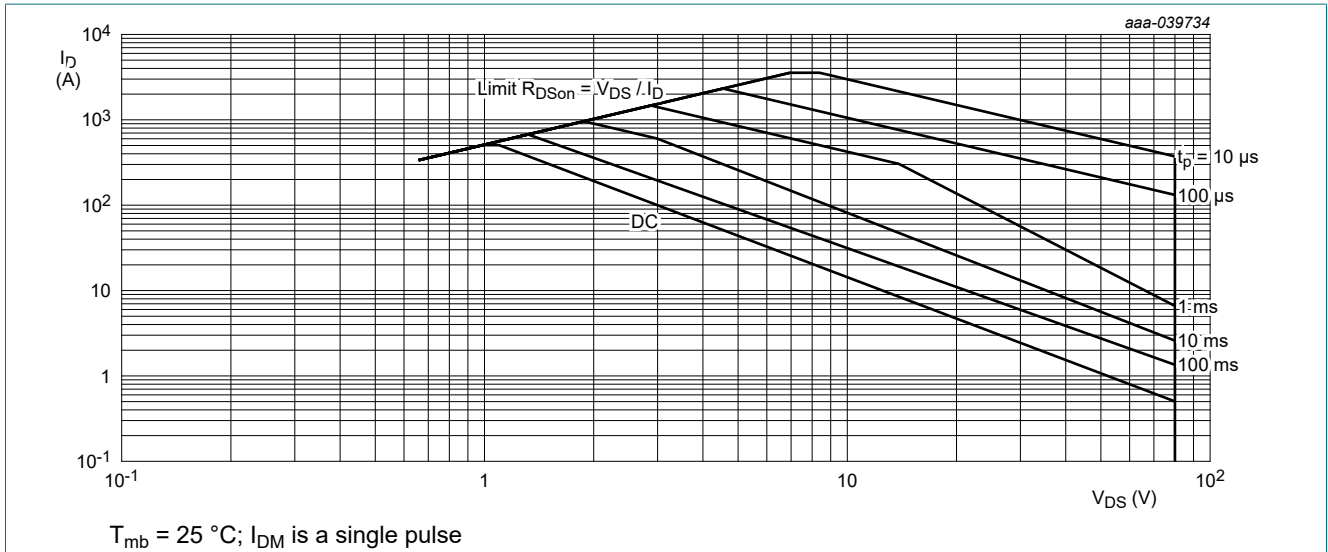


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

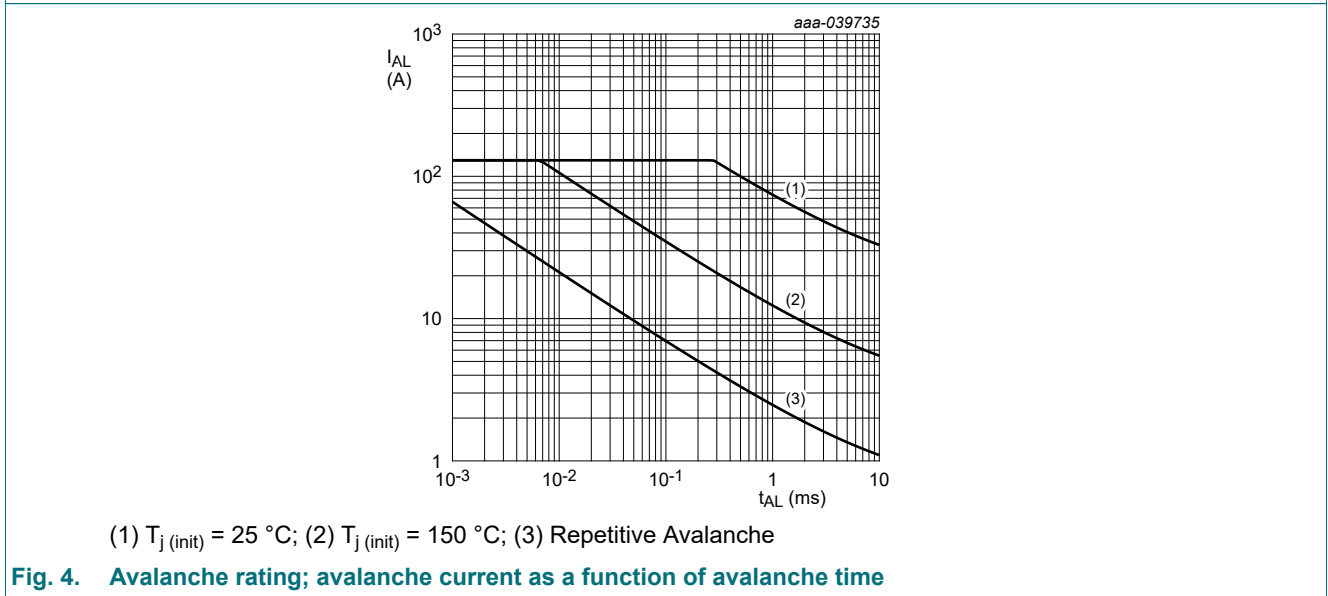


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.075	0.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 6</a>	-	58	-	K/W
		<a href="#">Fig. 7</a>	-	29	-	K/W

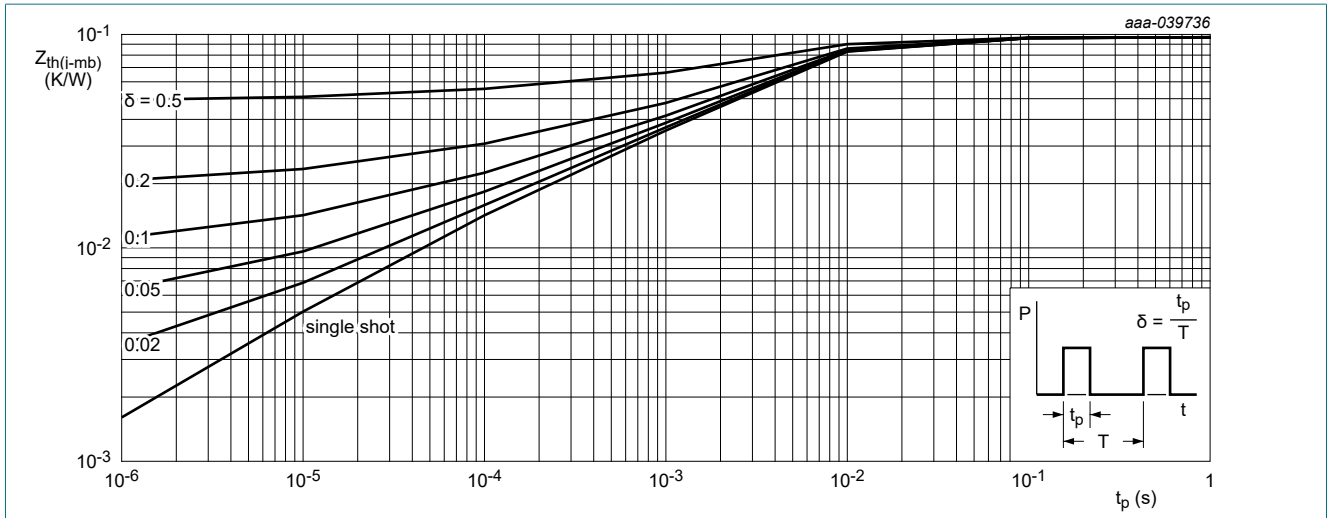
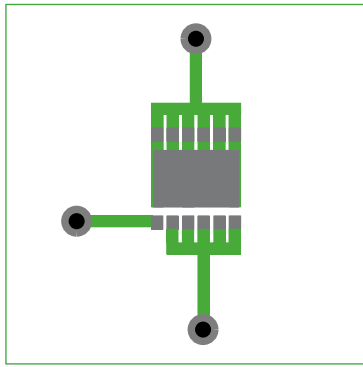


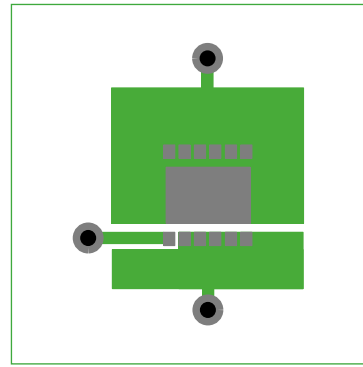
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-040397

70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient



aaa-040398

Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 7. PCB layout for thermal resistance from junction to ambient

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.56	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-9.28	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.22	2	$\mu A$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	49	200	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 11</a>	-	0.67	0.85	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	1	1.3	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	1.4	2	m $\Omega$
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 11</a>	-	0.81	1.22	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.68	1.35	2.7	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	154	309	463	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$	-	284	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	58	97	136	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	66.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	31.2	-	nC
$Q_{GD}$	gate-drain charge		12	42	96	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	4.3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 15</a>	13764	22939	32115	pF
$C_{oss}$	output capacitance		3685	6142	9827	pF
$C_{rss}$	reverse transfer capacitance		9	93	278	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	91	-	ns
$t_r$	rise time		-	69	-	ns
$t_{d(off)}$	turn-off delay time		-	203	-	ns
$t_f$	fall time		-	91	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 16</a>	-	0.74	1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;	-	77	-	ns
$Q_r$	recovered charge	$V_{DS} = 40 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; Fig. 17	-	94	-	nC

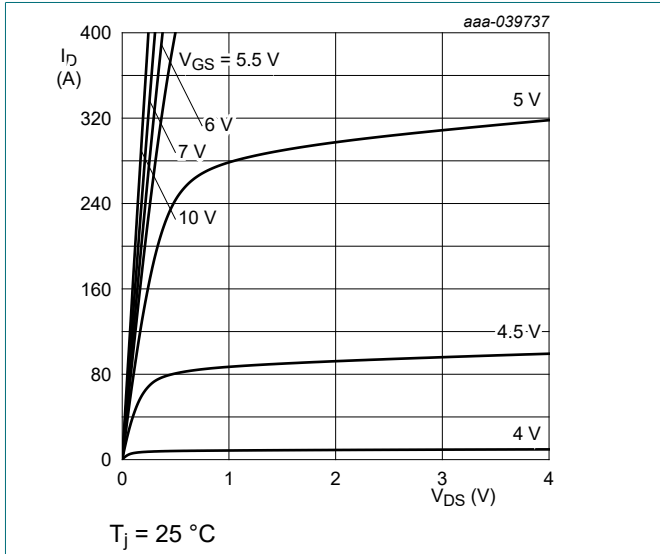


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

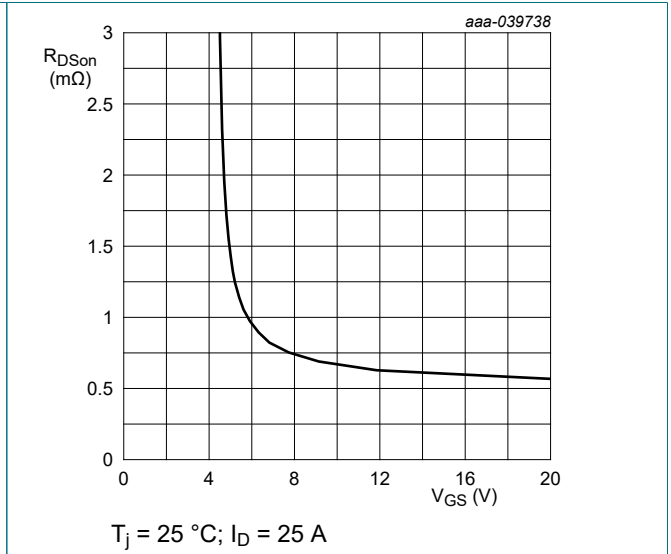


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

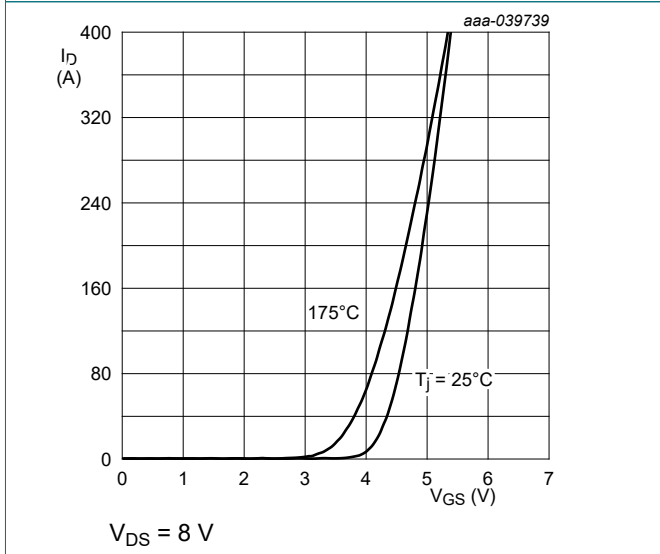


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

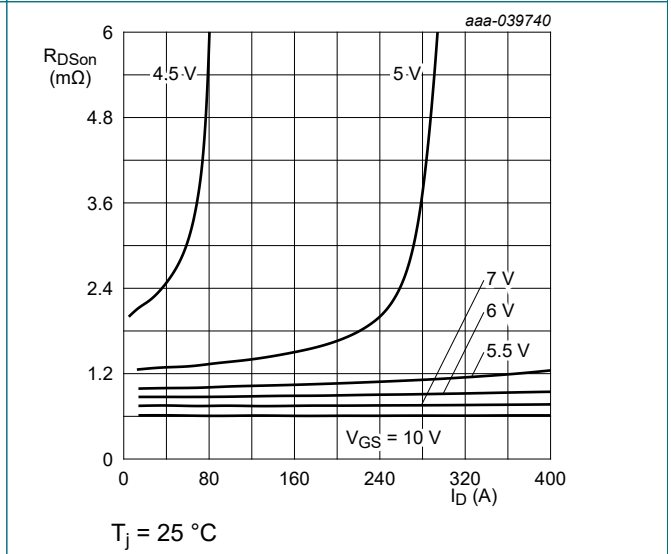
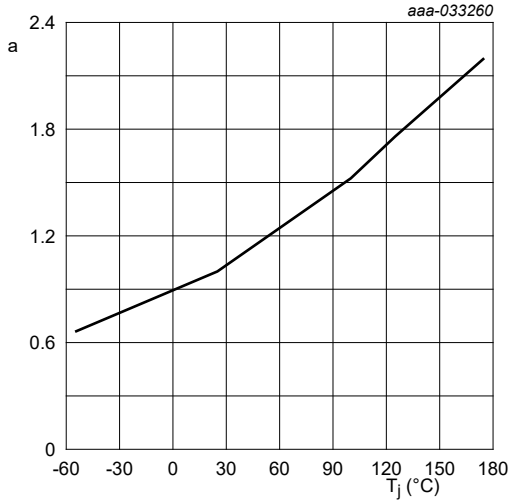
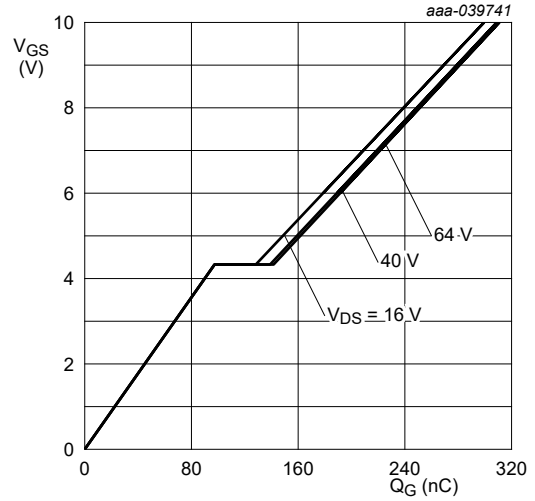


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

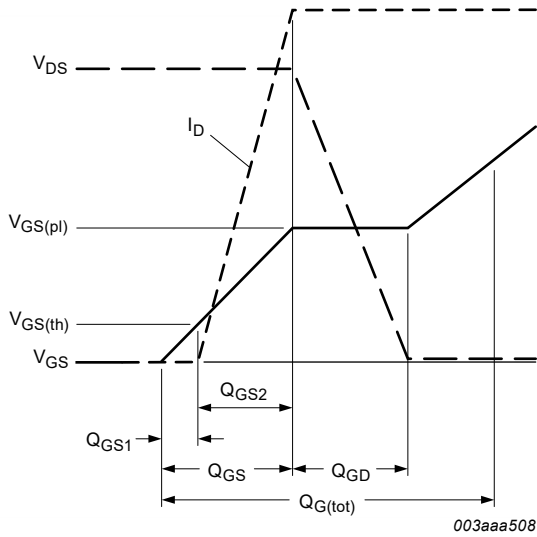
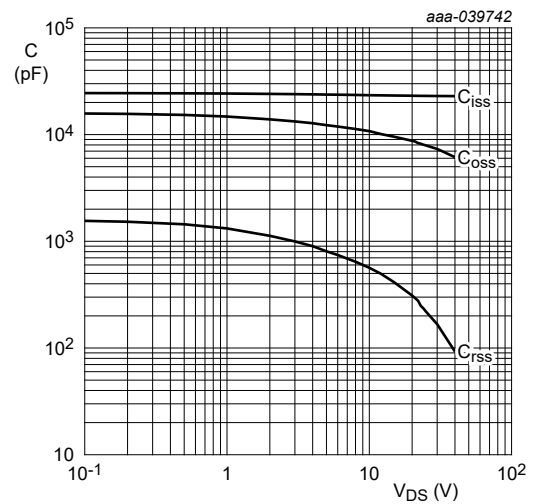
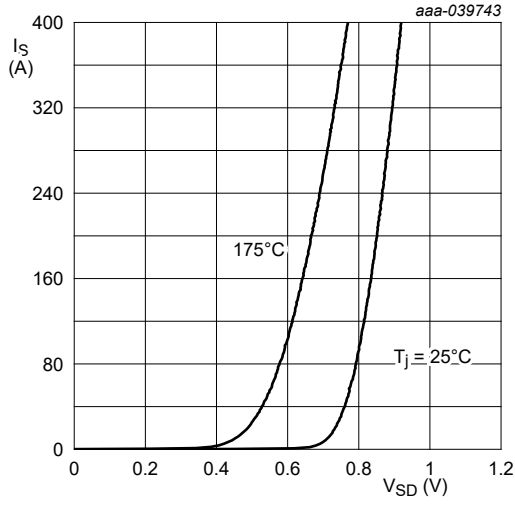


Fig. 14. Gate charge waveform definitions



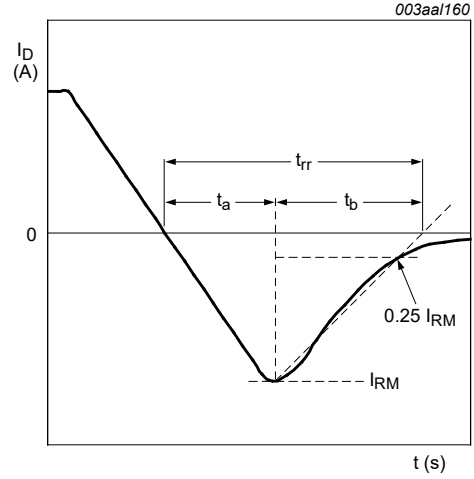
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

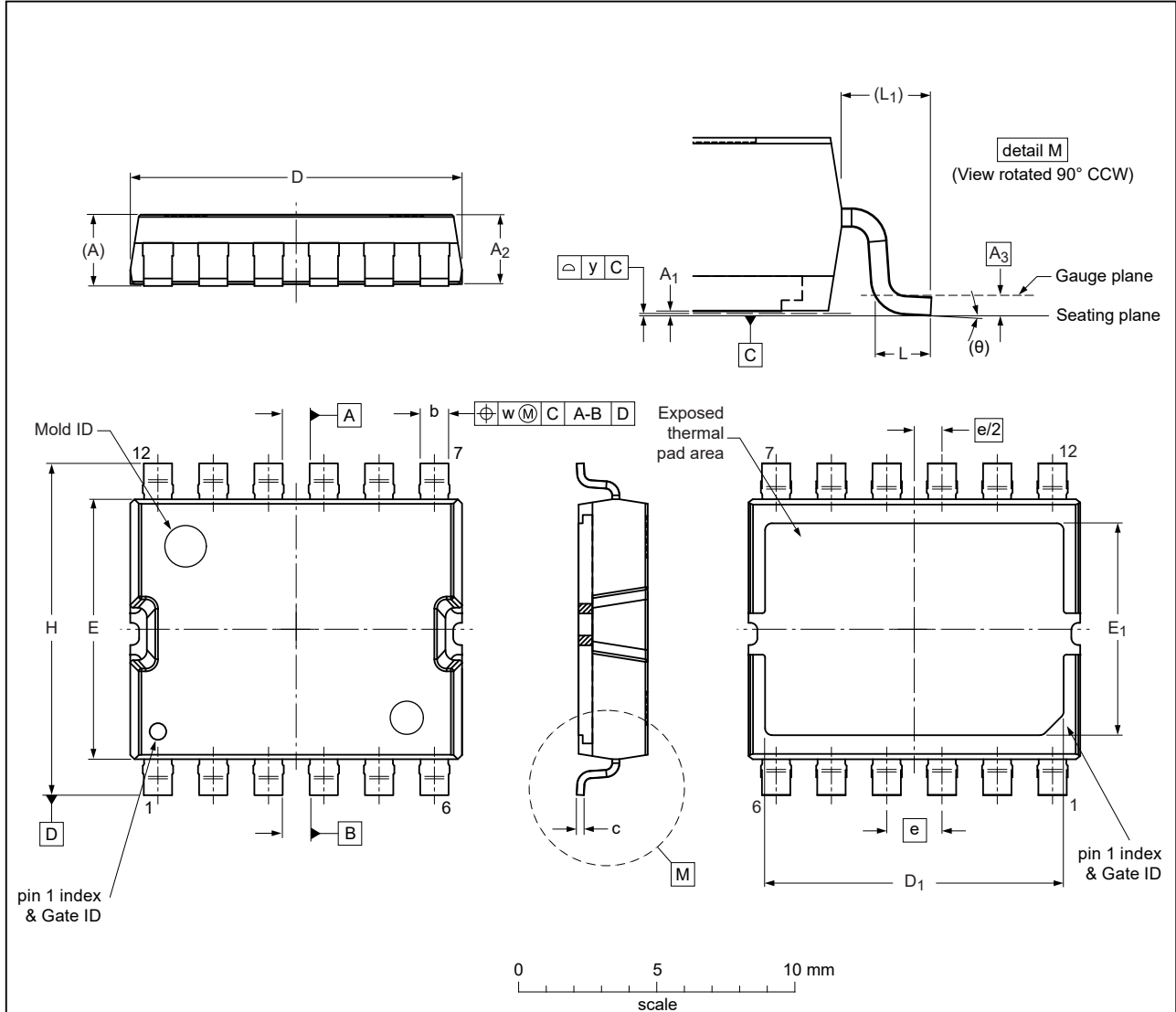


**Fig. 17. Reverse recovery timing definition**

11. Package outline

Plastic, surface mounted copper clip package (CCPAK1212);  
13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body

SOT8000A



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A(ref)	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	e	H	L	L <sub>1</sub> (ref)	w	y	θ(ref)	
max		0.13	2.65		1.12	0.30	12.15	10.95	9.55	7.40		12.15	1.0					
mm nom	2.75			0.25							2.0			1.3	0.20	0.1	4°	
min		0	2.4		0.93	0.22	11.85	10.65	9.25	7.10		11.85	0.6					

Note

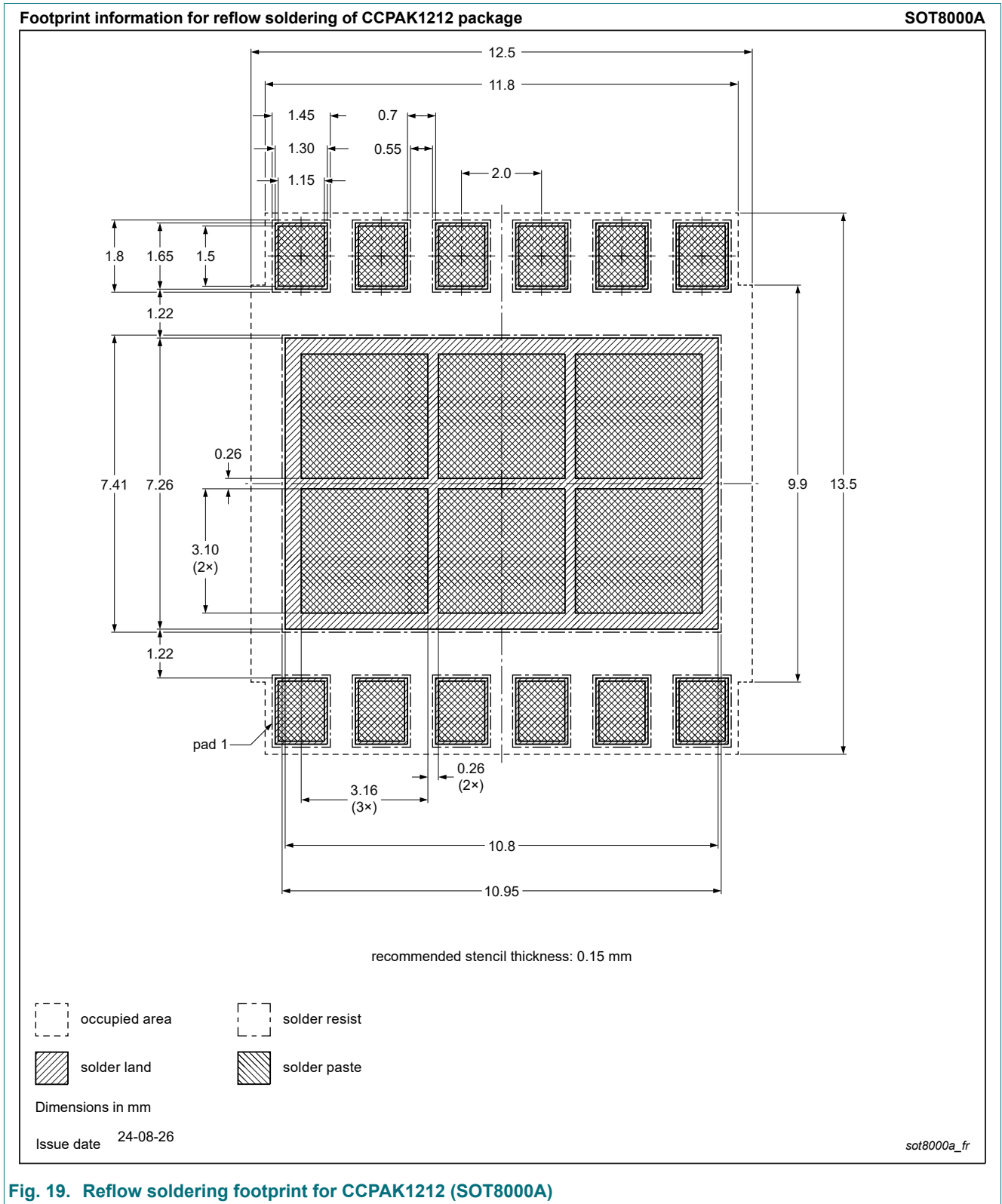
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included for dimension E.

sof8000a\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT8000A		MO-359			—23-12-12— 24-04-16

Fig. 18. Package outline CCPAK1212 (SOT8000A)

## 12. Soldering



**Fig. 19. Reflow soldering footprint for CCPAK1212 (SOT8000A)**

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 29 October 2024

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