



PSMNR70-40YSN

N-channel 40 V, 0.81 mOhm, ASFET for Battery System in LPAK56E

12 September 2024

Product data sheet

1. General description

ASFET for Battery System applications, characterized by low R_{DSon} and strong SOA capability for reduced I^2R conduction losses. ASFETs deliver high efficiency, reduced heat generation and superior handling of inrush current during transient and fault conditions.

2. Features and benefits

- 360 A continuous $I_{D(max)}$
- Strong SOA capability
- Avalanche rated, 100% tested at $I_{AS} = 190$ A
- High reliability LPAK (Power-SO8) package, qualified to 175 °C
- LPAK copper clip
- LPAK gull wing lead

3. Applications

- Battery management systems (BMS)
- eFuse
- Load-switch
- BLDC motor control
- High-performance power supply
- High-performance synchronous rectification

4. Quick reference data

Table 1. Quick reference data

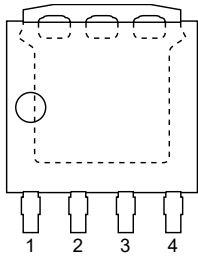
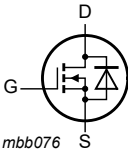
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	360	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	333	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12		0.5	0.72	0.81	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15		14	46	79	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ °C}$; Fig. 18	[2]	-	34	-	nC

[1] 360A Continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR70-40YSN	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR70-40YSN	N70S40J

8. Limiting values

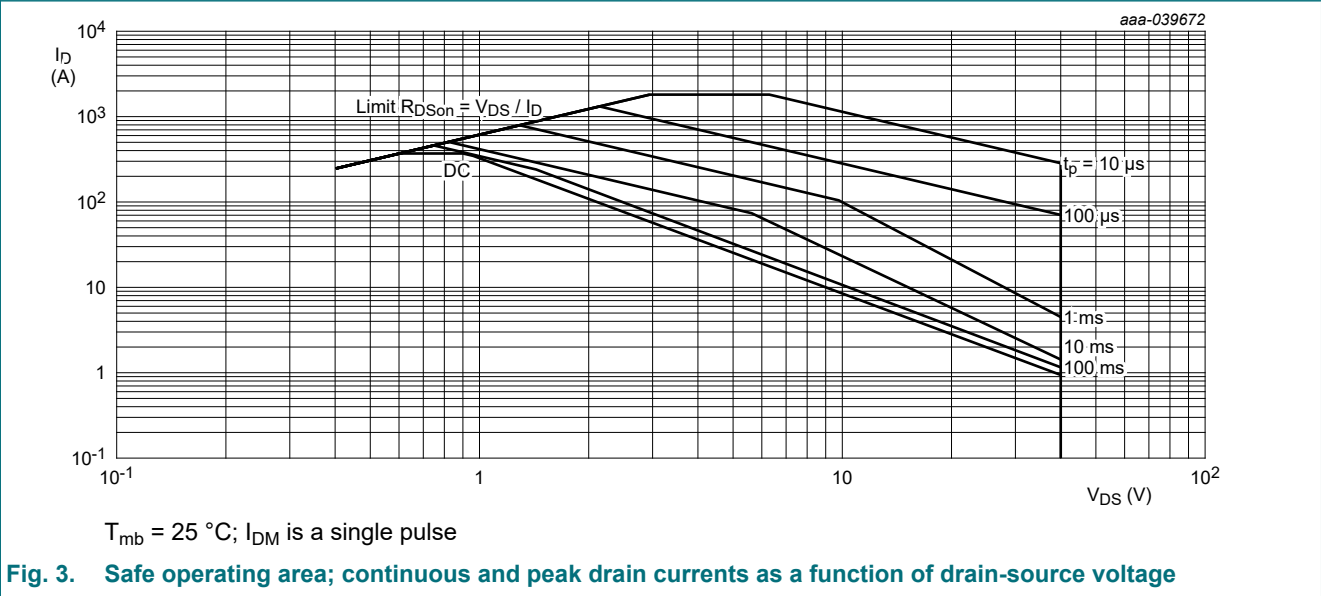
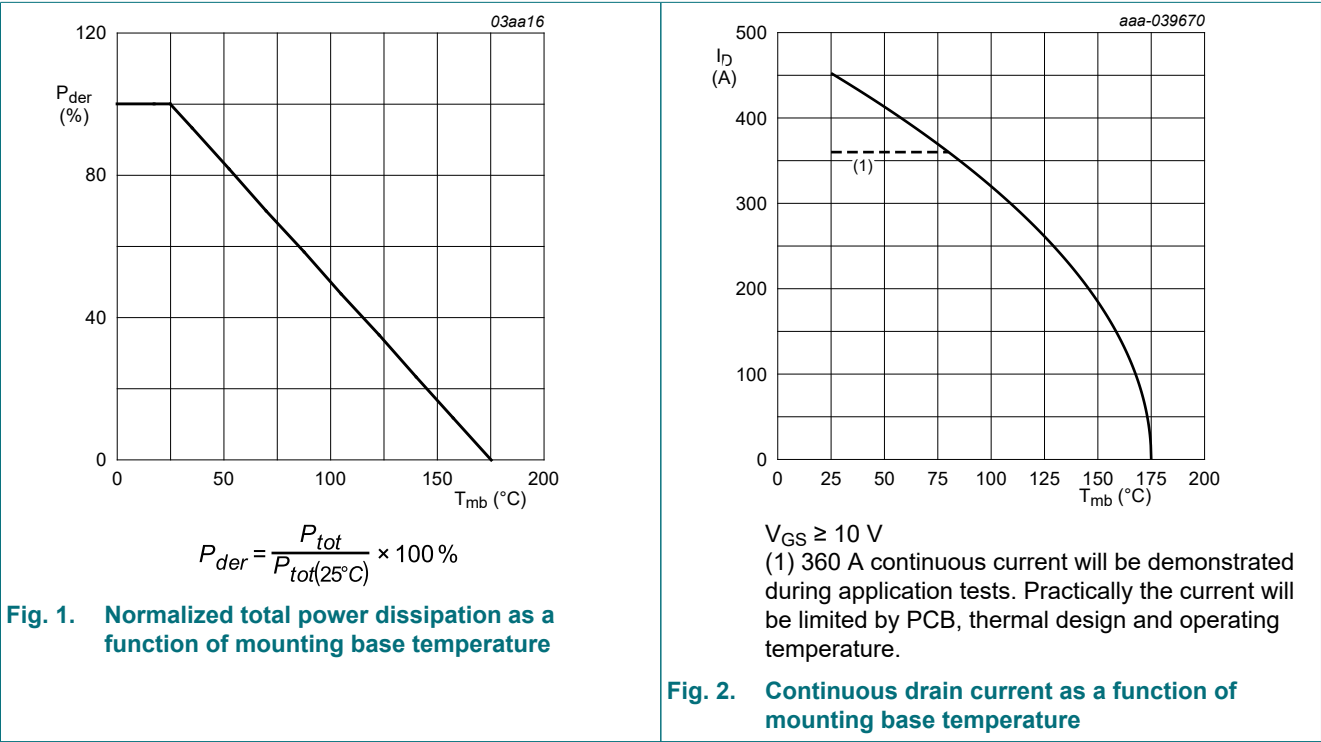
Table 5. Limiting values

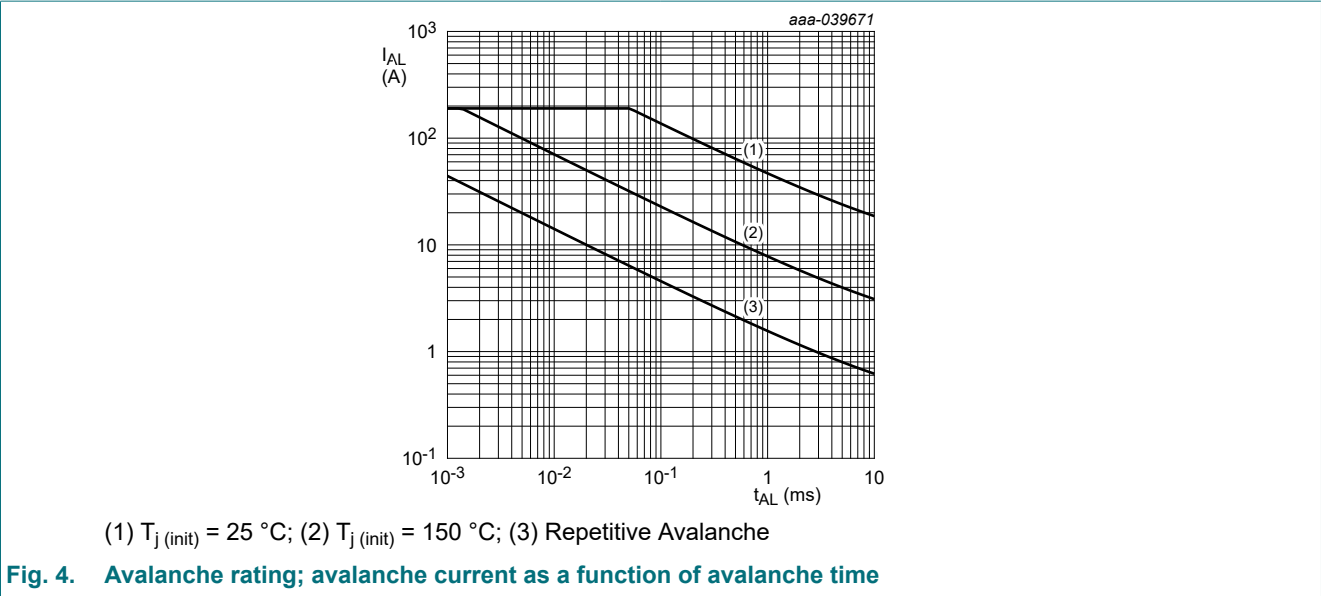
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V _{DSM}	peak drain-source voltage	t _p ≤ 20 ns; f ≤ 500 kHz; E _{DS(AL)} ≤ 200 nJ; single pulse		-	45	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	333	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	360	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	320	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1810	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	333	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1810	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 80.8\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 304\text{ }\mu\text{s}$; Fig. 4	[2]	-	638	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[2]	-	190	A

- [1] 360A Continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

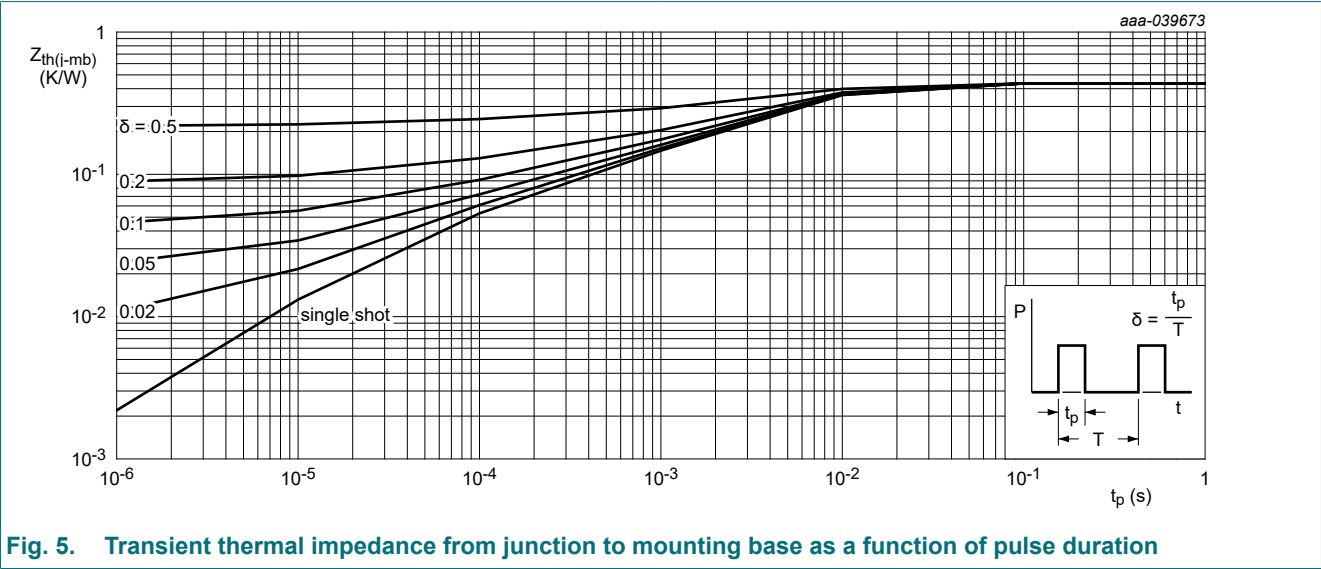


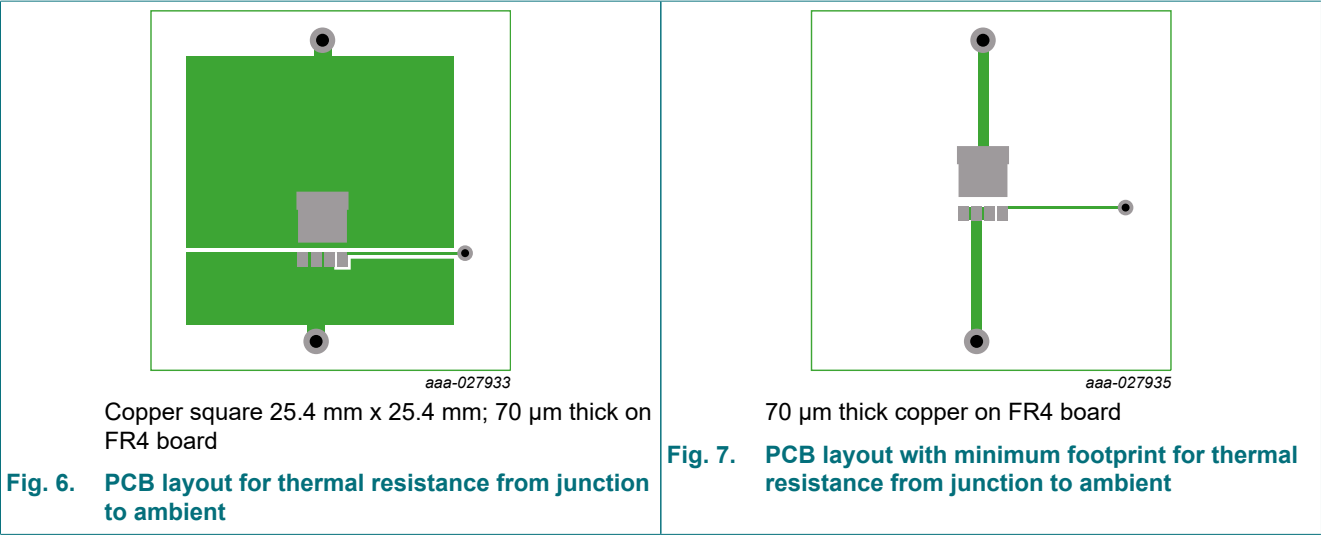


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.4	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	42	-	K/W
		Fig. 7	-	85	-	K/W





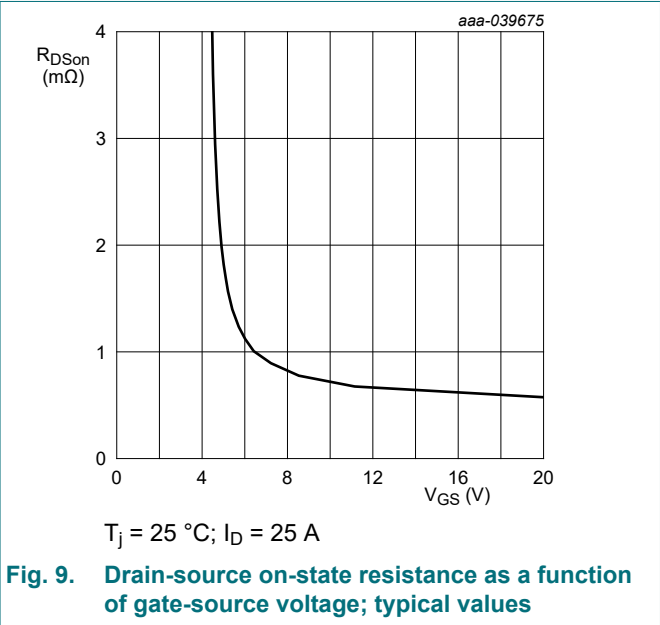
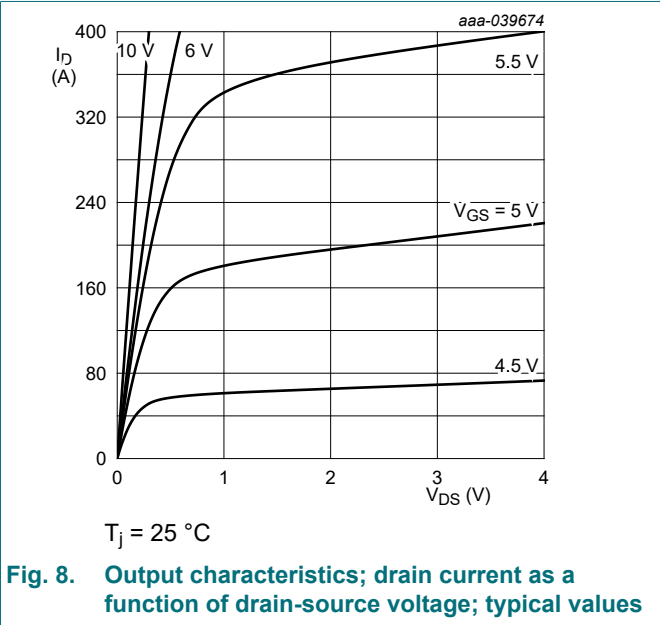
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	40	43	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	36	41	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 11	2.4	2.9	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C	-	3.4	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C	-	1.9	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 175 °C	-	-7.4	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C	-	0.1	1	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _J = 125 °C	-	1.2	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12	0.5	0.72	0.81	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 105 °C; Fig. 13	0.69	1.02	1.22	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 125 °C; Fig. 13	0.74	1.12	1.33	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 13	0.88	1.36	1.67	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C	0.3	0.78	2	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15	101	168	235	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C	-	136	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14 ; Fig. 15		20	37	54	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			14	25	36	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			6.6	12	17	nC
Q_{GD}	gate-drain charge			14	46	79	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14 ; Fig. 15		-	4.3	-	V
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 16		6152	10253	14355	pF
C_{oss}	output capacitance			1540	2200	2861	pF
C_{rss}	reverse transfer capacitance			351	877	1404	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$; $T_j = 25\text{ }^{\circ}\text{C}$		-	30	-	ns
t_r	rise time			-	51	-	ns
$t_{d(off)}$	turn-off delay time			-	96	-	ns
t_f	fall time			-	66	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	67	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 17		-	0.78	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	39	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 18	[1]	-	34	-	nC

[1] includes capacitive recovery



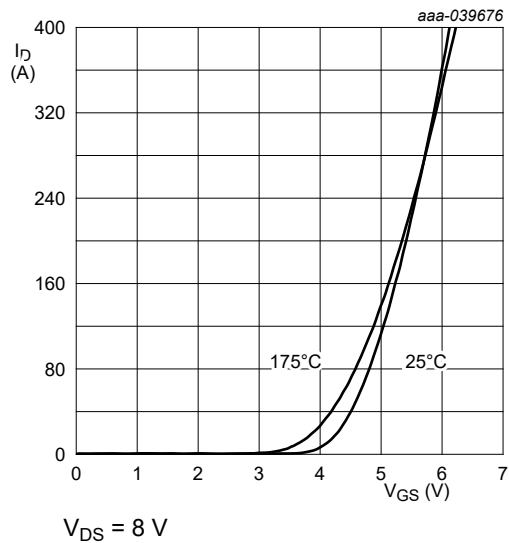


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

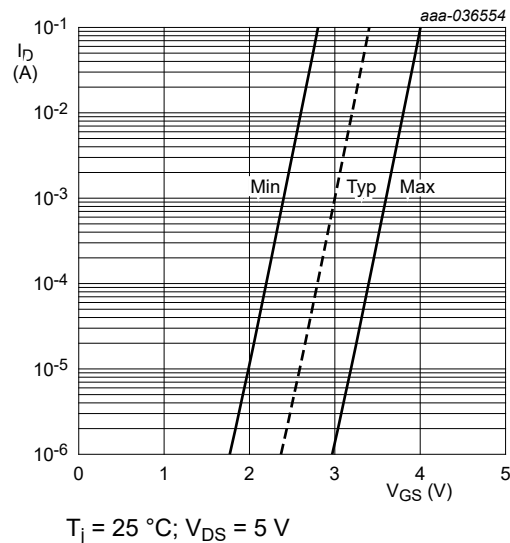


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

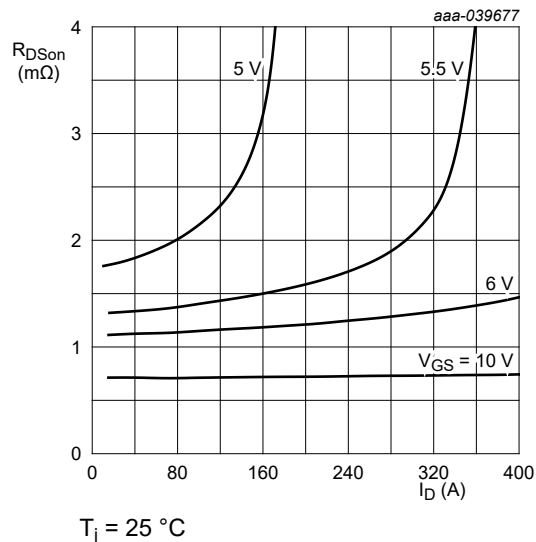


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

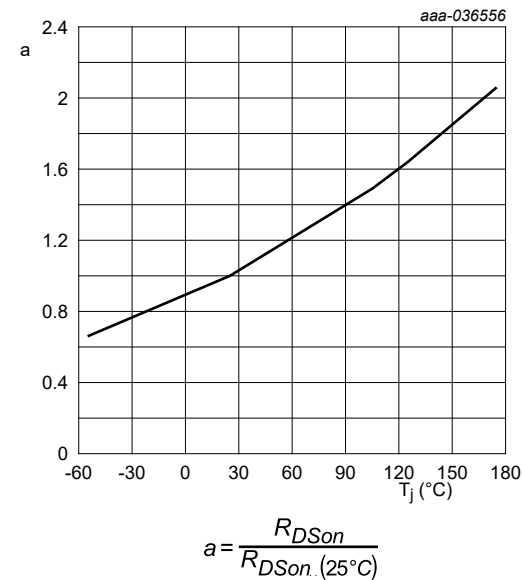


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

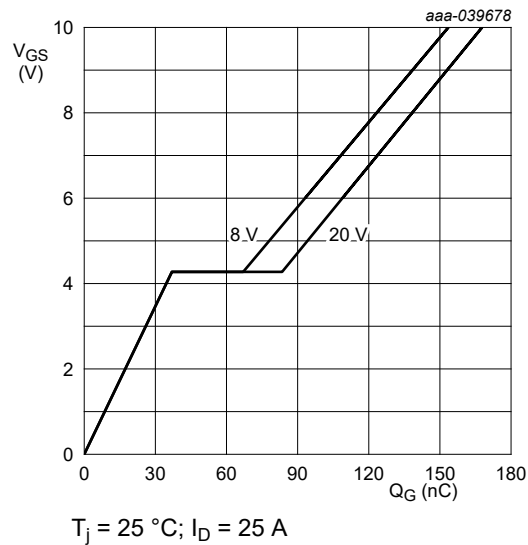


Fig. 14. Gate-source voltage as a function of gate charge; typical values

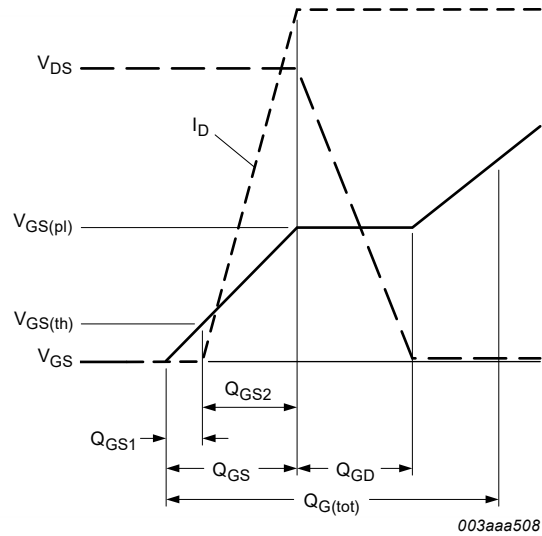


Fig. 15. Gate charge waveform definitions

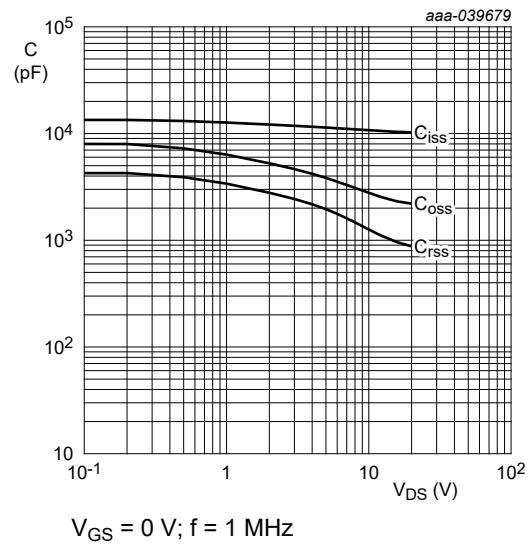


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

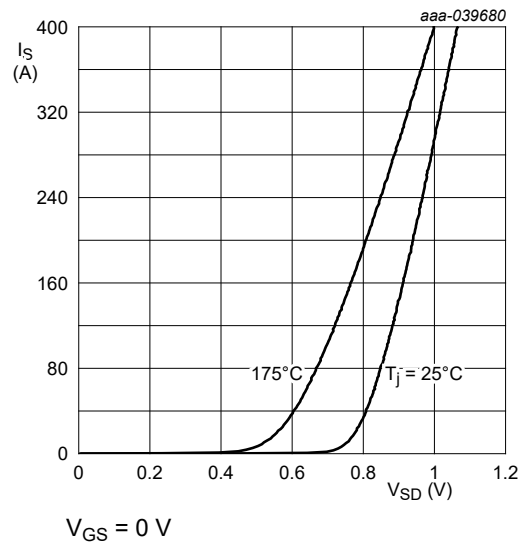


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

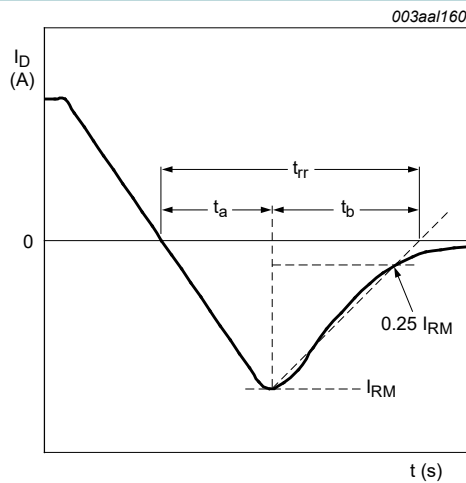


Fig. 18. Reverse recovery timing definition

11. Package outline

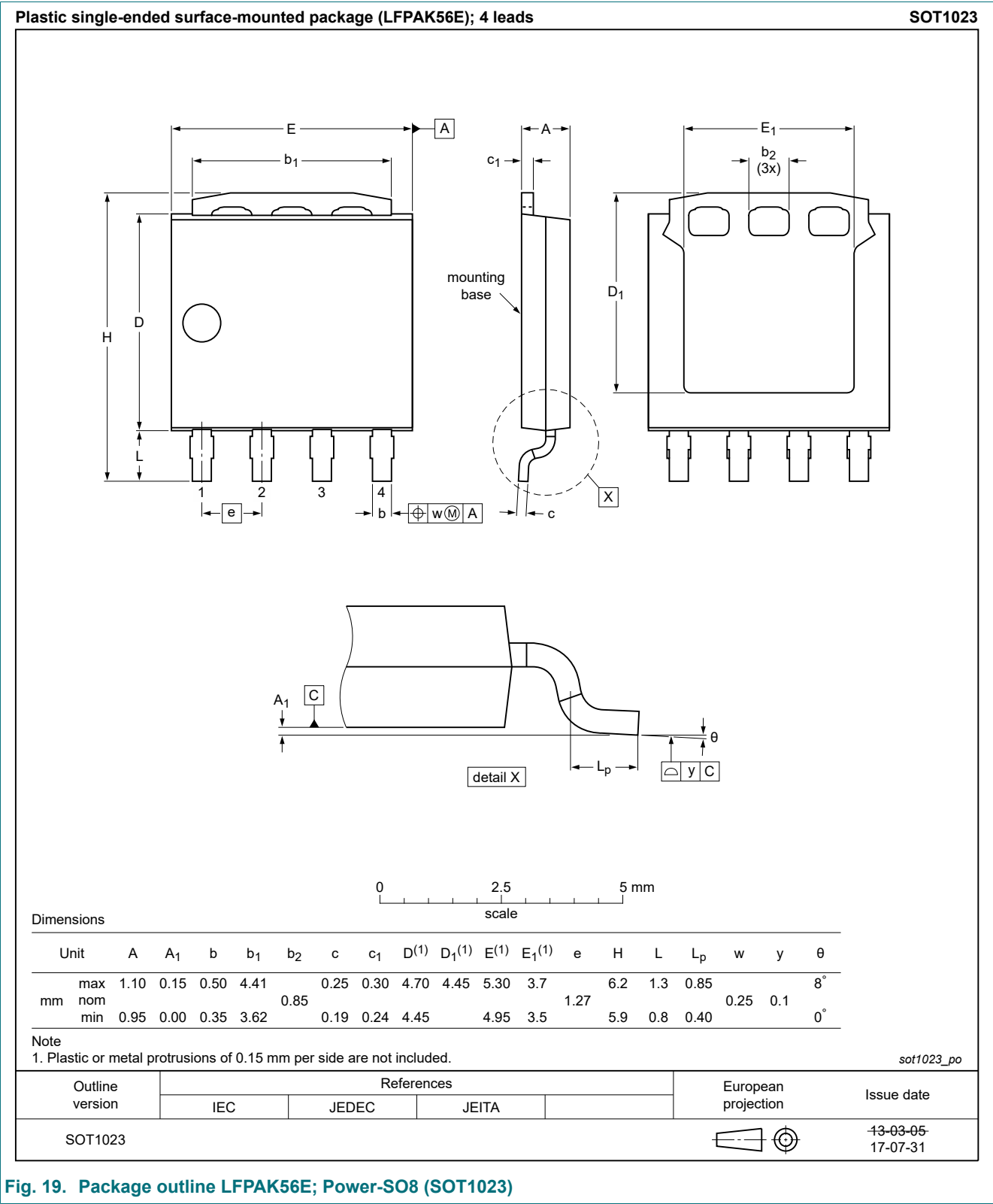


Fig. 19. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

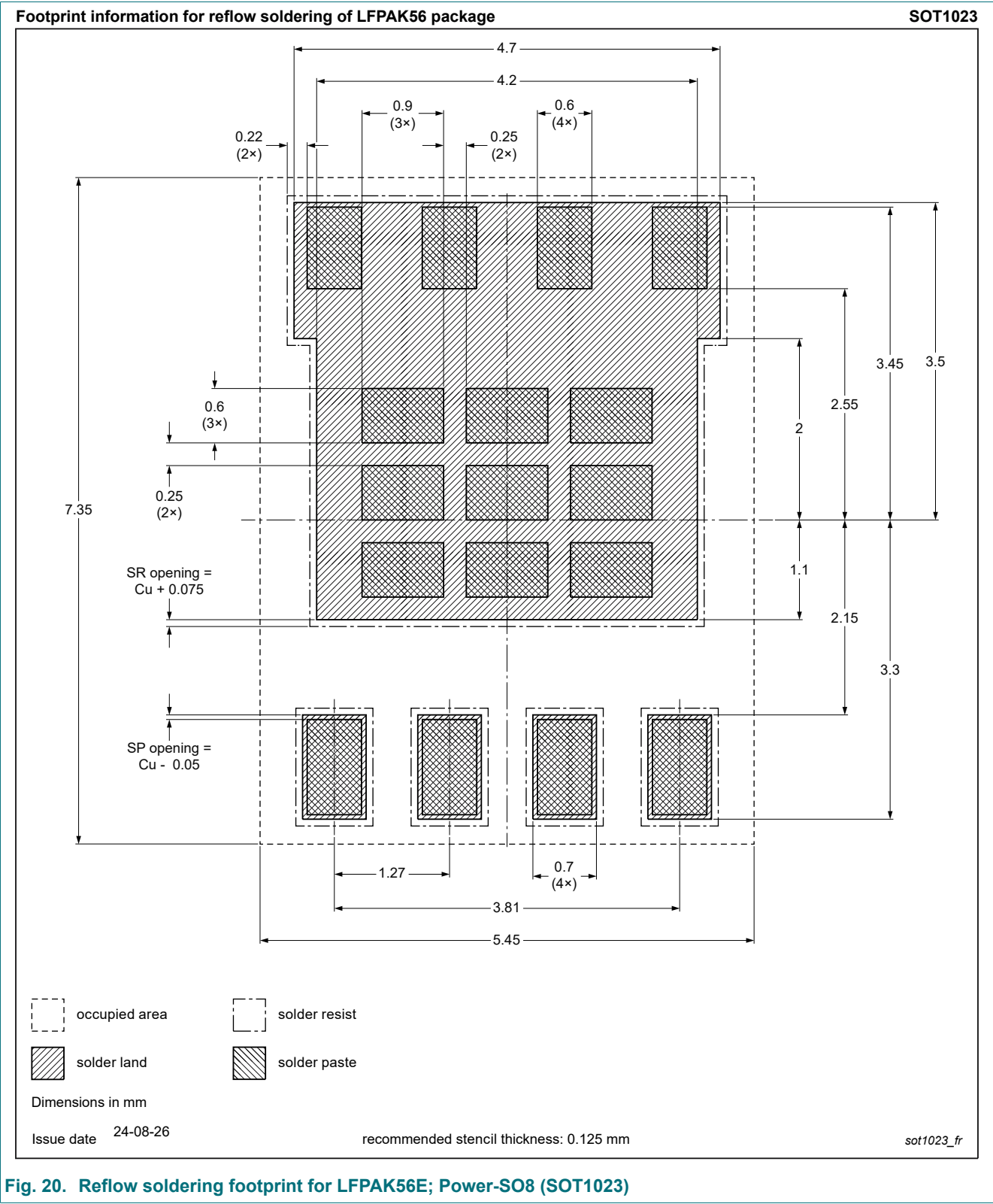


Fig. 20. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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