

ICM-45605 HIGHLIGHTS

The ICM-45605 is a high performance 6-axis MEMS MotionTracking device. It has a configurable host interface that supports I3CSM, I²C and SPI serial communication, and an I²C master mode interface for connection to external sensors. The device features up to 8Kbytes FIFO and 2 programmable interrupts.

The ICM-45605 supports the lowest gyro and accel sensor noise in this IMU class, and has the highest stability against temperature, shock (up to 20,000g) or SMT/bend induced offset as well as immunity against out-of-band vibration induced noise. Other industry-leading features include InvenSense on-chip APEX Motion Processing engine for gesture recognition, activity classification, and pedometer, along with programmable digital filters, and an embedded temperature sensor.

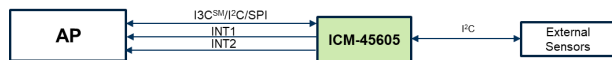
FEATURES

- Gyroscope Noise: 3.8 mdps/ $\sqrt{\text{Hz}}$ & Accelerometer Noise: 70 $\mu\text{g}/\sqrt{\text{Hz}}$
 - Low-Noise mode 6-axis current consumption of 0.42 mA at 1600Hz
- User selectable Gyro Full-scale range (dps): $\pm 15.625/\pm 31.25/\pm 62.5/\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000$
- User selectable Accelerometer Full-scale range (g): $\pm 2/\pm 4/\pm 8/\pm 16$
- User configurable internal pull-up/pull-downs included on I/O interfaces to reduce system costs associated with external pull-ups/pull-downs
- User configurable Output Data Rate (ODR) and FIFO Data Rate (FDR)
- User-programmable digital filters for gyro, accel, and temp sensor
- APEX Motion Functions:
 - Pedometer, Tilt Detection, Single/Double Tap Detection, Raise to Wake, Wake on Motion
 - Free-Fall Detection, Significant Motion Detection, Low-G Detection, High-G Detection
- Host interface: 12.9 MHz I3CSM, 1 MHz I²C, 24 MHz SPI

APPLICATIONS

- Game Controllers, Cameras, IoT, Drones, Non-OIS Smartphones, Wearables, Hearables

BLOCK DIAGRAM



ORDERING INFORMATION

| PART | TEMP RANGE | PACKAGE |
|------------|----------------|-----------------------|
| ICM-45605† | -40°C to +85°C | 2.5x3mm 14-Pin LGA |

† Denotes RoHS and Green-Compliant Package

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-45605 Dual-Interface MotionTracking device. The device is housed in a small 2.5x3x0.81 mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-45605 is a 6-axis MotionTracking device with a configurable host interface that supports I3CSM, I²C and SPI serial communication, and an I²C master mode interface for connection to external sensors. It combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.81 mm (14-pin LGA) package.

ICM-45605 also features up to 8Kbytes FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-45605, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports independently programmable full-scale range settings from ± 15.625 dps to ± 2000 dps for the UI path, and the accelerometer supports independently programmable full-scale range settings from ± 2 g to ± 16 g for the UI path.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3CSM, I²C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range of 1.08V to 3.6V.

The host interface can be configured to support I3CSM slave, I²C slave, or SPI slave modes. The I3CSM interface supports speeds up to 12.9MHz (data rates up to 12.9Mbps in SDR mode, 25.8Mbps in DDR mode), the I²C interface supports speeds up to 1MHz, and the SPI interface supports speeds up to 24MHz.

User configurable internal pull-up/pull-downs are included on I/O interfaces to reduce system costs associated with external pull-ups/pull-downs.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, TDK InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.81 mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000g shock reliability.

1.3 APPLICATIONS

- Game Controllers
- Cameras
- IoT
- Drones
- Non-OIS SmartPhones
- Wearables
- Hearables

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-45605 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with independently programmable full-scale range of ± 15.625 , ± 31.25 , ± 62.5 , ± 125 , ± 250 , ± 500 , ± 1000 , and ± 2000 degrees/sec for UI and auxiliary paths
- Low Noise (LN) and Low Power (LP) power modes support
- Digitally-programmable low-pass filters
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-45605 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with independently programmable full-scale range of $\pm 2g$, $\pm 4g$, $\pm 8g$ and $\pm 16g$ for UI and auxiliary paths
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 MOTION FEATURES

ICM-45605 includes the following motion features, also known as APEX (**A**dvanced **P**edometer and **E**vent Detection – neXt gen)

- Pedometer: Tracks Step Count, also issues Step Detect interrupt.
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35° for more than a programmable time.
- Raise to Wake/Sleep: Gesture detection for wake and sleep events. Interrupt is issued when either of these two events are detected.
- Single Tap / Double Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Significant Motion Detection: Detects significant motion based on accelerometer data.
- Low-G Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-G Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.

2.4 ADDITIONAL FEATURES

ICM-45605 includes the following additional features:

- Up to 8Kbytes FIFO buffer enables the applications processor to read the data in bursts, default FIFO size is 2Kbytes, user can extend it up to 8kByte by disabling APEX functions
- EDMP Enhanced Digital Motion Processor for implementing motion algorithms
- 20-bits data format support in FIFO for high-data resolution
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- Main interface: 12.5MHz I3CSM (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode) / 1 MHz I²C / 24 MHz SPI slave host interface
- Auxiliary interface: 400 kHz I²C master
- User configurable internal pull-up/pull-downs included on I/O interfaces to reduce system costs associated with external pull-ups/pull-downs
- User configurable Output Data Rate (ODR) and FIFO Data Rate (FDR)
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.81 mm (14-pin LGA)
- 20,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|---|--------|---------|------|-----------|-------|
| GYROSCOPE SENSITIVITY | | | | | | |
| Full-Scale Range | GYRO_UI_FS_SEL =1 | | ±2000 | | °/s | 3 |
| | GYRO_UI_FS_SEL =2 | | ±1000 | | °/s | 3 |
| | GYRO_UI_FS_SEL =3 | | ±500 | | °/s | 3 |
| | GYRO_UI_FS_SEL =4 | | ±250 | | °/s | 3 |
| | GYRO_UI_FS_SEL =5 | | ±125 | | °/s | 3 |
| | GYRO_UI_FS_SEL =6 | | ±62.5 | | °/s | 3 |
| | GYRO_UI_FS_SEL =7 | | ±31.25 | | °/s | 3 |
| | GYRO_UI_FS_SEL =8 | | ±15.625 | | °/s | 3 |
| Gyroscope ADC Word Length | Output in two's complement format | | 16 | | bits | 3, 6 |
| Sensitivity Scale Factor | GYRO_UI_FS_SEL =1 | | 16.4 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =2 | | 32.8 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =3 | | 65.5 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =4 | | 131 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =5 | | 262 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =6 | | 524.3 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =7 | | 1048.6 | | LSB/(°/s) | 3 |
| | GYRO_UI_FS_SEL =8 | | 2097.2 | | LSB/(°/s) | 3 |
| Sensitivity Scale Factor Initial Tolerance | Component-level, 25°C | | ±0.5 | | % | 2 |
| Sensitivity Change vs. Temperature | -40°C to +85°C, board-level | | ±0.01 | | %/°C | 1, 8 |
| Nonlinearity | Best fit straight line; board-level, 25°C | | ±0.1 | | % | 1, 8 |
| Cross-Axis Sensitivity | Board-level | | ±1 | | % | 1, 8 |
| ZERO-RATE OUTPUT (ZRO) | | | | | | |
| Initial ZRO Tolerance | Component-level, 25°C | | ±0.5 | | °/s | 2 |
| ZRO Change vs. Temperature | -40°C to +85°C, board-level | | ±0.015 | | °/s/°C | 1, 8 |
| OTHER PARAMETERS | | | | | | |
| Rate Noise Spectral Density | @ 10 Hz, 25°C | | 0.0038 | | °/s /√Hz | 2, 4 |
| Total RMS Noise | Bandwidth = 100 Hz | | 0.038 | | °/s-rms | 4, 5 |
| Gyroscope Mechanical Frequencies | | | 29.7 | | kHz | 2 |
| Gyroscope Start-Up Time | Time from gyro enable to gyro drive ready | | 35 | 45 | ms | 1, 7 |
| Output Data Rate | Low Noise Mode (LNM) | 12.5 | | 6400 | Hz | 3 |
| | Low Power Mode (LPM) | 1.5625 | | 400 | Hz | 3 |

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not tested in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.
5. Calculated from Rate Noise Spectral Density.
6. 20-bits data format supported in FIFO, see section 6.
7. Measurement conditions: Gyroscope ODR = 6400Hz; Register field GYRO_UI_LPFBW_SEL set to 000 (low pass filter bypassed).
8. Board-level specs performance depends on specific board design of TDK-InvenSense test boards and may not be directly reproducible with other board designs.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|--|--------|--------|------|--------|-------|
| ACCELEROMETER SENSITIVITY | | | | | | |
| Full-Scale Range | ACCEL_UI_FS_SEL = 1 | | ±16 | | g | 3 |
| | ACCEL_UI_FS_SEL = 2 | | ±8 | | g | 3 |
| | ACCEL_UI_FS_SEL = 3 | | ±4 | | g | 3 |
| | ACCEL_UI_FS_SEL = 4 | | ±2 | | g | 3 |
| ADC Word Length | Output in two's complement format | | 16 | | bits | 3, 6 |
| Sensitivity Scale Factor | ACCEL_UI_FS_SEL = 1 | | 2,048 | | LSB/g | 3 |
| | ACCEL_UI_FS_SEL = 2 | | 4,096 | | LSB/g | 3 |
| | ACCEL_UI_FS_SEL = 3 | | 8,192 | | LSB/g | 3 |
| | ACCEL_UI_FS_SEL = 4 | | 16,384 | | LSB/g | 3 |
| Sensitivity Scale Factor Initial Tolerance | Component-level, 25°C | | ±0.5 | | % | 2 |
| Sensitivity Change vs. Temperature | -40°C to +85°C, board-level | | ±0.01 | | %/°C | 1, 8 |
| Nonlinearity | Best fit straight line, ±2g; board-level, 25°C | | ±0.1 | | % | 1, 8 |
| Cross-Axis Sensitivity | Board-level | | ±1 | | % | 1, 8 |
| ZERO-G OUTPUT | | | | | | |
| Initial Tolerance | Component-level, 25°C | | ±15 | | mg | 2 |
| Zero-G Level Change vs. Temperature | -40°C to +85°C, board-level | | ±0.15 | | mg/°C | 1, 8 |
| OTHER PARAMETERS | | | | | | |
| Noise Spectral Density | @ 10 Hz; Up to ±8g FSR | | 70 | | μg/√Hz | 2, 4 |
| | @ 10 Hz; ±16g FSR | | 80 | | μg/√Hz | 2, 4 |
| RMS Noise | Bandwidth = 100 Hz; Up to ±8g FSR | | 0.7 | | mg-rms | 4, 5 |
| | Bandwidth = 100 Hz; ±16g FSR | | 0.8 | | mg-rms | 4, 5 |
| Accelerometer Startup Time | From sleep mode to valid data | | 10 | | ms | 1, 7 |
| Output Data Rate | Low Noise Mode (LNM) | 12.5 | | 6400 | 12.5 | 3 |
| | Low Power Mode (LPM) | 1.5625 | | 400 | 1.5625 | 3 |

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not tested in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.
5. Calculated from Rate Noise Spectral Density.
6. 20-bits data format supported in FIFO, see section 6.
7. Measurement conditions: Gyroscope ODR = 6400Hz; Register field GYRO_UI_LPFBW_SEL set to 000 (low pass filter bypassed).
8. Board-level specs performance depends on specific board design of TDK-InvenSense test boards and may not be directly reproducible with other board designs.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-----------------------------|--|-------|-----|-----|-------|-------|
| SUPPLY VOLTAGES | | | | | | |
| VDD | | 1.71 | 1.8 | 3.6 | V | 1 |
| VDDIO | | 1.08* | 1.8 | 3.6 | V | 1 |
| SUPPLY CURRENTS | | | | | | |
| Low-Noise Mode | 6-Axis Gyroscope + Accelerometer (1600Hz ODR) | | 420 | | μA | 2 |
| | 6-Axis Gyroscope + Accelerometer (6400Hz ODR) | | 440 | | μA | 2 |
| | 3-Axis Accelerometer (1600Hz ODR) | | 120 | | μA | 2 |
| | 3-Axis Accelerometer (6400Hz ODR) | | 130 | | μA | 2 |
| | 3-Axis Gyroscope (1600Hz ODR) | | 360 | | μA | 2 |
| | 3-Axis Gyroscope (6400Hz ODR) | | 370 | | μA | 2 |
| Low-Power Mode | 6-Axis Gyroscope + Accelerometer (50Hz ODR; Gyro 10x AVG; Accel 4x AVG) | | 220 | | μA | 2 |
| | 6-Axis Gyroscope + Accelerometer (200Hz ODR; Gyro 10x AVG; Accel 4x AVG) | | 325 | | μA | 2 |
| | 3-Axis Accelerometer (50Hz ODR; 4x AVG) | | 67 | | μA | 2 |
| | 3-Axis Gyroscope (50Hz ODR; 10x AVG) | | 210 | | μA | 2 |
| Ultra Low-Power Mode | 3-Axis Accelerometer (50Hz ODR; 1x AVG) | | 15 | | μA | 2 |
| Full-Chip Sleep Mode | At 25°C | | 2.2 | | μA | 2 |
| TEMPERATURE RANGE | | | | | | |
| Specified Temperature Range | Performance parameters are not applicable beyond Specified Temperature Range | -40 | | +85 | °C | 1 |

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

* Important Note: When using I3CSM interface the minimum VDDIO value is 1.1V.

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|--|----------------------|--------------------|--------------|--------------|-------|
| SUPPLIES | | | | | | |
| Supply Ramp Time | Valid power-on RESET Monotonic ramp. Ramp rate is 10% to 90% of the final value | 0.01 | | 1 | ms | 1 |
| Power Supply Noise | V _{DD} =1.8V or 3.6V, up to 1MHz | | 10 | 50 | mV peak-peak | 1 |
| TEMPERATURE SENSOR | | | | | | |
| Operating Range | Ambient | -40 | | 85 | °C | 1 |
| 25°C Output | Output in two's complement format | | 0 | | LSB | 3 |
| ADC Resolution | | | 16 | | bits | 2 |
| ODR | With Filter | 1.5625 | | 3200 | Hz | 2, 4 |
| Room Temperature Offset | 25°C | -5 | | 5 | °C | 3 |
| Stabilization Time (fixed number of clock cycles) | | | | 0.014 | sec | 2 |
| Sensitivity | Trimmed | | 128 | | LSB/°C | 1 |
| Sensitivity for FIFO data | Trimmed | | 2 | | LSB/°C | 1 |
| POWER-ON RESET | | | | | | |
| Start-up time for register read/write | From power-up | | | 1 | ms | 1 |
| I²C ADDRESS | | | | | | |
| I ² C ADDRESS | AP_AD0 = 0 AP_AD0 = 1 | | 1101000 1101001 | | | |
| DIGITAL INPUTS (FSYNC, SCLK, SDI, CS) | | | | | | |
| V _{IH} , High Level Input Voltage | | 0.7*VDDIO | | VDDIO + 0.5V | V | 1 |
| V _{IL} , Low Level Input Voltage | | -0.5V | | 0.3*VDDIO | V | |
| C _i , Input Capacitance | | | <10 | | pF | |
| DIGITAL OUTPUT (SDO, INT1, INT2) | | | | | | |
| V _{OH} , High Level Output Voltage | R _{LOAD} =1 MΩ; | 0.9*VDDIO | | | V | 1 |
| V _{OL} , LOW-Level Output Voltage | R _{LOAD} =1 MΩ; | | | 0.1*VDDIO | V | |
| V _{OLINT} , INT Low-Level Output Voltage | OPEN=1, 0.3 mA sink Current | | | 0.1 | V | |
| Output Leakage Current | OPEN=1 | | 100 | | nA | |
| t _{INT} , INT Pulse Width | int0_tpulse_duration= 0, 1 (100μs, 8μs) int1_tpulse_duration= 0, 1 (100μs, 8μs) | | 100 or 8 | 100 | μs | |
| I²C I/O (SCL, SDA) | | | | | | |
| V _{IL} , LOW-Level Input Voltage | | -0.5V | | 0.3*VDDIO | V | 1 |
| V _{IH} , HIGH-Level Input Voltage | | 0.7*VDDIO | | VDDIO + 0.5V | V | |
| V _{hys} , Hysteresis | | | 0.1*VDDIO | | V | |
| V _{OL} , LOW-Level Output Voltage | 3 mA sink current | 0 | | 0.4 | V | |
| I _{OL} , LOW-Level Output Current | V _{OL} =0.4 V V _{OL} =0.6 V | | 3 6 | | mA mA | |
| Output Leakage Current | | | 100 | | nA | |
| t _{of} , Output Fall Time from V _{IHmax} to V _{ILmax} | C _b bus capacitance in pf | 20+0.1C _b | | 300 | ns | |
| INTERNAL CLOCK SOURCE | | | | | | |
| Clock Frequency Initial Tolerance | Gyro inactive; 25°C | -1.25 | | +1.25 | % | 1 |
| | Gyro active; 25°C | -1.25 | | +1.25 | % | 1 |
| Frequency Variation over Temperature | Gyro inactive; -40°C to +85°C | | | ±3 | % | 1 |
| | Gyro active; -40°C to +85°C | | | ±1 | % | 1 |

Table 4. A.C. Electrical Characteristics

Notes:

1. Based on design. Not tested in production.
2. Guaranteed by design.
3. Production tested.
4. Temperature sensor ODR is the higher value between gyroscope and accelerometer ODR.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| Parameters | Conditions | Min | Typical | Max | Units | Notes |
|---|---|--------------------------------------|-----------------------|------|-------|-------|
| I²C TIMING (Host Interface) | | I²C FAST-MODE PLUS | | | | |
| f _{SCL} , SCL Clock Frequency | | | | 1 | MHz | 1 |
| t _{HD,STA} , (Repeated) START Condition Hold Time | | 0.26 | | | μs | 1 |
| t _{LOW} , SCL Low Period | | 0.50 | | | μs | 1 |
| t _{HIGH} , SCL High Period | | 0.26 | | | μs | 1 |
| t _{SU,STA} , Repeated START Condition Setup Time | | 0.26 | | | μs | 1 |
| t _{HD,DAT} , SDA Data Hold Time | | 0 | | | μs | 1 |
| t _{SU,DAT} , SDA Data Setup Time | | 50 | | | ns | 1 |
| t _r , SDA and SCL Rise Time | C _b bus cap. from 30 to 130 pF | | | 120 | ns | 1, 2 |
| t _f , SDA and SCL Fall Time | C _b bus cap. from 30 to 130 pF | | 20 x (VDD / 5.5 V) | 120 | ns | 1, 2 |
| t _{SU,STO} , STOP Condition Setup Time | | 0.26 | | | μs | 1 |
| t _{BUF} , Bus Free Time Between STOP and START Condition | | 0.50 | | | μs | 1 |
| C _b , Capacitive Load for each Bus Line | | 30 | | 130 | pF | 1 |
| t _{VD,DAT} , Data Valid Time | | | | 0.45 | μs | 1 |
| t _{VD,ACK} , Data Valid Acknowledge Time | | | | 0.45 | μs | 1 |

Table 5. I²C Host Interface Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.
2. Transition times are defined between thresholds: 0.3*VDDIO, 0.7*VDDIO.

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| Parameters | Conditions | Min | Typical | Max | Units | Notes |
|---|---|---------------------------------|-----------------------|------|-------|-------|
| I²C TIMING (Master Interface) | | I²C FAST-MODE | | | | |
| f _{SCL} , SCL Clock Frequency | | | | 400 | kHz | 1 |
| t _{HD,STA} , (Repeated) START Condition Hold Time | | 0.60 | | | μs | 1 |
| t _{LOW} , SCL Low Period | | 1.30 | | | μs | 1 |
| t _{HIGH} , SCL High Period | | 0.60 | | | μs | 1 |
| t _{SU,STA} , Repeated START Condition Setup Time | | 0.60 | | | μs | 1 |
| t _{HD,DAT} , SDA Data Hold Time | | 0 | | | μs | 1 |
| t _{SU,DAT} , SDA Data Setup Time | | 100 | | | ns | 1 |
| t _r , SDA and SCL Rise Time | C _b bus cap. from 30 to 200 pF | 20 | | 300 | ns | 1, 2 |
| t _f , SDA and SCL Fall Time | C _b bus cap. from 30 to 200 pF | | 20 x (VDD / 5.5 V) | 300 | ns | 1, 2 |
| t _{SU,STO} , STOP Condition Setup Time | | | | 0.60 | μs | 1 |
| t _{BUF} , Bus Free Time Between STOP and START Condition | | 1.30 | | | μs | 1 |
| C _b , Capacitive Load for each Bus Line | | 30 | | 200 | pF | 1 |
| t _{VD,DAT} , Data Valid Time | | | | 0.90 | μs | 1 |
| t _{VD,ACK} , Data Valid Acknowledge Time | | | | 0.90 | μs | 1 |

Table 6. I²C Master Interface Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.
2. Transition times are defined between thresholds: 0.3*VDDIO, 0.7*VDDIO.

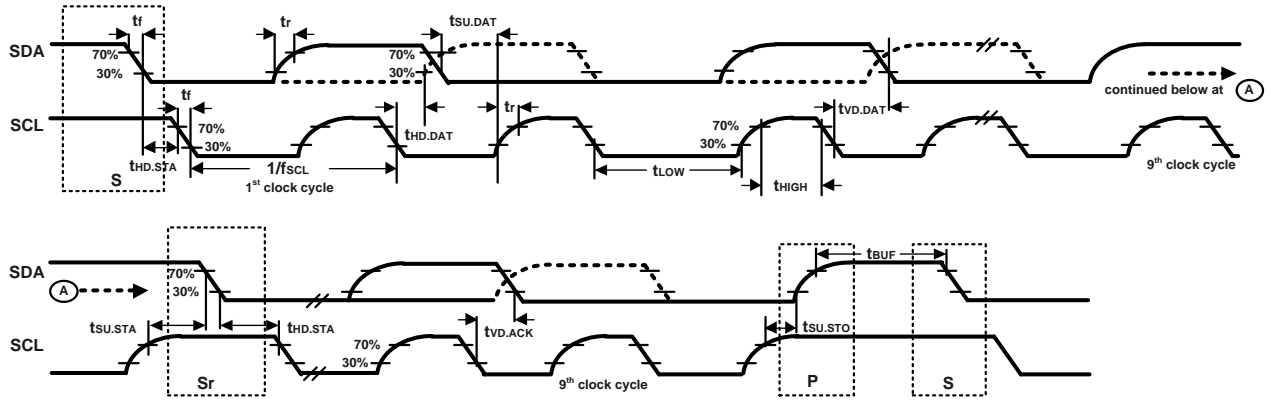


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

| PARAMETERS | CONDITIONS | VDDIO < 1.71V | | VDDIO ≥ 1.71V | | UNITS | NOTES |
|--|---------------------------|---------------|------|---------------|------|-------|-------|
| | | MIN | MAX | MIN | MAX | | |
| SPI TIMING | | | | | | | |
| f _{SPC} , SCLK Clock Frequency | Default | | 20 | | 24 | MHz | 1 |
| t _{LOW} , SCLK Low Period | | 23.5 | | 17 | | ns | 1 |
| t _{HIGH} , SCLK High Period | | 22.5 | | 17 | | ns | 1 |
| t _{SU,CS} , CS Setup Time | | 17 | | 17 | | ns | 1 |
| t _{HD,CS} , CS Hold Time | | 5 | | 5 | | ns | 1 |
| t _{SU,SDI} , SDI Setup Time | | 13 | | 13 | | ns | 1 |
| t _{HD,SDI} , SDI Hold Time | | 8 | | 8 | | ns | 1 |
| t _{VD,SDO} , SDO Valid Time | C _{load} = 20 pF | | 18.5 | | 18.5 | ns | 1 |
| t _{HD,SDO} , SDO Hold Time | C _{load} = 20 pF | 3.5 | | 3.5 | | ns | 1 |
| t _{DIS,SDO} , SDO Output Disable Time | | | 28 | | 28 | ns | 1 |

Table 7. 4-Wire SPI Timing Characteristics

Notes:

- Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

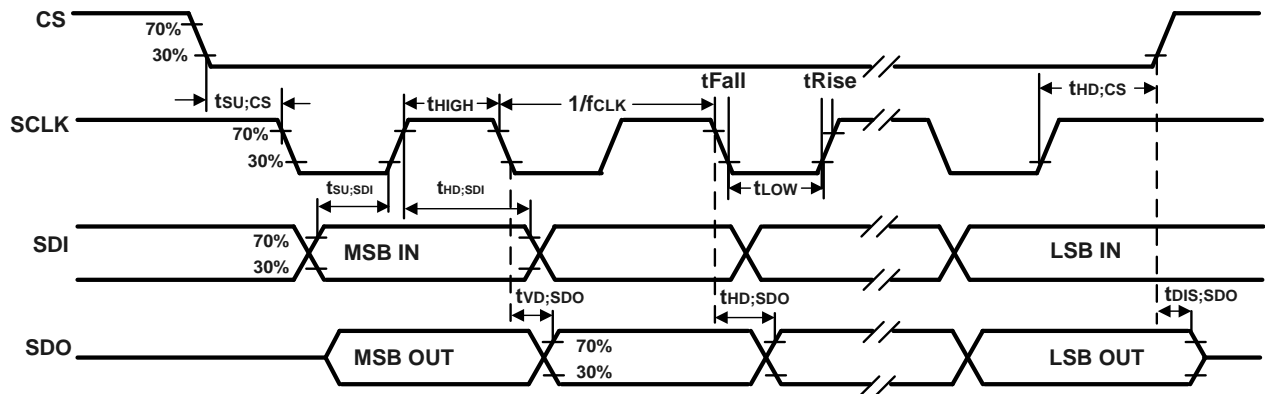


Figure 2. 4-Wire SPI Bus Timing Diagram

3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, TA=25°C, unless otherwise noted.

| PARAMETERS | CONDITIONS | VDDIO < 1.71V | | VDDIO ≥ 1.71V | | UNITS | NOTES |
|--|---------------------------|---------------|------|---------------|------|-------|-------|
| | | MIN | MAX | MIN | MAX | | |
| SPI TIMING | | | | | | | |
| f _{SPC} , SCLK Clock Frequency | Default | | 20 | | 24 | MHz | 1 |
| t _{LOW} , SCLK Low Period | | 23.5 | | 17 | | ns | 1 |
| t _{HIGH} , SCLK High Period | | 22.5 | | 17 | | ns | 1 |
| t _{SU,CS} , CS Setup Time | | 17 | | 17 | | ns | 1 |
| t _{HD,CS} , CS Hold Time | | 5 | | 5 | | ns | 1 |
| t _{SU,SDIO} , SDIO Input Setup Time | | 13 | | 13 | | ns | 1 |
| t _{HD,SDIO} , SDIO Input Hold Time | | 8 | | 8 | | ns | 1 |
| t _{VD,SDIO} , SDIO Output Valid Time | C _{load} = 20 pF | | 18.5 | | 18.5 | ns | 1 |
| t _{HD,SDIO} , SDIO Output Hold Time | C _{load} = 20 pF | 3.5 | | 3.5 | | ns | 1 |
| t _{DIS,SDIO} , SDIO Output Disable Time | | | 28 | | 28 | ns | 1 |

Table 8. 3-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

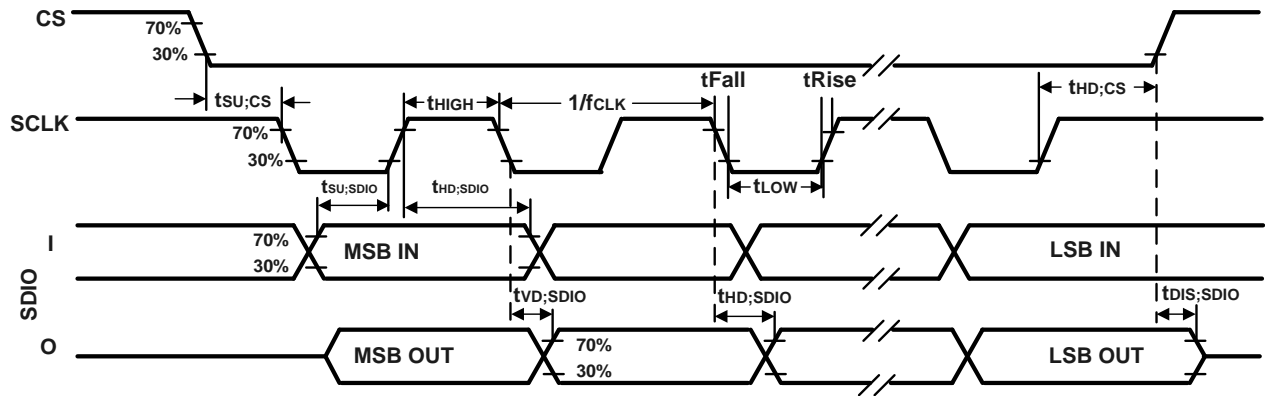


Figure 3. 3-Wire SPI Bus Timing Diagram

3.7 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

| Parameter | Rating |
|--|--|
| Supply Voltage, VDD | -0.5 V to +4 V |
| Supply Voltage, VDDIO | -0.5 V to +4 V |
| Input Voltage Level (FSYNC, SCL, SDA) | -0.5 V to VDDIO + 0.5 V |
| Acceleration (Any Axis, unpowered) | 20,000g for 0.2 ms |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -40°C to +125°C |
| Electrostatic Discharge (ESD) Protection | 2 kV (HBM); 500 V (CDM) |
| Latch-up | JEDEC Class II (2) for VDDIO ≤ 1.98V, JEDEC Class I (1) for VDDIO > 1.98V, ±100 mA |

Table 9. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

| Pin Number | Pin Name | Single Interface Mode | Dual Interface I ² C Master Mode | Notes |
|------------|-----------------|--|--|---|
| 1 | AP_SDO / AP_ADO | AP_SDO: AP SPI serial data output (4-wire mode); AP_ADO: AP I ³ C SM / I ² C slave address LSB | AP_SDO: AP SPI serial data output (4-wire mode); AP_ADO: AP I ³ C SM / I ² C slave address LSB | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_sdo_pe_trim_d2a[0] and pads_ap_sdo_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_ap_sdo_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_sdo_pud_trim_d2a[0] = 0 (1).</p> <p>If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_sdo_pe_trim_d2a[0] = 0.</p> |
| 2 | RESV / MAS_DA | RESV: No Connect or Connect to VDDIO or Connect to GND | MAS_DA: I ² C serial master data | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_aux1_sdi_pe_trim_d2a[0] and pads_aux1_sdi_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_sdi_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_sdi_pud_trim_d2a[0] = 0 (1).</p> <p>If the AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_sdi_pe_trim_d2a[0] = 0.</p> <p>If pin2 is no connect, leave pads_aux1_sdi_pe_trim_d2a[0] = 1. If pin2 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_sdi_pe_trim_d2a[0] = 0.</p> |
| 3 | RESV / MAS_CLK | RESV: No Connect or Connect to VDDIO or Connect to GND | MAS_CLK: I ² C serial master clock | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_aux1_sclk_pe_trim_d2a[0] and pads_aux1_sclk_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_sclk_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_sclk_pud_trim_d2a[0] = 0 (1).</p> <p>If the AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_sclk_pe_trim_d2a[0] = 0.</p> <p>If pin3 is no connect, leave pads_aux1_sclk_pe_trim_d2a[0] = 1. If pin3 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_sclk_pe_trim_d2a[0] = 0.</p> |
| 4 | INT1 / INT | INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain); INT: All | INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain); INT: All interrupts mapped to pin 4 | <p>By default, internal pull-up is disabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal</p> |

| | | | | |
|----|--------------|--|--|--|
| | | interrupts mapped to pin 4 | | pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_int1_pe_trim_d2a[0] and pads_int1_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_int1_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_int1_pud_trim_d2a[0] = 0 (1). |
| 5 | VDDIO | VDDIO: IO power supply voltage | VDDIO: IO power supply voltage | |
| 6 | GND | GND: Power supply ground | GND: Power supply ground | |
| 7 | RESV | RESV: No Connect or Connect to VDDIO or Connect to GND | RESV: No Connect or Connect to VDDIO or Connect to GND | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_pin7_pe_trim_d2a[0] and pads_pin7_cs_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_pin7_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_pin7_cs_pud_trim_d2a[0] = 0 (1).</p> <p>If pin7 is no connect, leave pads_pin7_pe_trim_d2a[0] = 1. If pin7 is connected to VDDIO or GND, disable internal pull-up by setting pads_pin7_pe_trim_d2a[0] = 0.</p> |
| 8 | VDD | VDD: Power supply voltage | VDD: Power supply voltage | |
| 9 | INT2 / FSYNC | INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain); FSYNC: Frame sync input; If pin not used, can be No Connect or Connect to VDDIO | INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain); FSYNC: Frame sync input; If pin not used, can be No Connect or Connect to VDDIO | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_int2_pe_trim_d2a[0] and pads_int2_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_int2_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_int2_pud_trim_d2a[0] = 0 (1).</p> <p>If pin9 is no connect, leave pads_int2_pe_trim_d2a[0] = 1. If pin9 is connected as an I/O, disable internal pull-up by setting pads_int2_pe_trim_d2a[0] = 0.</p> |
| 10 | RESV | RESV: No Connect or Connect to VDDIO or Connect to GND | RESV: No Connect or Connect to VDDIO or Connect to GND | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_aux1_cs_pe_trim_d2a[0] and pads_aux1_cs_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_cs_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_cs_pud_trim_d2a[0] = 0 (1).</p> <p>If the AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_cs_pe_trim_d2a[0] = 0. If pin10 is no connect, leave pads_aux1_cs_pe_trim_d2a[0] = 1. If pin10 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_cs_pe_trim_d2a[0] = 0.</p> |
| 11 | RESV | RESV: No Connect or Connect to VDDIO or Connect to GND | RESV: No Connect or Connect to VDDIO or Connect to GND | By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers |

| | | | | |
|----|---------------------------|--|--|--|
| | | | | <p>pads_aux1_sdo_pe_trim_d2a[0] and pads_aux1_sdo_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_sdo_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_sdo_pud_trim_d2a[0] = 0 (1).</p> <p>If AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_sdo_pe_trim_d2a[0] = 0. If pin11 is no connect, leave pads_aux1_sdo_pe_trim_d2a[0] = 1. If pin11 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_sdo_pe_trim_d2a[0] = 0.</p> |
| 12 | AP_CS | AP_CS: AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C SM / I ² C interface | AP_CS: AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C SM / I ² C interface | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_cs_pe_trim_d2a[0] and pads_ap_cs_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_ap_cs_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_cs_pud_trim_d2a[0] = 0 (1).</p> <p>If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_cs_pe_trim_d2a[0] = 0.</p> |
| 13 | AP_SCL / AP_SCLK | AP_SCL: AP I3C SM / I ² C serial clock; AP_SCLK: AP SPI serial clock | AP_SCL: AP I3C SM / I ² C serial clock; AP_SCLK: AP SPI serial clock | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_sclk_pe_trim_d2a[0] and pads_ap_sclk_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_ap_sclk_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_sclk_pud_trim_d2a[0] = 0 (1).</p> <p>If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_sclk_pe_trim_d2a[0] = 0.</p> |
| 14 | AP_SDA / AP_SDIO / AP_SDI | AP_SDA: AP I3C SM / I ² C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode) | AP_SDA: AP I3C SM / I ² C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode) | <p>By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_sdi_pe_trim_d2a[0] and pads_ap_sdi_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_ap_sdi_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_sdi_pud_trim_d2a[0] = 0 (1).</p> <p>If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_sdi_pe_trim_d2a[0] = 0.</p> |

Table 10. Signal Descriptions

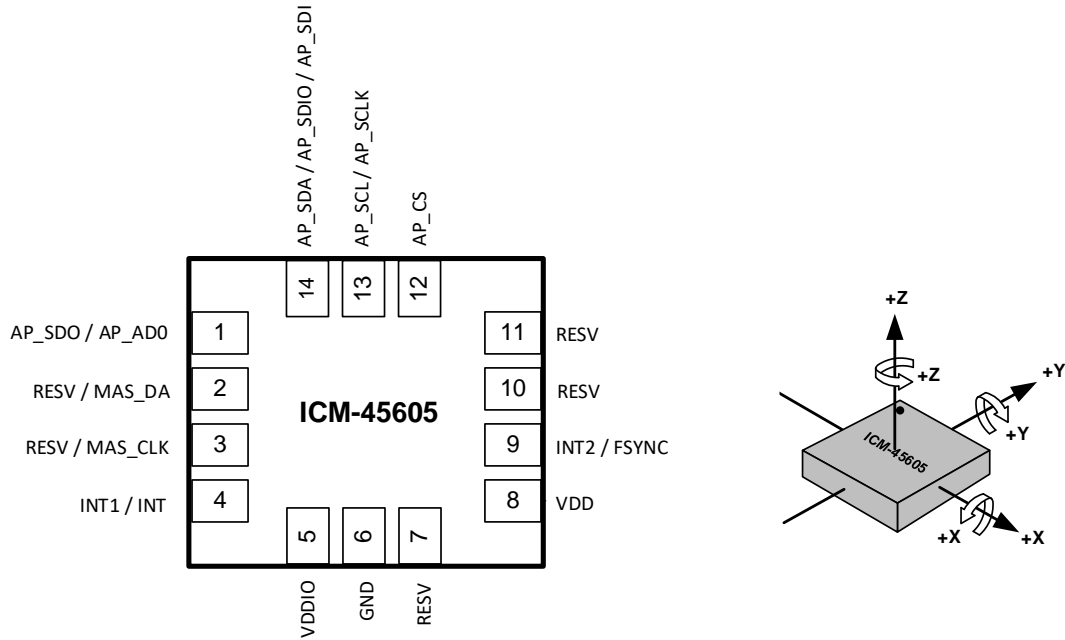
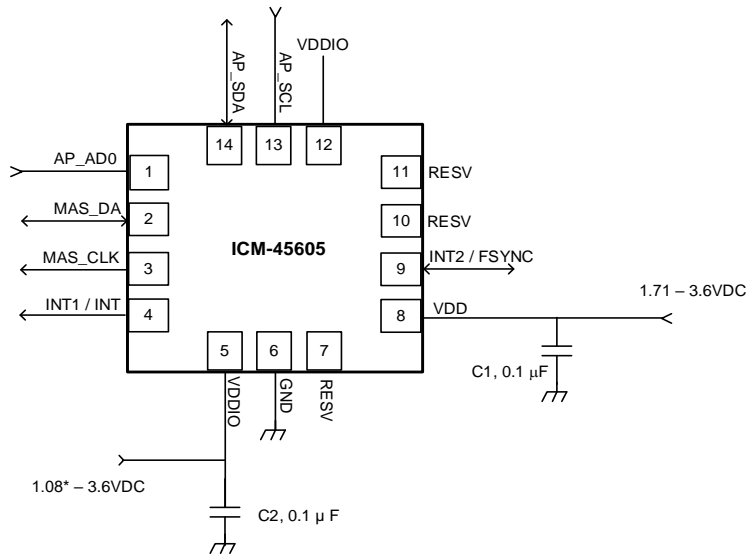


Figure 4. Pin Out Diagram for ICM-45605 2.5x3.0x0.81 mm LGA

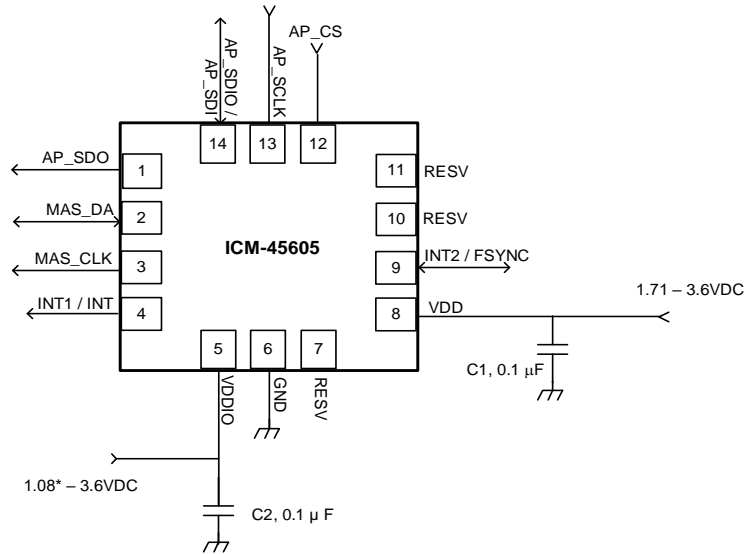
4.2 TYPICAL OPERATING CIRCUIT (DUAL INTERFACE I²C MASTER MODE)



* Important Note: When using I3CSM interface the minimum VDDIO value is 1.1V.

Figure 5. ICM-45605 Application Schematic Dual Interface I²C Master Mode (I3CSM / I²C Interface to Host)

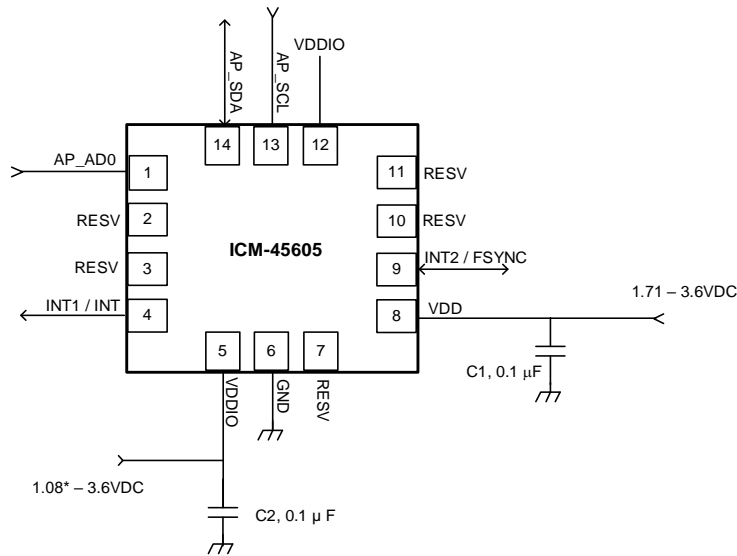
Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.



* Important Note: When using I3CSM interface the minimum VDDIO value is 1.1V.

Figure 6. ICM-45605 Application Schematic Dual Interface I²C Master Mode (SPI Interface to Host)

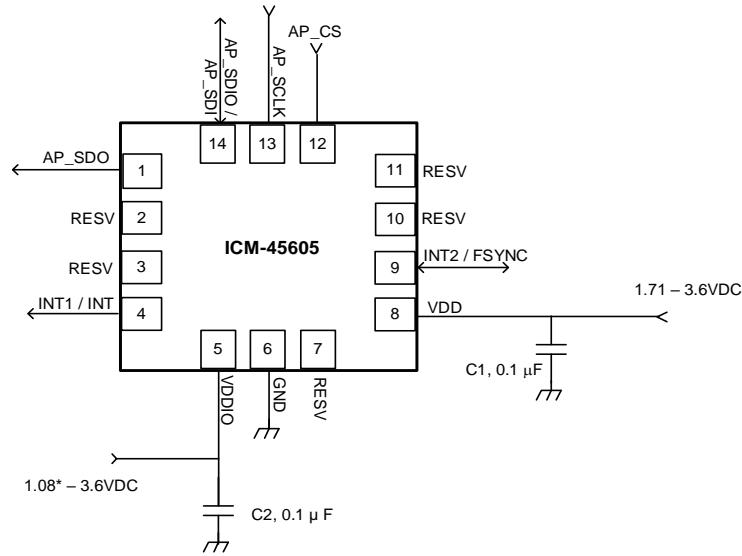
4.3 TYPICAL OPERATING CIRCUIT (SINGLE INTERFACE MODE)



* Important Note: When using I3CSM interface the minimum VDDIO value is 1.1V.

Figure 7. ICM-45605 Application Schematic Single Interface Mode (I3CSM / I²C Interface to Host)

Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.



* Important Note: When using I3CSM interface the minimum VDDIO value is 1.1V.

Figure 8. ICM-45605 Application Schematic Single Interface Mode (SPI Interface to Host)

4.4 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

| Component | Label | Specification | Quantity |
|------------------------|-------|-----------------|----------|
| VDD Bypass Capacitor | C1 | X7R, 0.1μF ±10% | 1 |
| VDDIO Bypass Capacitor | C2 | X7R, 0.1μF ±10% | 1 |

Table 11. Bill of Materials

Note: Use larger bypass capacitor than 0.1μF if power supply ripple exceeds 50mV peak-to-peak.

4.5 SYSTEM BLOCK DIAGRAM

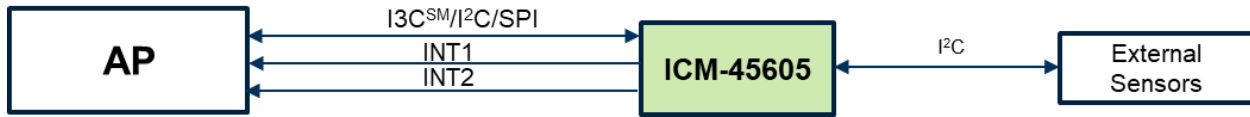


Figure 9. ICM-45605 System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.6 OVERVIEW

The ICM-45605 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
 - 20-bits data format support in FIFO for high-data resolution (see section 5 for details)
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
 - 20-bits data format support in FIFO for high-data resolution (see section 5 for details)
- I3CSM, I²C and SPI Host Interface
- I²C Master Interface for connection to external sensors
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.7 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-45605 includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ± 15.625 , ± 31.25 , ± 62.5 , ± 125 , ± 250 , ± 500 , ± 1000 , and ± 2000 degrees per second (dps).

4.8 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-45605 includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-45605 architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure $0g$ on the X- and Y-axes and $+1g$ on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full-scale range of the digital output can be adjusted to $\pm 2g$, $\pm 4g$, $\pm 8g$, and $\pm 16g$.

4.9 I3CSM, I²C AND SPI HOST INTERFACE

The ICM-45605 communicates to the application processor using an I3CSM, I²C, or SPI serial interface. The ICM-45605 always acts as a slave when communicating to the application processor.

4.10 I²C MASTER INTERFACE FOR CONNECTION TO EXTERNAL SENSORS

The ICM-45605 has an I²C master interface for connection to external sensors.

Up to 2 external sensors can be connected on this interface and their data read into the ICM-45605. I²C speed up to 400kHz is supported on the master interface. After I²C master finishes reading sensor data from the external sensor(s), the received sensor data is then reformatted by the internal processor (eDMP). The reformatted external sensor data is then moved into FIFO along with other internal sensor data. The external host reads the FIFO to retrieve both the external sensor data and the internal sensor data.

- Independent of the number of external devices on the I²C bus, the I²C master automatically executes up to 4 I²C transactions per trigger.
- The 4 I²C transactions are fully independent to each other.
- Each I²C transaction can be targeting any external I²C device (capped at 2 external I²C devices).
- Each I²C transaction can be a read or a write access transaction.
- Each I²C transaction can be a burst or a non-burst access transaction.
- A read transaction can be from an auto-incremented address location, or from a new address location.
- A read operation with a new address location consumes one of the 4 I²C transactions per trigger.

4.11 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.12 CLOCKING

The ICM-45605 has a flexible clocking scheme, allowing internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers.

Allowable internal sources for generating the internal clock are:

- a) An internal relaxation oscillator
- b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

For internal sources, the only setting supporting specified performance in all modes is option b). It is recommended that option b) be used when using internal clock source.

4.13 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read anytime.

4.14 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.15 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-45605 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature sensor register data TEMP_DATA is updated with new data at max (Accelerometer ODR, Gyroscope ODR).

4.16 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-45605.

4.17 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.18 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-45605.

| Name | Gyro | Accel |
|------------------------------------|-------------|-------------|
| Sleep Mode | Off | Off |
| Standby Mode | Drive On | Off |
| Accelerometer Low-Power Mode | Off | Duty-Cycled |
| Accelerometer Ultra Low-Power Mode | Off | Duty-Cycled |
| Gyroscope Low-Power Mode | Duty-Cycled | Off |
| 6-Axis Low-Power Mode | Duty-Cycled | Duty-Cycled |
| Accelerometer Low-Noise Mode | Off | On |
| Gyroscope Low-Noise Mode | On | Off |
| 6-Axis Low-Noise Mode | On | On |

Table 12. Standard Power Modes for ICM-45605

5 SIGNAL PATH

The following figure shows a block diagram of the signal path for ICM-45605.

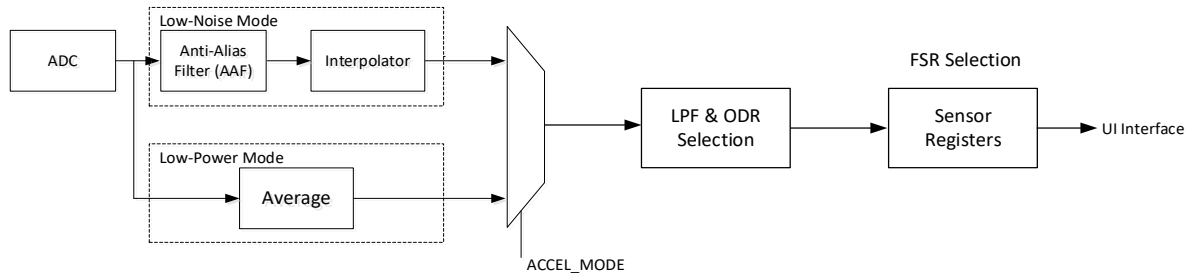


Figure 10. ICM-45605 Signal Path

The signal path starts with ADCs for the gyroscope and accelerometer. Low-Noise Mode and Low-Power Mode options are available for the gyroscope and accelerometer and are selectable using register fields GYRO_MODE and ACCEL_MODE respectively.

In Low-Noise Mode, the ADC output is sent through an Anti-Alias Filter (AAF). The AAF is an FIR filter with fixed coefficients (not user configurable). The AAF can be enabled or disabled by the user using GYRO_SRC_CTRL and ACCEL_SRC_CTRL.

The AAF is followed by an Interpolator. Sensor data can be re-timed using an interpolator when the user applies an external clock for higher ODR accuracy or operates the ICM-45605 in I3CSM synchronous mode. The Interpolator can be enabled or disabled by the user using GYRO_SRC_CTRL and ACCEL_SRC_CTRL.

In Low-Power Mode, the gyroscope and accelerometer ADC outputs are sent through Average filters, with user configurable average filter setting using register fields GYRO_LP_AVG_SEL and ACCEL_LP_AVG_SEL.

The output of Interpolator in Low-Noise Mode, or Average filter in Low-Power Mode is subject to UI LPF and ODR selection. The UI LPF BW is set by register bit field GYRO_UI_LPFBW_SEL and ACCEL_UI_LPFBW_SEL for gyroscope and accelerometer respectively. User selectable ODR is set using register fields GYRO_ODR and ACCEL_ODR. This is followed by Full Scale Range (FSR) selection based on user configurable settings for register fields GYRO_UI_FS_SEL and ACCEL_UI_FS_SEL.

6 FIFO

The ICM-45605 contains up to 8Kbytes FIFO (default FIFO size is 2Kbytes, user can extend it up to 8Kbytes by disabling APEX functions) that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO.

ICM-45605 includes FIFO Compression algorithm that allows storing compressed sensor data in FIFO frames, thus virtually providing more FIFO space. It allows to store up to 4 times the number of frames with respect to non-compressed data. Frame decompression must be performed on the Host which reads the FIFO. Compression algorithm uses a hardware lossless algorithm, based on data variation analysis of each axis. Compression ratios x2, x3, x4 are supported, providing up to 32kByte data storage capability.

A 20-bit data format support is included in one of the FIFO packets structures. When the 20-bit data format is used, the gyroscope data consists of 20-bit of actual data, the accelerometer data consists of 19-bit of actual data and the LSB is always set to 0. Irrespective of the user-full scale selection, this high-resolution 20-bit data format is always scaled to ± 4000 dps (131.1 LSB/dps) for gyroscope and ± 32 g (16384 LSB/g) for accelerometer.

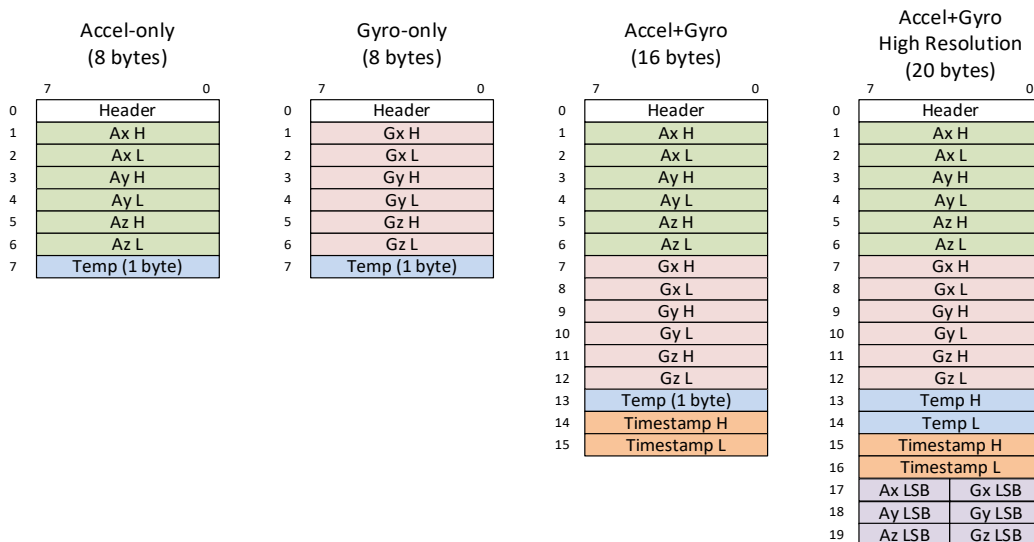
FIFO packet decimation capability is provided for additional storage optimization. User can configure the FIFO Data Rate (FDR) to control the decimation rate for writing packets to the FIFO. User must disable sensors when initializing FDR control value or making changes to it.

6.1 PACKET STRUCTURE

FIFO packets are assembled in different packet sizes based on the enabled sensors. When internal sensors Accel and Gyro are enabled, the following packets are available:

- 8 bytes packet: Contains Accel-only or Gyro-only data and Temperature data (1 byte)
- 16 bytes packet: Contains Accel data, Gyro data, Temperature data (1 byte), Timestamp
- 20 bytes packet: Contains high-resolution Accel data, Gyro data, Temperature data (2 bytes), Timestamp

The following figure shows packets organization for each format (big endian mode).



When external sensors ESO and ES1 are enabled, the following packets are available:

- 16 bytes packet: Contains 6/9 bytes ESO-only or ES1-only data
- 20 bytes frame: Contains 6/9 bytes ESO data and ES1 data
- 32 bytes frame: Contains Accel data, Gyro data, 6/9 bytes ESO data, ES1 data, Temperature data (1 byte), Timestamp. The 32 bytes format is always selected when at least one internal sensor and one external sensor are enabled

The following figure shows packets organization for each format (big endian mode).



6.2 FIFO HEADER

The following table shows the structure of the first byte of the FIFO header.

| Bit Field | Item | Description |
|-----------|---------------|---|
| 7 | EXT_HEADER | 1: FIFO header length is extended to 2 bytes. The second byte is used for compressed frame decoding fields or external sensors information 0: FIFO header length is 1 byte |
| 6 | ACCEL_EN | 1: Accel is enabled or high resolution is enabled 0: Accel is not enabled and high resolution is not enabled |
| 5 | GYRO_EN | 1: Gyro is enabled or high resolution is enabled 0: Gyro is not enabled and high resolution is not enabled |
| 4 | HIRES_EN | 1: High-resolution is enabled (20-bytes format) 0: High-resolution is not enabled |
| 3 | TMST_FIELD_EN | 1: Timestamp field is included in the packet. This requires that: a) high-resolution is enabled, or b) both Accel and Gyro are enabled, or c) either Accel or Gyro are enabled, and either ESO or ES1 are enabled The timestamp field contains the timestamp value or FSYNC-ODR delay depending on configuration 0: Timestamp field is not included in the packet |
| 2 | FSYNC_TAG_EN | 1: FSYNC is triggered and the Timestamp field contains the FSYNC-ODR delay 0: FSYNC is not triggered and the Timestamp field does not contain the FSYNC-ODR delay |

| | | |
|---|-----------|--|
| 1 | ACCEL_ODR | 1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel |
| 0 | GYRO_ODR | 1: The ODR for gyro is different for this gyro data packet compared to the previous gyro packet 0: The ODR for gyro is the same as the previous packet with gyro |

When External Sensors are enabled, an additional header byte is used. The second byte of the header is described below.

| Bit Field | Item | Description |
|-----------|-----------|--|
| 7:5 | - | Reserved |
| 4 | ES0_6b_9b | Indicates how many bytes sensor ES0 provides 1: Sensor ES0 provides 9 bytes data 0: Sensor ES0 provides 6 bytes data |
| 3 | ES1_VLD | 1: ES1 data is valid 0: ES1 data is not valid |
| 2 | ES0_VLD | 1: ES0 data is valid 0: ES0 data is not valid |
| 1 | ES1_EN | 1: Sensor ES1 is enabled 0: Sensor ES1 is not enabled |
| 0 | ES0_EN | 1: Sensor ES0 is enabled 0: Sensor ES0 is not enabled |

7 PROGRAMMABLE INTERRUPTS

The ICM-45605 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts:

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, ICM-45605 includes In-band Interrupt (IBI) support for the I3CSM interface.

8 *EDMP*

The on-chip Enhanced Digital Motion Processor (EDMP) is designed for motion processing of next-gen sensor products. It enables ultra-low power run-time and offloads computation of motion processing and sensor fusion algorithms from the host processor. It enables the host system to execute custom algorithms and issue software interrupts to the external environment. The EDMP can be deployed in the system to minimize system level power, simplify the software architecture, and save valuable MIPS on the host processor. The EDMP implements a motion sensor optimized custom ISA with special motion processing instructions.

9 APEX MOTION FUNCTIONS

The APEX (Advanced Pedometer and Event Detection – neXt gen) features of ICM-45605 consist of:

- Pedometer: Tracks Step Count, also issues Step Detect interrupt.
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35° for more than a programmable time.
- Raise to Wake/Sleep: Gesture detection for wake and sleep events. Interrupt is issued when either of these two events are detected.
- Single Tap / Double Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold. This motion event can be used to enable chip operation from sleep mode.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Significant Motion Detection: Detects significant motion based on accelerometer data.
- Low-G Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-G Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.

These functions are run as software on EDMP.

10 DIGITAL INTERFACE

10.1 I3CSM, I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-45605 can be accessed using I3CSM at 12.5 MHz (data rates up to 12.5 Mbps in SDR mode, 25 Mbps in DDR mode), I²C at 1 MHz or SPI at 24 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in section 4.

10.2 I3CSM INTERFACE

I3CSM is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3CSM is intended to improve upon the I²C interface, while preserving backward compatibility. The I3CSM capability of this device is compliant with Version 1.1.1 of the MIPI Alliance Specification for I3CSM. Please refer to the corresponding MIPI I3CSM specification for I3CSM timing information for this device.

I3CSM carries the advantages of I²C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3CSM adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

ICM-45605 supports the following features of I3CSM:

- SDR data rate up to 12.5 Mbps
- DDR data rate up to 25 Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- Support for asynchronous timing control mode 0
- Error detection (CRC and/or Parity)
- Common Command Code (CCC)

The ICM-45605 always operates as an I3CSM slave device when communicating to the system processor, which thus acts as the I3CSM master. I3CSM master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3CSM master.

The following table shows I3CSM Common Command Code (CCC) commands supported by the device.

| CCC Description | | Required or Optional per I3C v1.0 | Supported by ICM-45605 Host Interface |
|-----------------|---|-----------------------------------|---------------------------------------|
| 1 | ENEC, broadcast mode. (Enable Events). | Required | Yes |
| 2 | DISEC, broadcast mode. (Disable Events) | Required | Yes |
| 3 | ENTAS0, broadcast mode. (Enter Activity State 0) | Required | Yes |
| 4 | ENTAS1, broadcast mode. (Enter Activity State 1) | Optional | No |
| 5 | ENTAS2, broadcast mode. (Enter Activity State 0) | Optional | No |
| 6 | ENTAS3, broadcast mode. (Enter Activity State 0) | Optional | No |
| 7 | RSTDAA, broadcast mode. (Reset dynamic address assignment). | Required | Yes |
| 8 | ENTDAA, broadcast mode. (Enter dynamic address assignment). | Required | Yes |

| | | | | |
|----|--|--|----------|-----|
| 9 | DEFSLVS, broadcast mode. (Define list of slaves). | | Optional | No |
| 10 | SETMWL, broadcast mode. (Set Max Write Length). | | Required | Yes |
| 11 | SETMRL, broadcast mode. (Set Max Read Length). | | Required | Yes |
| 12 | ENTTM, broadcast mode. (Enter Test Mode). | | Optional | No |
| 13 | ENTHDR0, broadcast mode. (Enter HDR DDR mode) | | Optional | Yes |
| 14 | ENTHDR1, broadcast mode. (Enter HDR TSP mode) | | Optional | No |
| 15 | ENTHDR2, broadcast mode. (Enter HDR TSL mode) | | Optional | No |
| 16 | SETXTIME, broadcast mode. (Exchange Timing Information). | | | |
| | 16.1 | Defining byte = 0x7F (ST) | Optional | Yes |
| | 16.2 | Defining byte = 0xBF (DT) | Optional | Yes |
| | 16.3 | Defining byte = 0xDF (Enter Async Mode 0) | Optional | Yes |
| | 16.4 | Defining byte = 0xEF (Enter Async Mode 1) | Optional | No |
| | 16.5 | Defining byte = 0xF7 (Enter Async Mode 2) | Optional | No |
| | 16.6 | Defining byte = 0xFB (Enter Async Mode 3) | Optional | No |
| | 16.7 | Defining byte = 0xFD (Async Trigger for Async Mode 3). | Optional | No |
| | 16.8 | Defining byte = 0x3F (TPH) | Optional | Yes |
| | 16.9 | Defining byte = 0x9f (TU) | Optional | Yes |
| | 16.10 | Defining byte = 0x8F (ODR) | Optional | Yes |
| 17 | ENEC, direct mode. (Enable Events). | | Required | Yes |
| 18 | DISEC, direct mode. (Disable Events). | | Required | Yes |
| 19 | ENTAS0, direct mode. (Enter Activity State 0). | | Required | Yes |
| 20 | ENTAS1, direct mode. (Enter Activity State 1). | | Optional | No |
| 21 | ENTAS2, direct mode. (Enter Activity State 2). | | Optional | No |
| 22 | ENTAS3, direct mode. (Enter Activity State 3). | | Optional | No |
| 23 | RSTDAA, direct mode. (Reset dynamic address assignment). | | Required | Yes |
| 24 | SETDASA, direct mode. (Set Dynamic address from static address). | | Optional | Yes |

| | | | |
|----|---|--|-----------------|
| 25 | SETNEWDA, direct mode. (Set new dynamic address) | Required | Yes |
| 26 | SETMWL, direct mode. (Set Max Write Length). | Required / Conditional | Yes |
| 27 | SETMRL, direct mode. (Set Max Read length). | Required / Conditional | Yes |
| 28 | GETMWL, direct mode. (Get Max write length). | Required / Conditional | Yes |
| 29 | GETMRL, direct mode. (Get Max Read length). | Required / Conditional | Yes |
| 30 | GETPID, direct mode. (Get provisional ID). | Required | Yes |
| 31 | GETBCR, direct mode. (Get Bus Characteristics Register). | Required | Yes |
| 32 | GETDCR, direct mode. (Get Device Characteristics Register). | Required | Yes |
| 33 | GETSTATUS, direct mode. (Get Device Status). | Required | Yes |
| 34 | GETACCMST, direct mode. (Get Accept Mastership). | Optional | No |
| 35 | SETBRGTGT, direct mode. (Set Bridge Targets). | Optional | No |
| 36 | GETMXDS, direct mod. (Get Max Data Speed). | Optional | Yes |
| 37 | GETHDCAP, direct mode. (Get HDR capability). | Optional | Yes |
| 38 | SETXTIME, direct mode. (Set Exchange Timing information). | | |
| | 38.1 | Defining byte = 0x7F (ST) | Optional Yes |
| | 38.2 | Defining byte = 0xBF (DT) | Optional Yes |
| | 38.3 | Defining byte = 0xDF (Enter Async Mode 0) | Optional Yes |
| | 38.4 | Defining byte = 0xEF (Enter Async Mode 1) | Optional No |
| | 38.5 | Defining byte = 0xF7 (Enter Async Mode 2) | Optional No |
| | 38.6 | Defining byte = 0xFB (Enter Async Mode 3) | Optional No |
| | 38.7 | Defining byte = 0xFD (Async Trigger for Async Mode 3). | Optional No |
| | 38.8 | Defining byte = 0x3F (TPH) | Optional Yes |
| | 38.9 | Defining byte = 0x9f (TU) | Optional Yes |
| | 38.10 | Defining byte = 0x8F (ODR) | Optional Yes |

| | | | |
|--|--|----------|-----|
| | 39 GETXTIME, direct mode. (Get Exchange Timing Information). | Optional | Yes |
|--|--|----------|-----|

Table 13. I3CSM CCC Commands

10.3 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-45605 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-45605 is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two ICM-45605s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

10.4 I²C MASTER INTERFACE

I²C master is compliant with the I²C standard-Mode (max 100kbps), and I²C Fast-Mode (max 400kbps). It supports 8-bit I²C static address. It does not support multi-master on the I²C bus. Clock-stretching by external I²C devices is not supported.

10.5 SPI INTERFACE

The ICM-45605 supports 3-wire or 4-wire SPI for the host interface. The ICM-45605 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 24 MHz (it is 20MHz at VDDIO 1.2V)
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the Register Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

Register Address format

| MSB | | | | | | | LSB |
|-----|----|----|----|----|----|----|-----|
| R/W | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

SPI Data format

| MSB | | | | | | | LSB |
|-----|----|----|----|----|----|----|-----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

6. Supports Single or Burst Read/Writes.

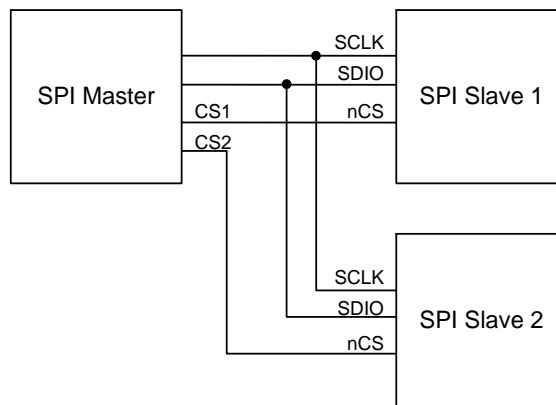


Figure 11. Typical SPI Master/Slave Configuration

11 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

11.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

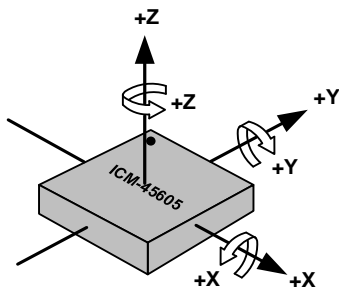
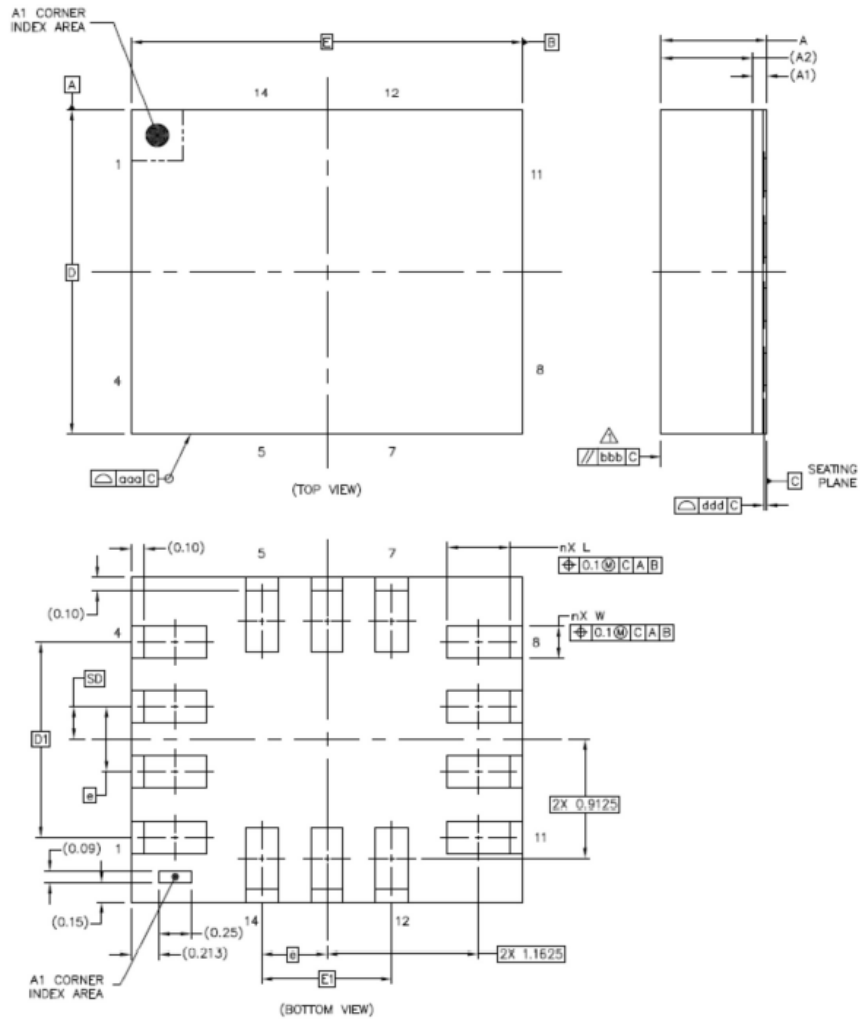


Figure 12. Orientation of Axes of Sensitivity and Polarity of Rotation

11.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.81) mm NiAu pad finish



| | SYMBOLS | DIMENSIONS IN MILLIMETERS | | |
|------------------------------------|------------|---------------------------|-------|-------|
| | | MIN | NOM | MAX |
| Total Thickness | A | 0.76 | 0.81 | 0.86 |
| Substrate Thickness | A1 | 0.105 | | REF |
| Mold Thickness | A2 | 0.7 | | REF |
| Body Size | D | | 2.5 | BSC |
| | E | | 3 | BSC |
| Lead Width | W | 0.2 | 0.25 | 0.3 |
| Lead Length | L | 0.425 | 0.475 | 0.525 |
| Lead Pitch | e | 0.5 | | BSC |
| Lead Count | n | 14 | | |
| Edge Ball Center to Center | D1 | 1.5 | | BSC |
| | E1 | 1 | | BSC |
| Body Center to Contact Ball | SD | 0.25 | | BSC |
| | SE | --- | | BSC |
| Package Edge Tolerance | aaa | 0.1 | | |
| Mold Flatness | bbb | 0.2 | | |
| Coplanarity | ddd | 0.08 | | |

12 DEVICE PACKAGE IN TAPE AND REEL

ICM-45605 devices are packaged in the tape and reel as shown in the figures below.

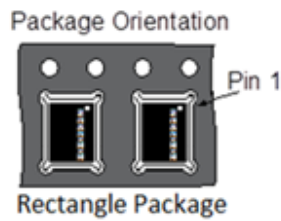


Figure 13. ICM-45605 Device Package in Tape and Reel

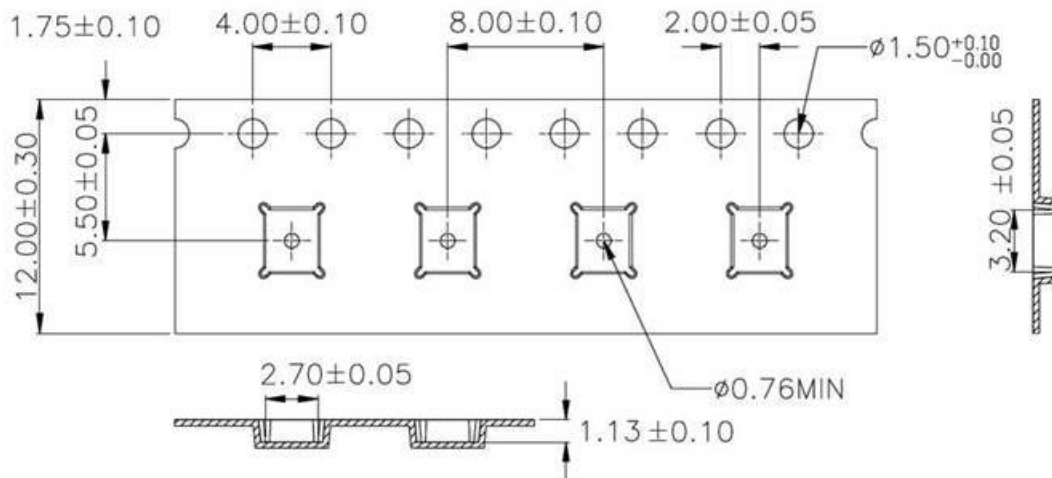
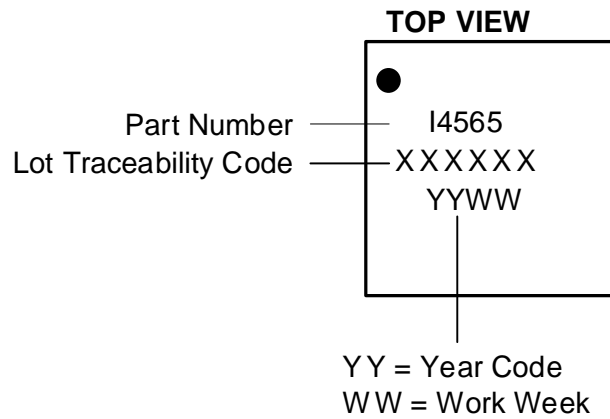


Figure 14. Tape Dimensions with ICM-45605 Device Package

13 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-45605 devices is summarized below:

| Part Number | Part Number Package Marking |
|-------------|-----------------------------|
| ICM-45605 | I4565 |



14 INDIRECT REGISTER ACCESS

14.1 HOST INDIRECT ACCESS REGISTER (IREG)

An IREG is a register or a memory storage element that is not addressed directly by a 7-bit address. IREGs can only be addressed using an internal 16-bit address. Indirect register access procedures described in this section must be used to access all IREGs.

The host configures the internal 16-bit address by programming following registers:
{ireg_addr_15_8[7:0], ireg_addr_7_0[7:0]}.

14.2 GENERAL RULES FOR ACCESSING IREG

1. Burst-write and burst-read operations are not supported when accessing IREGs from the host.
2. Reading of an IREG is done on a read-pre-fetch basis (details in IREG READ section below).
3. A minimum wait time (refer to section MINIMUM WAIT TIME GAP below for details) is required between two consecutive read/write access to an IREG.

14.3 MINIMUM WAIT TIME-GAP

The minimum time gap between two consecutive IREG accesses for various IREG components is 4 μ s.

14.4 IREG WRITE

Procedure for writing to an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
 - a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - b. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - c. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - d. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - e. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. The host programs the write data to the IREG_DATA register.
3. The above programming steps must be performed in a single burst-write transaction to prevent an unintended read-pre-fetch operation.
4. After the IREG_DATA register is written, an internal operation is triggered to pass the contents from the IREG_DATA register to a register pointed by {IREG_ADDR_7_0, IREG_ADDR_15_8}.
5. After the contents from the IREG_DATA register is written to the selected register, the internal 16-bit address is auto-incremented.
6. After a minimum wait time-gap, the host can write to the IREG_DATA register again, which is effectively writing to the register pointed by the post-auto-incremented address.
7. Or, after a minimum wait time-gap, the host can program a new destination address for the next write operation.

14.5 IREG READ

Procedure for reading from an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
 - a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - b. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - c. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - d. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
 - e. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. Upon the CSB=1 (SPI) or STOP (I2C) after the above programming, an internal read-pre-fetch operation is triggered.
3. The internal read-pre-fetch operation returns the desired data, which is saved to the IREG_DATA register.
4. After a minimum wait time-gap, the host reads the IREG_DATA register to retrieve the read-data.
5. After the host reads the IREG_DATA register, the internal 16-bit address is auto-incremented, and another internal read-pre-fetch is automatically triggered, to fetch data from the IREG register pointed to by the post-auto-incremented address.
6. After a minimum wait time-gap, the host can either read the IREG_DATA register to get the read-data from the next address location, or it can program a new read address.

15 DEVICE CONFIGURATION FOR DATA ENDIANNES

By default the device data endianness is Little Endian, for data in Sensor Data Registers and FIFO, and for FIFO Count. User must set register field SREG_DATA_ENDIAN_SEL in register SREG_CTRL to 1, to enable Big Endian data format for data in Sensor Data Registers and FIFO, and for FIFO Count.

Data descriptions in the register map for Sensor Data Registers, FIFO data, and FIFO Count are for the commonly used Big Endian format.

16 REGISTER MAP

This section lists the register map for the ICM-45605, for user bank 0, IMEM_SRAM, IPREG_BAR, IPREG_TOP1, IPREG_SYS1, IPREG_SYS2.

Please refer to the procedure in Section 14 for configuring device data endianness before using the register map.

16.1 USER BANK 0 REGISTER MAP

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|------------------|------------|---------------------------|-----------------------------|---------------------------|---------------------------------|--------------------------|----------------------|-------------------------|--------------------------|---------------|
| 00 | 00 | ACCEL_DATA_X1_UI | SYNCR | ACCEL_DATA_X_UI[15:8] | | | | | | | | |
| 01 | 01 | ACCEL_DATA_X0_UI | SYNCR | ACCEL_DATA_X_UI[7:0] | | | | | | | | |
| 02 | 02 | ACCEL_DATA_Y1_UI | SYNCR | ACCEL_DATA_Y_UI[15:8] | | | | | | | | |
| 03 | 03 | ACCEL_DATA_Y0_UI | SYNCR | ACCEL_DATA_Y_UI[7:0] | | | | | | | | |
| 04 | 04 | ACCEL_DATA_Z1_UI | SYNCR | ACCEL_DATA_Z_UI[15:8] | | | | | | | | |
| 05 | 05 | ACCEL_DATA_Z0_UI | SYNCR | ACCEL_DATA_Z_UI[7:0] | | | | | | | | |
| 06 | 06 | GYRO_DATA_X1_UI | SYNCR | GYRO_DATA_X_UI[15:8] | | | | | | | | |
| 07 | 07 | GYRO_DATA_X0_UI | SYNCR | GYRO_DATA_X_UI[7:0] | | | | | | | | |
| 08 | 08 | GYRO_DATA_Y1_UI | SYNCR | GYRO_DATA_Y_UI[15:8] | | | | | | | | |
| 09 | 09 | GYRO_DATA_Y0_UI | SYNCR | GYRO_DATA_Y_UI[7:0] | | | | | | | | |
| 0A | 10 | GYRO_DATA_Z1_UI | SYNCR | GYRO_DATA_Z_UI[15:8] | | | | | | | | |
| 0B | 11 | GYRO_DATA_Z0_UI | SYNCR | GYRO_DATA_Z_UI[7:0] | | | | | | | | |
| 0C | 12 | TEMP_DATA1_UI | SYNCR | TEMP_DATA_UI[15:8] | | | | | | | | |
| 0D | 13 | TEMP_DATA0_UI | SYNCR | TEMP_DATA_UI[7:0] | | | | | | | | |
| 0E | 14 | TMST_FSYNCH | SYNCR | TMST_FSYNCH_DATA_UI[15:8] | | | | | | | | |
| 0F | 15 | TMST_FSYNCL | SYNCR | TMST_FSYNCH_DATA_UI[7:0] | | | | | | | | |
| 10 | 16 | PWR_MGMT0 | R/W | - | | | | GYRO_MODE | | ACCEL_MODE | | |
| 12 | 18 | FIFO_COUNT_0 | R | FIFO_DATA_CNT[15:8] | | | | | | | | |
| 13 | 19 | FIFO_COUNT_1 | R | FIFO_DATA_CNT[7:0] | | | | | | | | |
| 14 | 20 | FIFO_DATA | R | FIFO_DATA | | | | | | | | |
| 16 | 22 | INT1_CONFIG0 | R/W | INT1_STATUS_EN_RESET_DONE | INT1_STATUS_EN_AUX1_AGC_RDY | INT1_STATUS_EN_AP_AGC_RDY | INT1_STATUS_EN_AP_FSYNC | INT1_STATUS_EN_AUX1_DRDY | INT1_STATUS_EN_DRDY | INT1_STATUS_EN_FIFO_THS | INT1_STATUS_EN_FIFO_FULL | |
| 17 | 23 | INT1_CONFIG1 | R/W | - | INT1_STATUS_EN_APEX_EVENT | INT1_STATUS_EN_I2CM_DONE | INT1_STATUS_EN_I3C_PROTOCOL_ERR | INT1_STATUS_EN_WOM_Z | INT1_STATUS_EN_WOM_Y | INT1_STATUS_EN_WOM_X | INT1_STATUS_EN_PLL_RDY | |
| 18 | 24 | INT1_CONFIG2 | R/W | - | | | | | | INT1_DRIVE | INT1_MODE | INT1_POLARITY |
| 19 | 25 | INT1_STATUS0 | R/C | INT1_STATUS_RESET_DONE | INT1_STATUS_AUX1_AGC_RDY | INT1_STATUS_AP_AGC_RDY | INT1_STATUS_AP_FSYNC | INT1_STATUS_AUX1_DRDY | INT1_STATUS_DRDY | INT1_STATUS_FIFO_THS | INT1_STATUS_FIFO_FULL | |
| 1A | 26 | INT1_STATUS1 | R/C | - | INT1_STATUS_APEX_EVENT | INT1_STATUS_I2CM_DONE | INT1_STATUS_I3C_PROTOCOL_ERR | INT1_STATUS_WOM_Z | INT1_STATUS_WOM_Y | INT1_STATUS_WOM_X | INT1_STATUS_PLL_RDY | |
| 1B | 27 | ACCEL_CONFIG0 | R/W | - | ACCEL_UI_FS_SEL | | | ACCEL_ODR | | | | |
| 1C | 28 | GYRO_CONFIG0 | R/W | GYRO_UI_FS_SEL | | | | GYRO_ODR | | | | |
| 1D | 29 | FIFO_CONFIG0 | R/W | FIFO_MODE | | | FIFO_DEPTH | | | | | |
| 1E | 30 | FIFO_CONFIG1_0 | R/W | FIFO_WM_TH[7:0] | | | | | | | | |
| 1F | 31 | FIFO_CONFIG1_1 | R/W | FIFO_WM_TH[15:8] | | | | | | | | |
| 20 | 32 | FIFO_CONFIG2 | R/W | FIFO_FLUSH | - | | | FIFO_WR_WM_GT_TH | - | | | |
| 21 | 33 | FIFO_CONFIG3 | R/W | - | | FIFO_ES1_EN | FIFO_ES0_EN | FIFO_HIRES_EN | FIFO_GYRO_EN | FIFO_ACCEL_EN | FIFO_IF_EN | |
| 22 | 34 | FIFO_CONFIG4 | R/W | - | | FIFO_COMP_NC_FLOW_CFG | | | FIFO_COMP_EN | FIFO_TMST_FSYNC_EN | FIFO_ES0_6B_9B | |
| 23 | 35 | TMST_WOM_CONFIG | R/W | - | TMST_DELTA_EN | TMST_RESOL | WOM_EN | WOM_MODE | WOM_INT_MODE | WOM_INT_DUR | | |

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|---------------------------|------------|----------------------------------|-----------------------------|------------------------------|-----------------------------------|------------------------------|-----------------------------------|--------------------------------|-----------------------------------|-------------|
| 24 | 36 | FSYNC_CONFIG0 | R/W | - | | | | AP_FSYNC_FL AG_CLEAR_SEL | AP_FSYNC_SEL | | | |
| 27 | 39 | DMP_EXT_SEN_ODR_CFG | R/W | - | EXT_SENSOR_EN | EXT_ODR | | | APEX_ODR | | | |
| 28 | 40 | ODR_DECIMATE_CONFIG | R/W | GYRO_FIFO_ODR_DEC | | | | ACCEL_FIFO_ODR_DEC | | | | |
| 29 | 41 | EDMP_APEX_EN0 | R/W | SMD_EN | R2W_EN | FF_EN | PEDO_EN | TILT_EN | - | | TAP_EN | |
| 2A | 42 | EDMP_APEX_EN1 | R/W | - | EDMP_ENABLE | FEATURE3_EN | - | | POWER_SAVE_EN | INIT_EN | SOFT_HARD_IRON_CORR_EN | |
| 2B | 43 | APEX_BUFFER_MGMT | R/W | FF_DURATION_HOST_RPTR | | FF_DURATION_EDMP_WPTR | | STEP_COUNT_HOST_RPTR | | STEP_COUNT_EDMP_WPTR | | |
| 2C | 44 | INTF_CONFIG0 | R/W | - | | | | | | | AP_SPI_34_MODE | AP_SPI_MODE |
| 2D | 45 | INTF_CONFIG1_OVRD | R/W | - | | | | AP_SPI_34_MODE_OVRD | AP_SPI_34_MODE_OVRD_VAL | AP_SPI_MODE_OVRD | AP_SPI_MODE_OVRD_VAL | |
| 2F | 47 | IOC_PAD_SCENARIO | R | - | | | | | AUX1_MODE | | AUX1_ENABLE | |
| 30 | 48 | IOC_PAD_SCENARIO_AUX_OVRD | R/W | - | | | AUX1_MODE_OVRD | AUX1_ENABLE_OVRD_VAL | | AUX1_ENABLE_OVRD | AUX1_ENABLE_OVRD_VAL | |
| 32 | 50 | DRIVE_CONFIG0 | R/W | - | PADS_I2C_SLEW | | | PADS_SPI_SLEW | | | - | |
| 33 | 51 | DRIVE_CONFIG1 | R/W | - | | PADS_I3C_DDR_SLEW | | | PADS_I3C_SDR_SLEW | | | |
| 34 | 52 | DRIVE_CONFIG2 | R/W | - | | | | | | | PADS_SLEW | |
| 35 | 53 | REG_MISC1 | R/W | - | | | | OSC_ID_OVRD | | | | |
| 39 | 57 | INT_APEX_CONFIG0 | R/W | INT_STATUS_MASK_PIN_R2W_WAKE_DET | INT_STATUS_MASK_PIN_FF_DET | INT_STATUS_MASK_PIN_STEP_DET | INT_STATUS_MASK_PIN_STEP_CNT_OVFL | INT_STATUS_MASK_PIN_TILT_DET | INT_STATUS_MASK_PIN_LOW_G_DET | INT_STATUS_MASK_PIN_HIGH_G_DET | INT_STATUS_MASK_PIN_TAP_DET | |
| 3A | 58 | INT_APEX_CONFIG1 | R/W | - | | | INT_STATUS_MASK_PIN_SA_DONE | - | INT_STATUS_MASK_PIN_SELFTEST_DONE | INT_STATUS_MASK_PIN_SMD_DET | INT_STATUS_MASK_PIN_R2W_SLEEP_DET | |
| 3B | 59 | INT_APEX_STATUS0 | R/C | INT_STATUS_R2W_WAKE_DET | INT_STATUS_FF_DET | INT_STATUS_STEP_DET | INT_STATUS_STEP_CNT_OVFL | INT_STATUS_TILT_DET | INT_STATUS_LOW_G_DET | INT_STATUS_HIGH_G_DET | INT_STATUS_TAP_DET | |
| 3C | 60 | INT_APEX_STATUS1 | R/C | - | | | INT_STATUS_SA_DONE | - | INT_STATUS_SELFTEST_DONE | INT_STATUS_SMD_DET | INT_STATUS_R2W_SLEEP_DET | |
| 56 | 86 | INT2_CONFIG0 | R/W | INT2_STATUS_EN_RESET_DONE | INT2_STATUS_EN_AUX1_AGC_RDY | INT2_STATUS_EN_AP_AGC_RDY | INT2_STATUS_EN_AP_FSYNC | INT2_STATUS_EN_AUX1_DRDY | INT2_STATUS_EN_DRDY | INT2_STATUS_EN_FIFO_THS | INT2_STATUS_EN_FIFO_FULL | |
| 57 | 87 | INT2_CONFIG1 | R/W | - | INT2_STATUS_EN_APEX_EVENT | INT2_STATUS_EN_I2CM_DONE | INT2_STATUS_EN_I3C_PROTOCOL_ERR | INT2_STATUS_EN_WOM_Z | INT2_STATUS_EN_WOM_Y | INT2_STATUS_EN_WOM_X | INT2_STATUS_EN_PLL_RDY | |
| 58 | 88 | INT2_CONFIG2 | R/W | - | | | | | INT2_DRIVE | INT2_MODE | INT2_POLARITY | |
| 59 | 89 | INT2_STATUS0 | R/C | INT2_STATUS_RESET_DONE | INT2_STATUS_AUX1_AGC_RDY | INT2_STATUS_AP_AGC_RDY | INT2_STATUS_AP_FSYNC | INT2_STATUS_AUX1_DRDY | INT2_STATUS_DRDY | INT2_STATUS_FIFO_THS | INT2_STATUS_FIFO_FULL | |
| 5A | 90 | INT2_STATUS1 | R/C | - | INT1_STATUS_APEX_EVENT | INT1_STATUS_I2CM_DONE | INT1_STATUS_I3C_PROTOCOL_ERR | INT1_STATUS_WOM_Z | INT1_STATUS_WOM_Y | INT1_STATUS_WOM_X | INT1_STATUS_PLL_RDY | |
| 72 | 114 | WHO_AM_I | R | WHOAMI | | | | | | | | |
| 73 | 115 | REG_HOST_MSG | R/W | - | | | EDMP_ON_DEMAND_EN | - | | | TESTOPENABLE | |
| 7C | 124 | IREG_ADDR_15_8 | R/W | IREG_ADDR_15_8 | | | | | | | | |
| 7D | 125 | IREG_ADDR_7_0 | R/W | IREG_ADDR_7_0 | | | | | | | | |
| 7E | 126 | IREG_DATA | R/W | IREG_DATA | | | | | | | | |
| 7F | 127 | REG_MISC2 | R/W | - | | | | | | | SOFT_RST | IREG_DONE |

16.2 USER BANK IMEM_SRAM REGISTER MAP

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|-------------------|------------|--------------------------|------|------------|----------------|------------|------------|------------------|---------------------------|-------------|
| 00 | 00 | IMEM_SRAM_REG_0 | R/W | GYRO_X_STR_FT[7:0] | | | | | | | | |
| 01 | 01 | IMEM_SRAM_REG_1 | R/W | GYRO_X_STR_FT[15:8] | | | | | | | | |
| 02 | 02 | IMEM_SRAM_REG_2 | R/W | GYRO_Y_STR_FT[7:0] | | | | | | | | |
| 03 | 03 | IMEM_SRAM_REG_3 | R/W | GYRO_Y_STR_FT[15:8] | | | | | | | | |
| 04 | 04 | IMEM_SRAM_REG_4 | R/W | GYRO_Z_STR_FT[7:0] | | | | | | | | |
| 05 | 05 | IMEM_SRAM_REG_5 | R/W | GYRO_Z_STR_FT[15:8] | | | | | | | | |
| 06 | 06 | IMEM_SRAM_REG_6 | R/W | GYRO_X_CMOS_GAIN_FT[7:0] | | | | | | | | |
| 07 | 07 | IMEM_SRAM_REG_7 | R/W | - | | | | | | | GYRO_X_CMOS_GAIN_FT[11:8] | |
| 08 | 08 | IMEM_SRAM_REG_8 | R/W | GYRO_Y_CMOS_GAIN_FT[7:0] | | | | | | | | |
| 09 | 09 | IMEM_SRAM_REG_9 | R/W | - | | | | | | | GYRO_Y_CMOS_GAIN_FT[11:8] | |
| 0A | 10 | IMEM_SRAM_REG_10 | R/W | GYRO_Z_CMOS_GAIN_FT[7:0] | | | | | | | | |
| 0B | 11 | IMEM_SRAM_REG_11 | R/W | - | | | | | | | GYRO_Z_CMOS_GAIN_FT[11:8] | |
| 38 | 56 | IMEM_SRAM_REG_56 | R/W | ST_AVG_TIME[0] | - | | | | | ST_GYRO_EN | ST_ACCEL_EN | STC_INIT_EN |
| 39 | 57 | IMEM_SRAM_REG_57 | R/W | ST_GYRO_LIMIT | | | ST_ACCEL_LIMIT | | | ST_AVG_TIME[2:1] | | |
| 40 | 64 | IMEM_SRAM_REG_64 | R/W | ST_DEBUG_EN | | | | | | | | |
| 44 | 68 | IMEM_SRAM_REG_68 | R | ST_STATUS | | GZ_ST_PASS | GY_ST_PASS | GX_ST_PASS | AZ_ST_PASS | AY_ST_PASS | AX_ST_PASS | |
| 5C | 92 | IMEM_SRAM_REG_92 | R/W | QUAT_RESET_EN | | | | | | | | |
| 60 | 96 | IMEM_SRAM_REG_96 | R/W | STC_GAIN_GX[7:0] | | | | | | | | |
| 61 | 97 | IMEM_SRAM_REG_97 | R/W | STC_GAIN_GX[15:8] | | | | | | | | |
| 62 | 98 | IMEM_SRAM_REG_98 | R/W | STC_GAIN_GX[23:16] | | | | | | | | |
| 63 | 99 | IMEM_SRAM_REG_99 | R/W | STC_GAIN_GX[31:24] | | | | | | | | |
| 64 | 100 | IMEM_SRAM_REG_100 | R/W | STC_GAIN_GY[7:0] | | | | | | | | |
| 65 | 101 | IMEM_SRAM_REG_101 | R/W | STC_GAIN_GY[15:8] | | | | | | | | |
| 66 | 102 | IMEM_SRAM_REG_102 | R/W | STC_GAIN_GY[23:16] | | | | | | | | |
| 67 | 103 | IMEM_SRAM_REG_103 | R/W | STC_GAIN_GY[31:24] | | | | | | | | |
| 68 | 104 | IMEM_SRAM_REG_104 | R/W | STC_GAIN_GZ[7:0] | | | | | | | | |
| 69 | 105 | IMEM_SRAM_REG_105 | R/W | STC_GAIN_GZ[15:8] | | | | | | | | |
| 6A | 106 | IMEM_SRAM_REG_106 | R/W | STC_GAIN_GZ[23:16] | | | | | | | | |
| 6B | 107 | IMEM_SRAM_REG_107 | R/W | STC_GAIN_GZ[31:24] | | | | | | | | |
| 88 | 136 | IMEM_SRAM_REG_136 | R/W | FF_DURATION_BUF1[7:0] | | | | | | | | |
| 89 | 137 | IMEM_SRAM_REG_137 | R/W | FF_DURATION_BUF1[15:8] | | | | | | | | |
| 8A | 138 | IMEM_SRAM_REG_138 | R/W | FF_DURATION_BUF2[7:0] | | | | | | | | |
| 8B | 139 | IMEM_SRAM_REG_139 | R/W | FF_DURATION_BUF2[15:8] | | | | | | | | |
| 8D | 141 | IMEM_SRAM_REG_141 | R/W | TAP_NUM | | | | | | | | |
| 8E | 142 | IMEM_SRAM_REG_142 | R/W | TAP_AXIS | | | | | | | | |
| 8F | 143 | IMEM_SRAM_REG_143 | R/W | TAP_DIR | | | | | | | | |
| 90 | 144 | IMEM_SRAM_REG_144 | R/W | DOUBLE_TAP_TIMING | | | | | | | | |
| 92 | 146 | IMEM_SRAM_REG_146 | R/W | TILT_RESET_EN | | | | | | | | |
| 9A | 154 | IMEM_SRAM_REG_154 | R/W | PED_STEP_CNT_BUF1[7:0] | | | | | | | | |
| 9B | 155 | IMEM_SRAM_REG_155 | R/W | PED_STEP_CNT_BUF1[15:8] | | | | | | | | |
| 9C | 156 | IMEM_SRAM_REG_156 | R/W | PED_STEP_CNT_BUF2[7:0] | | | | | | | | |
| 9D | 157 | IMEM_SRAM_REG_157 | R/W | PED_STEP_CNT_BUF2[15:8] | | | | | | | | |
| 9F | 159 | IMEM_SRAM_REG_159 | R/W | PED_STEP_CADENCE | | | | | | | | |
| A0 | 160 | IMEM_SRAM_REG_160 | R/W | POWER_ACTIVITY_CLASS | | | | | | | | |
| B6 | 182 | IMEM_SRAM_REG_182 | R/W | ES_RAM_IMAGE_EN | | | | | | | | |
| B9 | 185 | IMEM_SRAM_REG_185 | R/W | ESO_COMPASS_EN | | | | | | | | |
| BA | 186 | IMEM_SRAM_REG_186 | R/W | ES_POWER_MODE | | | | | | | | |
| C4 | 196 | IMEM_SRAM_REG_196 | R/W | POWER_SAVE_TIME[7:0] | | | | | | | | |
| C5 | 197 | IMEM_SRAM_REG_197 | R/W | POWER_SAVE_TIME[15:8] | | | | | | | | |

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------|-------------|-------------------|------------|------|------|------|------|--------------------------------|------|------|------|
| C6 | 198 | IMEM_SRAM_REG_198 | R/W | | | | | POWER_SAVE_TIME[23:16] | | | |
| C7 | 199 | IMEM_SRAM_REG_199 | R/W | | | | | POWER_SAVE_TIME[31:24] | | | |
| 120 | 288 | IMEM_SRAM_REG_288 | R/W | | | | | FF_MIN_DURATION[7:0] | | | |
| 121 | 289 | IMEM_SRAM_REG_289 | R/W | | | | | FF_MIN_DURATION[15:8] | | | |
| 122 | 290 | IMEM_SRAM_REG_290 | R/W | | | | | FF_MIN_DURATION[23:16] | | | |
| 123 | 291 | IMEM_SRAM_REG_291 | R/W | | | | | FF_MIN_DURATION[31:24] | | | |
| 124 | 292 | IMEM_SRAM_REG_292 | R/W | | | | | FF_MAX_DURATION[7:0] | | | |
| 125 | 293 | IMEM_SRAM_REG_293 | R/W | | | | | FF_MAX_DURATION[15:8] | | | |
| 126 | 294 | IMEM_SRAM_REG_294 | R/W | | | | | FF_MAX_DURATION[23:16] | | | |
| 127 | 295 | IMEM_SRAM_REG_295 | R/W | | | | | FF_MAX_DURATION[31:24] | | | |
| 128 | 296 | IMEM_SRAM_REG_296 | R/W | | | | | FF_DEBOUNCE_DURATION[7:0] | | | |
| 129 | 297 | IMEM_SRAM_REG_297 | R/W | | | | | FF_DEBOUNCE_DURATION[15:8] | | | |
| 12A | 298 | IMEM_SRAM_REG_298 | R/W | | | | | FF_DEBOUNCE_DURATION[23:16] | | | |
| 12B | 299 | IMEM_SRAM_REG_299 | R/W | | | | | FF_DEBOUNCE_DURATION[31:24] | | | |
| 130 | 304 | IMEM_SRAM_REG_304 | R/W | | | | | HIGHG_PEAK_TH[7:0] | | | |
| 131 | 305 | IMEM_SRAM_REG_305 | R/W | | | | | HIGHG_PEAK_TH[15:8] | | | |
| 132 | 306 | IMEM_SRAM_REG_306 | R/W | | | | | HIGHG_PEAK_TH_HYST[7:0] | | | |
| 133 | 307 | IMEM_SRAM_REG_307 | R/W | | | | | HIGHG_PEAK_TH_HYST[15:8] | | | |
| 134 | 308 | IMEM_SRAM_REG_308 | R/W | | | | | HIGHG_TIME_TH[7:0] | | | |
| 135 | 309 | IMEM_SRAM_REG_309 | R/W | | | | | HIGHG_TIME_TH[15:8] | | | |
| 13C | 316 | IMEM_SRAM_REG_316 | R/W | | | | | LOWG_PEAK_TH[7:0] | | | |
| 13D | 317 | IMEM_SRAM_REG_317 | R/W | | | | | LOWG_PEAK_TH[15:8] | | | |
| 13E | 318 | IMEM_SRAM_REG_318 | R/W | | | | | LOWG_PEAK_TH_HYST[7:0] | | | |
| 13F | 319 | IMEM_SRAM_REG_319 | R/W | | | | | LOWG_PEAK_TH_HYST[15:8] | | | |
| 140 | 320 | IMEM_SRAM_REG_320 | R/W | | | | | LOWG_TIME_TH[7:0] | | | |
| 141 | 321 | IMEM_SRAM_REG_321 | R/W | | | | | LOWG_TIME_TH[15:8] | | | |
| 188 | 392 | IMEM_SRAM_REG_392 | R/W | | | | | TILT_WAIT_TIME[7:0] | | | |
| 189 | 393 | IMEM_SRAM_REG_393 | R/W | | | | | TILT_WAIT_TIME[15:8] | | | |
| 190 | 400 | IMEM_SRAM_REG_400 | R/W | | | | | TAP_TMAX[7:0] | | | |
| 191 | 401 | IMEM_SRAM_REG_401 | R/W | | | | | TAP_TMAX[15:8] | | | |
| 192 | 402 | IMEM_SRAM_REG_402 | R/W | | | | | TAP_TMIN | | | |
| 193 | 403 | IMEM_SRAM_REG_403 | R/W | | | | | TAP_MIN_JERK | | | |
| 194 | 404 | IMEM_SRAM_REG_404 | R/W | | | | | TAP_SMUDGE_REJECT_THR | | | |
| 195 | 405 | IMEM_SRAM_REG_405 | R/W | | | | | TAP_MAX_PEAK_TOL | | | |
| 196 | 406 | IMEM_SRAM_REG_406 | R/W | | | | | TAP_TAVG | | | |
| 21C | 543 | IMEM_SRAM_REG_540 | R/W | | | | | R2W_SLEEP_TIME_OUT[7:0] | | | |
| 21D | 543 | IMEM_SRAM_REG_541 | R/W | | | | | R2W_SLEEP_TIME_OUT[15:8] | | | |
| 21E | 543 | IMEM_SRAM_REG_542 | R/W | | | | | R2W_SLEEP_TIME_OUT[23:16] | | | |
| 21F | 543 | IMEM_SRAM_REG_543 | R/W | | | | | R2W_SLEEP_TIME_OUT[31:24] | | | |
| 220 | 544 | IMEM_SRAM_REG_544 | R/W | | | | | R2W_SLEEP_GESTURE_DELAY[7:0] | | | |
| 221 | 545 | IMEM_SRAM_REG_545 | R/W | | | | | R2W_SLEEP_GESTURE_DELAY[15:8] | | | |
| 222 | 546 | IMEM_SRAM_REG_546 | R/W | | | | | R2W_SLEEP_GESTURE_DELAY[23:16] | | | |
| 223 | 547 | IMEM_SRAM_REG_547 | R/W | | | | | R2W_SLEEP_GESTURE_DELAY[31:24] | | | |
| 224 | 548 | IMEM_SRAM_REG_548 | R/W | | | | | R2W_MOUNTING_MATRIX[7:0] | | | |
| 225 | 549 | IMEM_SRAM_REG_549 | R/W | | | | | R2W_MOUNTING_MATRIX[15:8] | | | |
| 226 | 550 | IMEM_SRAM_REG_550 | R/W | | | | | R2W_MOUNTING_MATRIX[23:16] | | | |
| 227 | 551 | IMEM_SRAM_REG_551 | R/W | | | | | R2W_MOUNTING_MATRIX[31:24] | | | |
| 22C | 556 | IMEM_SRAM_REG_556 | R/W | | | | | R2W_GRAVITY_FILTER_GAIN[7:0] | | | |
| 22D | 557 | IMEM_SRAM_REG_557 | R/W | | | | | R2W_GRAVITY_FILTER_GAIN[15:8] | | | |
| 22E | 558 | IMEM_SRAM_REG_558 | R/W | | | | | R2W_GRAVITY_FILTER_GAIN[23:16] | | | |
| 22F | 559 | IMEM_SRAM_REG_559 | R/W | | | | | R2W_GRAVITY_FILTER_GAIN[31:24] | | | |

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------|--------------|--|------------|------|------|------|------|------|------|------|--|
| 230 | 560 | IMEM_SRAM_REG_560 | R/W | | | | | | | | R2W_MOTION_THR_ANGLE_COSINE[7:0] |
| 231 | 561 | IMEM_SRAM_REG_561 | R/W | | | | | | | | R2W_MOTION_THR_ANGLE_COSINE[15:8] |
| 232 | 562 | IMEM_SRAM_REG_562 | R/W | | | | | | | | R2W_MOTION_THR_ANGLE_COSINE[23:16] |
| 233 | 563 | IMEM_SRAM_REG_563 | R/W | | | | | | | | R2W_MOTION_THR_ANGLE_COSINE[31:24] |
| 234 | 564 | IMEM_SRAM_REG_564 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_FAST[7:0] |
| 235 | 565 | IMEM_SRAM_REG_565 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_FAST[15:8] |
| 236 | 566 | IMEM_SRAM_REG_566 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_FAST[23:16] |
| 237 | 567 | IMEM_SRAM_REG_567 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_FAST[31:24] |
| 238 | 568 | IMEM_SRAM_REG_568 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_SLOW[7:0] |
| 239 | 569 | IMEM_SRAM_REG_569 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_SLOW[15:8] |
| 23A | 570 | IMEM_SRAM_REG_570 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_SLOW[23:16] |
| 23B | 571 | IMEM_SRAM_REG_571 | R/W | | | | | | | | R2W_MOTION_THR_TIMER_SLOW[31:24] |
| 23C | 572 | IMEM_SRAM_REG_572 | R/W | | | | | | | | R2W_MOTION_PREV_GRAVITY_TIMEOUT[7:0] |
| 23D | 573 | IMEM_SRAM_REG_573 | R/W | | | | | | | | R2W_MOTION_PREV_GRAVITY_TIMEOUT[15:8] |
| 23E | 574 | IMEM_SRAM_REG_574 | R/W | | | | | | | | R2W_MOTION_PREV_GRAVITY_TIMEOUT[23:16] |
| 23F | 575 | IMEM_SRAM_REG_575 | R/W | | | | | | | | R2W_MOTION_PREV_GRAVITY_TIMEOUT[31:24] |
| 240 | 576 | IMEM_SRAM_REG_576 | R/W | | | | | | | | R2W_LAST_GRAVITY_MOTION_TIMER[7:0] |
| 241 | 577 | IMEM_SRAM_REG_577 | R/W | | | | | | | | R2W_LAST_GRAVITY_MOTION_TIMER[15:8] |
| 242 | 578 | IMEM_SRAM_REG_578 | R/W | | | | | | | | R2W_LAST_GRAVITY_MOTION_TIMER[23:16] |
| 243 | 579 | IMEM_SRAM_REG_579 | R/W | | | | | | | | R2W_LAST_GRAVITY_MOTION_TIMER[31:24] |
| 244 | 580 | IMEM_SRAM_REG_580 | R/W | | | | | | | | R2W_LAST_GRAVITY_TIMEOUT[7:0] |
| 245 | 581 | IMEM_SRAM_REG_581 | R/W | | | | | | | | R2W_LAST_GRAVITY_TIMEOUT[15:8] |
| 246 | 582 | IMEM_SRAM_REG_582 | R/W | | | | | | | | R2W_LAST_GRAVITY_TIMEOUT[23:16] |
| 247 | 583 | IMEM_SRAM_REG_583 | R/W | | | | | | | | R2W_LAST_GRAVITY_TIMEOUT[31:24] |
| 248 | 584 | IMEM_SRAM_REG_584 | R/W | | | | | | | | R2W_GESTURE_VALIDITY_TIMEOUT[7:0] |
| 249 | 585 | IMEM_SRAM_REG_585 | R/W | | | | | | | | R2W_GESTURE_VALIDITY_TIMEOUT[15:8] |
| 24A | 586 | IMEM_SRAM_REG_586 | R/W | | | | | | | | R2W_GESTURE_VALIDITY_TIMEOUT[23:16] |
| 24B | 587 | IMEM_SRAM_REG_587 | R/W | | | | | | | | R2W_GESTURE_VALIDITY_TIMEOUT[31:24] |
| 3DC | 988 | IMEM_SRAM_REG_988 | R/W | | | | | | | | PED_STEP_CNT_TH[7:0] |
| 3DD | 989 | IMEM_SRAM_REG_989 | R/W | | | | | | | | PED_STEP_CNT_TH[15:8] |
| 3DE | 990 | IMEM_SRAM_REG_990 | R/W | | | | | | | | PED_STEP_DET_TH[7:0] |
| 3DF | 991 | IMEM_SRAM_REG_991 | R/W | | | | | | | | PED_STEP_DET_TH[15:8] |
| 3E2 | 994 | IMEM_SRAM_REG_994 | R/W | | | | | | | | PED_SB_TIMER_TH[7:0] |
| 3E3 | 995 | IMEM_SRAM_REG_995 | R/W | | | | | | | | PED_SB_TIMER_TH[15:8] |
| 3E8 | 1000 | IMEM_SRAM_REG_1000 | R/W | | | | | | | | PED_LOW_EN_AMP_TH[7:0] |
| 3E9 | 1001 | IMEM_SRAM_REG_1001 | R/W | | | | | | | | PED_LOW_EN_AMP_TH[15:8] |
| 3EA | 1002 | IMEM_SRAM_REG_1002 | R/W | | | | | | | | PED_LOW_EN_AMP_TH[23:16] |
| 3EB | 1003 | IMEM_SRAM_REG_1003 | R/W | | | | | | | | PED_LOW_EN_AMP_TH[31:24] |
| 3EC | 1004 | IMEM_SRAM_REG_1004 | R/W | | | | | | | | PED_SENSITIVITY_MODE |
| 3F0 | 1008 | IMEM_SRAM_REG_1008 | R/W | | | | | | | | PED_AMP_TH[7:0] |
| 3F1 | 1009 | IMEM_SRAM_REG_1009 | R/W | | | | | | | | PED_AMP_TH[15:8] |
| 3F2 | 1010 | IMEM_SRAM_REG_1010 | R/W | | | | | | | | PED_AMP_TH[23:16] |
| 3F3 | 1011 | IMEM_SRAM_REG_1011 | R/W | | | | | | | | PED_AMP_TH[31:24] |
| 3F8 | 1016 | IMEM_SRAM_REG_1016 | R/W | | | | | | | | PED_HI_EN_TH[7:0] |
| 3F9 | 1017 | IMEM_SRAM_REG_1017 | R/W | | | | | | | | PED_HI_EN_TH[15:8] |
| 3FA | 1018 | IMEM_SRAM_REG_1018 | R/W | | | | | | | | PED_HI_EN_TH[23:16] |
| 3FB | 1019 | IMEM_SRAM_REG_1019 | R/W | | | | | | | | PED_HI_EN_TH[31:24] |
| 412 | 1042 | IMEM_SRAM_REG_1042 | R/W | | | | | | | | SMD_SENSITIVITY |
| 490 to 4B3 | 1168 to 1203 | IMEM_SRAM_REG_1168 to IMEM_SRAM_REG_1203 | R/W | | | | | | | | SOFT_IRON_SENSITIVITY_MATRIX[287:0] |

16.3 USER BANK IPREG_BAR REGISTER MAP

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|------------------|------------|---------------------------|-----------------------------|----------------------------|--|---------------------------|--------------------------|----------------------------|----------------------------|--|
| 39 | 57 | IPREG_BAR_REG_57 | R/W | - | IO_OPT0 | IO_OPT1 | - | | | | | |
| 3A | 58 | IPREG_BAR_REG_58 | R/W | PADS_AP_SCLK_PUD_TRIM_D2A | PADS_AP_SCLK_PE_TRIM_D2A | - | PADS_AP_CS_PUD_TRIM_D2A | PADS_AP_CS_PE_TRIM_D2A | - | | IO_OPT2 | |
| 3B | 59 | IPREG_BAR_REG_59 | R/W | PADS_PIN7_PE_TRIM_D2A | - | PADS_AP_SDO_PUD_TRIM_D2A | PADS_AP_SDO_PUD_TRIM_D2A | - | PADS_AP_SDO_PUD_TRIM_D2A | PADS_AP_SDO_PUD_TRIM_D2A | - | |
| 3C | 60 | IPREG_BAR_REG_60 | R/W | - | PADS_AUX1_SCLK_PUD_TRIM_D2A | PADS_AUX1_SCLK_PE_TRIM_D2A | PADS_AUX1_SCLK_TP2_FRM_PAD_DISABLER_TRIM_D2A | PADS_AUX1_CS_PUD_TRIM_D2A | PADS_AUX1_CS_PE_TRIM_D2A | - | PADS_PIN7_CS_PUD_TRIM_D2A | |
| 3D | 61 | IPREG_BAR_REG_61 | R/W | PADS_INT1_PUD_TRIM_D2A | PADS_INT1_PE_TRIM_D2A | - | PADS_AUX1_SDO_PUD_TRIM_D2A | PADS_AUX1_SDO_PE_TRIM_D2A | - | PADS_AUX1_SDO_PUD_TRIM_D2A | PADS_AUX1_SDO_PUD_TRIM_D2A | |
| 3E | 62 | IPREG_BAR_REG_62 | R/W | - | | | | | PADS_INT2_PUD_TRIM_D2A | PADS_INT2_PE_TRIM_D2A | - | |

16.4 USER BANK IPREG_TOP1 REGISTER MAP

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|---------------------|------------|----------------|-----------------|--------------|--------------|---------------|------------------|-----------|---------------------|--|
| 06 | 06 | I2CM_COMMAND_0 | R/W | ENDFLAG_0 | CH_SEL_0 | R_W_0 | | BURSTLEN_0 | | | | |
| 07 | 07 | I2CM_COMMAND_1 | R/W | ENDFLAG_1 | CH_SEL_1 | R_W_1 | | BURSTLEN_1 | | | | |
| 08 | 08 | I2CM_COMMAND_2 | R/W | ENDFLAG_2 | CH_SEL_2 | R_W_2 | | BURSTLEN_2 | | | | |
| 09 | 09 | I2CM_COMMAND_3 | R/W | ENDFLAG_3 | CH_SEL_3 | R_W_3 | | BURSTLEN_3 | | | | |
| 0E | 14 | I2CM_DEV_PROFILE0 | R/W | RD_ADDRESS_0 | | | | | | | | |
| 0F | 15 | I2CM_DEV_PROFILE1 | R/W | - | DEV_ID_0 | | | | | | | |
| 10 | 16 | I2CM_DEV_PROFILE2 | R/W | RD_ADDRESS_1 | | | | | | | | |
| 11 | 17 | I2CM_DEV_PROFILE3 | R/W | - | DEV_ID_1 | | | | | | | |
| 16 | 22 | I2CM_CONTROL | RWS | - | I2CM_RESTART_EN | - | | I2CM_SPEED | - | | I2CM_GO | |
| 18 | 24 | I2CM_STATUS | R | - | | I2CM_SDA_ERR | I2CM_SCL_ERR | I2CM_SRST_ERR | I2CM_TIMEOUT_ERR | I2CM_DONE | I2CM_BUSY | |
| 1A | 26 | I2CM_EXT_DEV_STATUS | | - | | | | | | | I2CM_EXT_DEV_STATUS | |
| 1B | 27 | I2CM_RD_DATA0 | RWS | I2CM_RD_DATA0 | | | | | | | | |
| 1C | 28 | I2CM_RD_DATA1 | RWS | I2CM_RD_DATA1 | | | | | | | | |
| 1D | 29 | I2CM_RD_DATA2 | RWS | I2CM_RD_DATA2 | | | | | | | | |
| 1E | 30 | I2CM_RD_DATA3 | RWS | I2CM_RD_DATA3 | | | | | | | | |
| 1F | 31 | I2CM_RD_DATA4 | RWS | I2CM_RD_DATA4 | | | | | | | | |
| 20 | 32 | I2CM_RD_DATA5 | RWS | I2CM_RD_DATA5 | | | | | | | | |
| 21 | 33 | I2CM_RD_DATA6 | RWS | I2CM_RD_DATA6 | | | | | | | | |
| 22 | 34 | I2CM_RD_DATA7 | RWS | I2CM_RD_DATA7 | | | | | | | | |
| 23 | 35 | I2CM_RD_DATA8 | RWS | I2CM_RD_DATA8 | | | | | | | | |
| 24 | 36 | I2CM_RD_DATA9 | RWS | I2CM_RD_DATA9 | | | | | | | | |
| 25 | 37 | I2CM_RD_DATA10 | RWS | I2CM_RD_DATA10 | | | | | | | | |
| 26 | 38 | I2CM_RD_DATA11 | RWS | I2CM_RD_DATA11 | | | | | | | | |
| 27 | 39 | I2CM_RD_DATA12 | RWS | I2CM_RD_DATA12 | | | | | | | | |
| 28 | 40 | I2CM_RD_DATA13 | RWS | I2CM_RD_DATA13 | | | | | | | | |
| 29 | 41 | I2CM_RD_DATA14 | RWS | I2CM_RD_DATA14 | | | | | | | | |
| 2A | 42 | I2CM_RD_DATA15 | RWS | I2CM_RD_DATA15 | | | | | | | | |
| 2B | 43 | I2CM_RD_DATA16 | RWS | I2CM_RD_DATA16 | | | | | | | | |
| 2C | 44 | I2CM_RD_DATA17 | RWS | I2CM_RD_DATA17 | | | | | | | | |
| 2D | 45 | I2CM_RD_DATA18 | RWS | I2CM_RD_DATA18 | | | | | | | | |

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | |
|------------|-------------|-------------------------|------------|-----------------------------|------|----------------------------|------------------|-------------------------------|------------------------|--------------------------------|-----------------------------|--|--|
| 2E | 46 | I2CM_RD_DATA19 | RWS | I2CM_RD_DATA19 | | | | | | | | | |
| 2F | 47 | I2CM_RD_DATA20 | RWS | I2CM_RD_DATA20 | | | | | | | | | |
| 33 | 51 | I2CM_WR_DATA0 | R/W | I2CM_WR_DATA0 | | | | | | | | | |
| 34 | 52 | I2CM_WR_DATA1 | R/W | I2CM_WR_DATA1 | | | | | | | | | |
| 35 | 53 | I2CM_WR_DATA2 | R/W | I2CM_WR_DATA2 | | | | | | | | | |
| 36 | 54 | I2CM_WR_DATA3 | R/W | I2CM_WR_DATA3 | | | | | | | | | |
| 37 | 55 | I2CM_WR_DATA4 | R/W | I2CM_WR_DATA4 | | | | | | | | | |
| 38 | 56 | I2CM_WR_DATA5 | R/W | I2CM_WR_DATA5 | | | | | | | | | |
| 4B | 75 | SIFS_IXC_ERROR_STATUS | R/C | | | | | | | AUX1_SIFS_IXC_TIMEOUT_ERR | SIFS_IXC_TIMEOUT_ERR | | |
| 4F | 79 | EDMP_PRGRM_IRQ0_0 | R/W | PRGRM_STRT_ADDR_IRQ_0[7:0] | | | | | | | | | |
| 50 | 80 | EDMP_PRGRM_IRQ0_1 | R/W | PRGRM_STRT_ADDR_IRQ_0[15:8] | | | | | | | | | |
| 51 | 81 | EDMP_PRGRM_IRQ1_0 | R/W | PRGRM_STRT_ADDR_IRQ_1[7:0] | | | | | | | | | |
| 52 | 82 | EDMP_PRGRM_IRQ1_1 | R/W | PRGRM_STRT_ADDR_IRQ_1[15:8] | | | | | | | | | |
| 53 | 83 | EDMP_PRGRM_IRQ2_0 | R/W | PRGRM_STRT_ADDR_IRQ_2[7:0] | | | | | | | | | |
| 54 | 84 | EDMP_PRGRM_IRQ2_1 | R/W | PRGRM_STRT_ADDR_IRQ_2[15:8] | | | | | | | | | |
| 55 | 85 | EDMP_SP_START_ADDR | R/W | EDMP_SP_START_ADDR | | | | | | | | | |
| 58 | 88 | SMC_CONTROL_0 | R/W | | | | ACCEL_LP_CLK_SEL | TEMP_DIS | TMST_FORCE_AUX_FINE_EN | TMST_FSYNC_EN | TMST_EN | | |
| 59 | 89 | SMC_CONTROL_1 | R/W | | | | | SREG_AUX_ACCEL_ONLY_EN | | | | | |
| 63 | 99 | STC_CONFIG | R/W | | | | STC_SENSOR_SEL | | | | | | |
| 67 | 103 | SREG_CTRL | R/W | | | | | | | SREG_DATA_ENDIAN_SEL | | | |
| 68 | 104 | SIFS_I3C_STC_CFG | R/W | | | | | I3C_STC_MODE | | | | | |
| 69 | 105 | INT_PULSE_MIN_ON_INTF0 | R/W | | | | | | | INT0_TPULSE_DURATION | | | |
| 6A | 106 | INT_PULSE_MIN_ON_INTF1 | R/W | | | | | | | INT1_TPULSE_DURATION | | | |
| 6B | 107 | INT_PULSE_MIN_OFF_INTF0 | R/W | | | | | | | INT0_TDEASSERT_DISABLE | | | |
| 6C | 108 | INT_PULSE_MIN_OFF_INTF1 | R/W | | | | | | | INT1_TDEASSERT_DISABLE | | | |
| 6E | 110 | ISR_0_7 | R/C | - | | INT_STATUS_ON_DEMAND_PIN_0 | - | INT_STATUS_EXT_ODR_DRDY_PIN_0 | | | INT_STATUS_ACCEL_DRDY_PIN_0 | | |
| 6F | 111 | ISR_8_15 | R/C | - | | INT_STATUS_ON_DEMAND_PIN_1 | - | INT_STATUS_EXT_ODR_DRDY_PIN_1 | | | INT_STATUS_ACCEL_DRDY_PIN_1 | | |
| 70 | 112 | ISR_16_23 | R/C | - | | INT_STATUS_ON_DEMAND_PIN_2 | - | INT_STATUS_EXT_ODR_DRDY_PIN_2 | | | INT_STATUS_ACCEL_DRDY_PIN_2 | | |
| 71 | 113 | STATUS_MASK_PIN_0_7 | R/W | - | | INT_ON_DEMAND_PIN_0_DIS | - | INT_EXT_ODR_DRDY_PIN_0_DIS | | | INT_ACCEL_DRDY_PIN_0_DIS | | |
| 72 | 114 | STATUS_MASK_PIN_8_15 | R/W | - | | INT_ON_DEMAND_PIN_1_DIS | - | INT_EXT_ODR_DRDY_PIN_1_DIS | | | INT_ACCEL_DRDY_PIN_1_DIS | | |
| 73 | 115 | STATUS_MASK_PIN_16_23 | R/W | - | | INT_ON_DEMAND_PIN_2_DIS | - | INT_EXT_ODR_DRDY_PIN_2_DIS | | | INT_ACCEL_DRDY_PIN_2_DIS | | |
| 74 | 116 | INT_I2CM_SOURCE | R/W | | | | | | | INT_STATUS_I2CM_SMC_EXT_ODR_EN | | | |
| 7E | 126 | ACCEL_WOM_X_THR | R/W | WOM_X_TH | | | | | | | | | |
| 7F | 127 | ACCEL_WOM_Y_THR | R/W | WOM_Y_TH | | | | | | | | | |
| 80 | 128 | ACCEL_WOM_Z_THR | R/W | WOM_Z_TH | | | | | | | | | |
| 90 | 144 | SELFTEST | | - | | EN_GZ_ST | EN_GY_ST | EN_GX_ST | EN_AZ_ST | EN_AY_ST | EN_AX_ST | | |
| 97 | 151 | IPREG_MISC | R | | | | | | | EDMP_IDLE | | | |
| A2 | 162 | SW_PLL1_TRIM | R | SW_PLL1_TRIM | | | | | | | | | |

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|-----------------|------------|------|------|------|------|------|------|------|-------------------------|--|
| A7 | 167 | FIFO_SRAM_SLEEP | R/W | - | | | | | | | FIFO_GSLEEP_SHARED_SRAM | |

16.5 USER BANK IPREG_SYS1 REGISTER MAP

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|--------------------|------------|---------------------|----------------------|------|-----------------|------|------|------|-------------------|---|
| 2A | 42 | IPREG_SYS1_REG_42 | R/W | GYRO_X_OFFUSER[7:0] | | | | | | | | |
| 2B | 43 | IPREG_SYS1_REG_43 | R/W | - | GYRO_X_OFFUSER[13:8] | | | | | | | |
| 38 | 56 | IPREG_SYS1_REG_56 | R/W | GYRO_Y_OFFUSER[7:0] | | | | | | | | |
| 39 | 57 | IPREG_SYS1_REG_57 | R/W | - | GYRO_Y_OFFUSER[13:8] | | | | | | | |
| 46 | 70 | IPREG_SYS1_REG_56 | R/W | GYRO_Z_OFFUSER[7:0] | | | | | | | | |
| 47 | 71 | IPREG_SYS1_REG_57 | R/W | - | GYRO_Z_OFFUSER[13:8] | | | | | | | |
| A6 | 166 | IPREG_SYS1_REG_166 | R/W | - | GYRO_SRC_CTRL | | - | | | | | |
| AA | 170 | IPREG_SYS1_REG_170 | R/W | - | | | GYRO_LP_AVG_SEL | | | | | - |
| AC | 172 | IPREG_SYS1_REG_172 | R/W | - | | | | | | | GYRO_UI_LPFBW_SEL | |

16.6 USER BANK IPREG_SYS2 REGISTER MAP

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|------------|-------------|--------------------|------------|----------------------|-----------------------|------|------------------|------|------|------|--------------------|--|
| 18 | 24 | IPREG_SYS2_REG_24 | R/W | ACCEL_X_OFFUSER[7:0] | | | | | | | | |
| 19 | 25 | IPREG_SYS2_REG_25 | R/W | - | ACCEL_X_OFFUSER[13:8] | | | | | | | |
| 20 | 32 | IPREG_SYS2_REG_32 | R/W | ACCEL_Y_OFFUSER[7:0] | | | | | | | | |
| 21 | 33 | IPREG_SYS2_REG_33 | R/W | - | ACCEL_Y_OFFUSER[13:8] | | | | | | | |
| 28 | 40 | IPREG_SYS2_REG_40 | R/W | ACCEL_Z_OFFUSER[7:0] | | | | | | | | |
| 29 | 41 | IPREG_SYS2_REG_41 | R/W | - | ACCEL_Z_OFFUSER[13:8] | | | | | | | |
| 7B | 123 | IPREG_SYS2_REG_123 | R/W | - | | | | | | | ACCEL_SRC_CTRL | |
| 81 | 129 | IPREG_SYS2_REG_129 | R/W | - | | | ACCEL_LP_AVG_SEL | | | | | |
| 83 | 131 | IPREG_SYS2_REG_131 | R/W | - | | | | | | | ACCEL_UI_LPFBW_SEL | |

Detailed register descriptions are provided in the sections that follow.

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

In the sections that follow, some register fields are described as “can be changed on-the-fly.” These are the only register fields that can be changed on-the-fly even if sensor is on. Register fields not described as such must not be changed on-the-fly if sensor is on.

17 USER BANK 0 REGISTER MAP – DESCRIPTIONS

Please refer to the procedure in Section 14 for configuring device data endianness before using the register map.

17.1 ACCEL_DATA_X1_UI

| Name: ACCEL_DATA_X1_UI Address: 00 (00h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|--|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_DATA_X_UI[15:8] | Upper byte of Accel X-axis data for UI path |

17.2 ACCEL_DATA_X0_UI

| Name: ACCEL_DATA_X0_UI Address: 01 (01h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|--|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_DATA_X_UI[7:0] | Lower byte of Accel X-axis data for UI path |

17.3 ACCEL_DATA_Y1_UI

| Name: ACCEL_DATA_Y1_UI Address: 02 (02h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|--|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_DATA_Y_UI[15:8] | Upper byte of Accel Y-axis data for UI path |

17.4 ACCEL_DATA_Y0_UI

| Name: ACCEL_DATA_Y0_UI Address: 03 (03h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|--|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_DATA_Y_UI[7:0] | Lower byte of Accel Y-axis data for UI path |

17.5 ACCEL_DATA_Z1_UI

| Name: ACCEL_DATA_Z1_UI Address: 04 (04h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|--|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_DATA_Z_UI[15:8] | Upper byte of Accel Z-axis data for UI path |

17.6 ACCEL_DATA_Z0_UI

| Name: ACCEL_DATA_Z0_UI | | |
|------------------------|----------------------|---|
| Address: 05 (05h) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_DATA_Z_UI[7:0] | Lower byte of Accel Z-axis data for UI path |

17.7 GYRO_DATA_X1_UI

| Name: GYRO_DATA_X1_UI | | |
|-----------------------|----------------------|--|
| Address: 06 (06h) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_DATA_X_UI[15:8] | Upper byte of Gyro X-axis data for UI path |

17.8 GYRO_DATA_X0_UI

| Name: GYRO_DATA_X0_UI | | |
|-----------------------|---------------------|--|
| Address: 07 (07h) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_DATA_X_UI[7:0] | Lower byte of Gyro X-axis data for UI path |

17.9 GYRO_DATA_Y1_UI

| Name: GYRO_DATA_Y1_UI | | |
|-----------------------|----------------------|--|
| Address: 08 (08h) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_DATA_Y_UI[15:8] | Upper byte of Gyro Y-axis data for UI path |

17.10 GYRO_DATA_Y0_UI

| Name: GYRO_DATA_Y0_UI | | |
|-----------------------|---------------------|--|
| Address: 09 (09h) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_DATA_Y_UI[7:0] | Lower byte of Gyro Y-axis data for UI path |

17.11 GYRO_DATA_Z1_UI

| Name: GYRO_DATA_Z1_UI | | |
|-----------------------|----------------------|--|
| Address: 10 (0Ah) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_DATA_Z_UI[15:8] | Upper byte of Gyro Z-axis data for UI path |

17.12 GYRO_DATA_Z0_UI

| Name: GYRO_DATA_Z0_UI | | |
|-----------------------|---------------------|--|
| Address: 11 (0Bh) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_DATA_Z_UI[7:0] | Lower byte of Gyro Z-axis data for UI path |

17.13 TEMP_DATA1_UI

| Name: TEMP_DATA1_UI | | |
|---------------------|--------------------|--|
| Address: 12 (0Ch) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | TEMP_DATA_UI[15:8] | Upper byte of temperature data for UI path |

17.14 TEMP_DATA0_UI

| Name: TEMP_DATA0_UI | | |
|---------------------|-------------------|--|
| Address: 13 (0Dh) | | |
| Serial IF: SYNCR | | |
| Reset value: 0x00 | | |
| Clock Domain: SCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | TEMP_DATA_UI[7:0] | Lower byte of temperature data for UI path |

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

$$\text{Temperature in Degrees Centigrade} = (\text{TEMP_DATA} / 128) + 25$$

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

$$\text{Temperature in Degrees Centigrade} = (\text{FIFO_TEMP_DATA} / 2) + 25$$

17.15 TMST_FSYNCH

| Name: TMST_FSYNCH Address: 14 (0Eh) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|---|---------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TMST_FSYNCH_DATA_UI[15:8] | Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register |

17.16 TMST_FSYNCL

| Name: TMST_FSYNCL Address: 15 (0Fh) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK | | |
|---|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TMST_FSYNCH_DATA_UI[7:0] | Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register |

17.17 PWR_MGMT0

| Name: PWR_MGMT0 Address: 16 (10h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|------------|--|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:2 | GYRO_MODE | 00: Turns gyroscope off 01: Places gyroscope in Standby Mode 10: Places gyroscope in Low Power (LP) Mode 11: Places gyroscope in Low Noise (LN) Mode Can be changed on-the-fly. |
| 1:0 | ACCEL_MODE | 00: Turns accelerometer off 01: Turns accelerometer off 10: Places accelerometer in Low Power (LP) Mode 11: Places accelerometer in Low Noise (LN) Mode Can be changed on-the-fly. |

17.18 FIFO_COUNT_0

Name: FIFO_COUNT_0
 Address: 18 (12h)
 Serial IF: R
 Reset value: 0x00
 Clock Domain: SCLK

| BIT | NAME | FUNCTION |
|-----|---------------------|---|
| 7:0 | FIFO_DATA_CNT[15:8] | High Bits, count indicates the number of packets available in FIFO. |

17.19 FIFO_COUNT_1

Name: FIFO_COUNT_1
 Address: 19 (13h)
 Serial IF: R
 Reset value: 0x00
 Clock Domain: SCLK

| BIT | NAME | FUNCTION |
|-----|--------------------|--|
| 7:0 | FIFO_DATA_CNT[7:0] | Low Bits, count indicates the number of packets available in FIFO. |

17.20 FIFO_DATA

Name: FIFO_DATA
 Address: 20 (14h)
 Serial IF: R
 Reset value: 0x7F
 Clock Domain: SCLK

| BIT | NAME | FUNCTION |
|-----|-----------|----------------|
| 7:0 | FIFO_DATA | FIFO data port |

17.21 INT1_CONFIG0

| Name: INT1_CONFIG0 Address: 22 (16h) Serial IF: R/W Reset value: 0x80 Clock Domain: MCLK | | |
|--|-------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | INT1_STATUS_EN_RESET_DONE | Enable interrupt status bit to flag the occurrence of Reset Done event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 6 | INT1_STATUS_EN_AUX1_AGC_RDY | Enable interrupt status bit to flag the occurrence of AUX1 AGC Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 5 | INT1_STATUS_EN_AP_AGC_RDY | Enable interrupt status bit to flag the occurrence of UI AGC Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 4 | INT1_STATUS_EN_AP_FSYNC | Enable interrupt status bit to flag the occurrence of UI FSYNC event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 3 | INT1_STATUS_EN_AUX1_DRDY | Enable interrupt status bit to flag the occurrence of AUX1 Data Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 2 | INT1_STATUS_EN_DRDY | Enable interrupt status bit to flag the occurrence of UI Data Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 1 | INT1_STATUS_EN_FIFO_THRESHOLD | Enable interrupt status bit to flag the occurrence of FIFO count \geq FIFO threshold event on INT1 |

| | | |
|---|--------------------------|---|
| | | <p>0: Disable interrupt. 1: Enable interrupt.</p> <p>Setting can be changed by UI interface.</p> |
| 0 | INT1_STATUS_EN_FIFO_FULL | <p>Enable interrupt status bit to flag the occurrence of FIFO full event on INT1</p> <p>0: Disable interrupt. 1: Enable interrupt.</p> <p>Setting can be changed by UI interface.</p> |

17.22 INT1_CONFIG1

| Name: INT1_CONFIG1 Address: 23 (17h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|---------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | INT1_STATUS_EN_APEX_EVENT | Enable interrupt status bit to flag the occurrence of APEX event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 5 | INT1_STATUS_EN_I2CM_DONE | Enable interrupt status bit to flag the completion of I ² C master event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 4 | INT1_STATUS_EN_I3C_PROTOCOL_ERR | Enable interrupt status bit to flag the occurrence of I3C Protocol Error event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 3 | INT1_STATUS_EN_WOM_Z | Enable interrupt status bit to flag the occurrence of WOM on Z-axis event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 2 | INT1_STATUS_EN_WOM_Y | Enable interrupt status bit to flag the occurrence of WOM on Y-axis event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 1 | INT1_STATUS_EN_WOM_X | Enable interrupt status bit to flag the occurrence of WOM on X-axis event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 0 | INT1_STATUS_EN_PLL_RDY | Enable interrupt status bit to flag the occurrence of PLL Ready event on INT1 0: Disable interrupt. |

| | | |
|--|--|---|
| | | 1: Enable interrupt. Setting can be changed by UI interface. |
|--|--|---|

17.23 INT1_CONFIG2

| Name: INT1_CONFIG2 Address: 24 (18h) Serial IF: R/W Reset value: 0x04 Clock Domain: MCLK | | |
|--|---------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2 | INT1_DRIVE | Sets INT1 to open-drain or push-pull 0: Push-pull 1: Open-drain |
| 1 | INT1_MODE | INT1 interrupt mode 0: Pulse mode 1: Latch mode Setting can be changed only when all interrupts of the corresponding serial interface are disabled |
| 0 | INT1_POLARITY | INT1 interrupt polarity 0: Active low 1: Active high Setting can be changed only when all interrupts of the corresponding serial interface are disabled |

17.24 INT1_STATUS0

| Name: INT1_STATUS0 Address: 25 (19h) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | INT1_STATUS_RESET_DONE | Flags the occurrence of Reset Done event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 6 | INT1_STATUS_AUX1_AGC_RDY | Flags the occurrence of AUX1 AGC Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 5 | INT1_STATUS_AP_AGC_RDY | Flags the occurrence of UI AGC Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 4 | INT1_STATUS_AP_FSYNC | Flags the occurrence of UI FSYNC event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 3 | INT1_STATUS_AUX1_DRDY | Flags the occurrence of AUX1 Data Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 2 | INT1_STATUS_DRDY | Flags the occurrence of UI Data Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 1 | INT1_STATUS_FIFO_THS | Flags the occurrence of FIFO count \geq FIFO threshold event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 0 | INT1_STATUS_FIFO_FULL | Flags the occurrence of FIFO full event on INT1 0: Interrupt did not occur 1: Interrupt occurred |

17.25 INT1_STATUS1

| Name: INT1_STATUS1 Address: 26 (1Ah) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | INT1_STATUS_APEX_EVENT | Flags the occurrence of APEX event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 5 | INT1_STATUS_I2CM_DONE | Flags the occurrence of I ² C Master Done event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 4 | INT1_STATUS_I3C_PROTOCOL_ERR | Flags the occurrence of I3C SM Protocol Error event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 3 | INT1_STATUS_WOM_Z | Flags the occurrence of Z-axis WOM event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 2 | INT1_STATUS_WOM_Y | Flags the occurrence of Y-axis WOM event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 1 | INT1_STATUS_WOM_X | Flags the occurrence of X-axis WOM event on INT1 0: Interrupt did not occur 1: Interrupt occurred |
| 0 | INT1_STATUS_PLL_RDY | Flags the occurrence of PLL Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred |

17.26 ACCEL_CONFIG0

| Name: ACCEL_CONFIG0 Address: 27 (1Bh) Serial IF: R/W Reset value: 0x06 Clock Domain: MCLK | | |
|---|-----------------|--|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6:4 | ACCEL_UI_FS_SEL | Full scale select for accelerometer UI interface output 000: Reserved 001: ±16g 010: ±8g 011: ±4g 100: ±2g 101: Reserved 110: Reserved 111: Reserved Can be changed on-the-fly. |
| 3:0 | ACCEL_ODR | Accelerometer ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: 6.4kHz (LN mode) 0100: 3.2kHz (LN mode) 0101: 1.6kHz (LN mode) 0110: 800Hz (LN mode) 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode) Can be changed on-the-fly. |

17.27 GYRO_CONFIG0

| Name: GYRO_CONFIG0 Address: 28 (1Ch) Serial IF: R/W Reset value: 0x06 Clock Domain: MCLK | | |
|--|----------------|--|
| BIT | NAME | FUNCTION |
| 7:4 | GYRO_UI_FS_SEL | Full scale select for gyroscope UI interface output 0000: Reserved 0001: ±2000dps 0010: ±1000dps 0011: ±500dps 0100: ±250dps 0101: ±125dps 0110: ±62.5dps 0111: ±31.25dps 1000: ±15.625dps Rest of the settings are reserved Can be changed on-the-fly. |
| 3:0 | GYRO_ODR | Gyroscope ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: 6.4kHz (LN mode) 0100: 3.2kHz (LN mode) 0101: 1.6kHz (LN mode) 0110: 800Hz (LN mode) 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode) Can be changed on-the-fly. |

17.28 FIFO_CONFIG0

| Name: FIFO_CONFIG0 Address: 29 (1Dh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | FIFO_MODE | Set the FIFO operation mode. 00: Bypass (disabled) 01: Stream mode - Frames are overwritten when the FIFO full condition is reached. Supported only for 8, 16, 20 bytes frame size. When this mode is selected for 32 or 64 bytes frame sizes, FIFO remains in Bypass mode. 10: Stop-on-full mode - Frames are not stored in FIFO once the FIFO full condition is reached. 11: Reserved Can be changed on-the-fly. |
| 5:0 | FIFO_DEPTH | Set the FIFO depth in bytes. 000111: Sets FIFO depth to 2K bytes (recommended setting) 011111: Sets FIFO depth to 8K bytes (valid when all APEX features are disabled) Others: Reserved Can be changed when FIFO is disabled (Bypass mode). |

17.29 FIFO_CONFIG1_0

| Name: FIFO_CONFIG1_0 Address: 30 (1Eh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|-----------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FIFO_WM_TH[7:0] | Lower bits of FIFO watermark threshold. When set to 0, the watermark is disabled. When writing new threshold value, user must first write threshold LSByte (bits [7:0]), then MSByte (bits [15:8]). New threshold register value will take effect only when MSByte is written. Can be changed on-the-fly. |

17.30 FIFO_CONFIG1_1

| Name: FIFO_CONFIG1_1 Address: 31 (1Fh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FIFO_WM_TH[15:8] | Upper bits of FIFO watermark threshold. When set to 0, the watermark is disabled. When writing new threshold value, user must first write threshold LSByte (bits [7:0]), then MSByte (bits [15:8]). New threshold register value will take effect only when MSByte is written. Can be changed on-the-fly. |

17.31 FIFO_CONFIG2

| Name: FIFO_CONFIG2 Address: 32 (20h) Serial IF: R/W Reset value: 0x20 Clock Domain: MCLK | | |
|--|------------------|--|
| BIT | NAME | FUNCTION |
| 7 | FIFO_FLUSH | FIFO flush command. When set high the FIFO is flushed, meaning the pointers and control logic is reset. Configuration registers are not reset. Can be changed on-the-fly. |
| 6:4 | - | Reserved |
| 3 | FIFO_WR_WM_GT_TH | Set write watermark interrupt generating condition: 0: Write watermark interrupt generated when FIFO data count is equal to the FIFO watermark threshold 1: Write watermark interrupt generated when FIFO data count is greater than or equal to FIFO watermark threshold Can be changed when FIFO is disabled (Bypass mode). |
| 2:0 | - | Reserved |

17.32 FIFO_CONFIG3

| Name: FIFO_CONFIG3 Address: 33 (21h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|---------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | FIFO_ES1_EN | Enable External Sensor 1 data insertion into FIFO frame |
| 4 | FIFO_ES0_EN | Enable External Sensor 0 data insertion into FIFO frame |
| 3 | FIFO_HIRES_EN | Enable high resolution accel and gyro data insertion into FIFO frame |
| 2 | FIFO_GYRO_EN | Enable gyro data insertion into FIFO frame |
| 1 | FIFO_ACCEL_EN | Enable accel data insertion into FIFO frame |
| 0 | FIFO_IF_EN | <p>Enable Sensor Registers write interface to FIFO. This interface should be enabled when the FIFO is also enabled (i.e., not in bypass mode). A standard enable sequence is:</p> <ol style="list-style-type: none"> 1) Enable FIFO. 2) Enable Sensor Registers to FIFO interface. <p>The opposite sequence should be used for the disable.</p> <p>To prevent power drain, FIFO_IF_EN should be set to 0 if FIFO is in bypass mode.</p> <p>Can be changed on-the-fly.</p> |

17.33 FIFO_CONFIG4

| Name: FIFO_CONFIG4 Address: 34 (22h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:3 | FIFO_COMP_NC_FLOW_CFG | Configures the compression algorithm to write non-compressed packets to FIFO at a certain rate 000: Non-compressed packet flow is disabled 001: Non-compressed packet every 8 frames 010: Non-compressed packet every 16 frames 011: Non-compressed packet every 32 frames 100: Non-compressed packet every 64 frames 101: Non-compressed packet every 128 frames Others: Reserved |
| 2 | FIFO_COMP_EN | 0: FIFO compression disabled 1: FIFO compression enabled |
| 1 | FIFO_TMST_FSYNC_EN | Enable the insertion of the Timestamp or FSYNC data into FIFO frame 0: No Timestamp/FSYNC data inserted into FIFO frame (timestamp fields are 0x0000). FSYNC_TAG_EN bit in FIFO header is 0. 1: Timestamp/FSYNC data inserted into FIFO frame. FSYNC_TAG_EN bit in FIFO header is set on an FSYNC trigger event. |
| 0 | FIFO_ES0_6B_9B | Select number of valid bytes provided by External Sensor 0 0: 6 bytes 1: 9 bytes |

17.34 TMST_WOM_CONFIG

| Name: TMST_WOM_CONFIG Address: 35 (23h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | TMST_DELTA_EN | Time Stamp Delta Enable 0: Time stamp field does not contain the measurement of time since the last occurrence of trigger event 1: Time stamp field contains the measurement of time since the last occurrence of trigger event |
| 5 | TMST_RESOL | Time Stamp Resolution 0: 1 μ s 1: 16 μ s |
| 4 | WOM_EN | Wake on Motion Enable 0: Wake on Motion not enabled 1: Wake on Motion enabled |
| 3 | WOM_MODE | Wake on Motion Mode 0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample |
| 2 | WOM_INT_MODE | Wake on Motion Interrupt 0: Off 1: On |
| 1:0 | WOM_INT_DUR | Wake on Motion Interrupt Duration 00: Wake on Motion interrupt asserted at first over-threshold event 01: Wake on Motion interrupt asserted at second over-threshold event 10: Wake on Motion interrupt asserted at third over-threshold event 11: Wake on Motion interrupt asserted at fourth over-threshold event |

17.35 FSYNC_CONFIG0

| Name: FSYNC_CONFIG0 Address: 36 (24h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-------------------------|--|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3 | AP_FSYNC_FLAG_CLEAR_SEL | Select the AP/UI FSYNC flag clear policy. 0: The FSYNC flag is cleared when UI/AP sensor register is updated. 1: The FSYNC flag is cleared when UI/AP serial interface reads the sensor register LSB of FSYNC tagged axis. |
| 2:0 | AP_FSYNC_SEL | Select the AP/UI sensor that will carry the FSYNC tagging. 0: FSYNC tagging is disabled 1: Tag FSYNC flag to TEMP_DATA_UI LSB 2: Tag FSYNC flag to GYRO_DATA_X_UI LSB 3: Tag FSYNC flag to GYRO_DATA_Y_UI LSB 4: Tag FSYNC flag to GYRO_DATA_Z_UI LSB 5: Tag FSYNC flag to ACCEL_DATA_X_UI LSB 6: Tag FSYNC flag to ACCEL_DATA_Y_UI LSB 7: Tag FSYNC flag to ACCEL_DATA_Z_UI LSB |

17.36 DMP_EXT_SEN_ODR_CFG

| Name: DMP_EXT_SEN_ODR_CFG Address: 39 (27h) Serial IF: R/W Reset value: 0x01 Clock Domain: MCLK | | |
|---|---------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | EXT_SENSOR_EN | 0: Disables generation of ODR event for external sensor operation per the setting of EXT_ODR. 1: Enables generation of ODR event for external sensor operation per the setting of EXT_ODR. |
| 5:3 | EXT_ODR | I ² C master external sensor ODR 000: 3.125Hz 001: 6.25Hz 010: 12.5Hz 011: 25Hz 100: 50Hz 101: 100Hz 110: 200Hz 111: 400Hz |
| 2:0 | APEX_ODR | DMP Output Data Rate. APEX_ODR should be smaller than or equal to both ACCEL_ODR and GYRO_ODR. All rates shown below except 800Hz can be set if Accel UI/AP in in LP mode. Accel UI/AP must be in LN mode to set 800Hz. 000: 25Hz 001: 50Hz 010: 100Hz 011: 200Hz 100: 400Hz 101: 800Hz 110: Reserved 111: Reserved |

17.37 ODR_DECIMATE_CONFIG

Name: ODR_DECIMATE_CONFIG
 Address: 40 (28h)
 Serial IF: R/W
 Reset value: 0x00
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|--------------------|--|
| 7:4 | GYRO_FIFO_ODR_DEC | Decimation factor for Gyroscope FIFO data: 0000: 1 (same are input ODR) 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 1001: 512 1010: 1024 1011: 2048 1100: 4096 1101: Reserved 1110: Reserved 1111: Reserved |
| 3:0 | ACCEL_FIFO_ODR_DEC | Decimation factor for Accelerometer FIFO data: 0000: 1 (same are input ODR) 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 1001: 512 1010: 1024 1011: 2048 1100: 4096 1101: Reserved 1110: Reserved 1111: Reserved |

17.38 EDMP_APEX_EN0

| Name: EDMP_APEX_EN0 | | |
|---------------------|---------|---|
| Address: 41 (29h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7 | SMD_EN | Set 1 to enable SMD algorithm |
| 6 | R2W_EN | Set 1 to enable Raise to Wake algorithm |
| 5 | FF_EN | Set 1 to enable Freefall algorithm |
| 4 | PEDO_EN | Set 1 to enable Pedometer algorithm |
| 3 | TILT_EN | Set 1 to enable Tilt algorithm |
| 2:1 | - | Reserved |
| 0 | TAP_EN | Set 1 to enable Tap algorithm |

17.39 EDMP_APEX_EN1

| Name: EDMP_APEX_EN1 | | |
|---------------------|------------------------|---|
| Address: 42 (2Ah) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | EDMP_ENABLE | Set 1 to enable eDMP |
| 5 | FEATURE3_EN | Set 1 to enable eDMP to run algorithms from RAM image |
| 4:3 | - | Reserved |
| 2 | POWER_SAVE_EN | Set 1 to enable power save mode |
| 1 | INIT_EN | This bit is set by the host to indicate: eDMP executes only the segment of code that initialize constants used by algorithms. |
| 0 | SOFT_HARD_IRON_CORR_EN | Set 1 to enable soft iron hard iron correction |

17.40 APEX_BUFFER_MGMT

| Name: APEX_BUFFER_MGMT Address: 43 (2Bh) Serial IF: R/W (bits 5:4 are R only) Reset value: 0x00 Clock Domain: MCLK | | |
|--|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | FF_DURATION_HOST_RPTR | LSB indicates SRAM address for host to read; MSB indicates size 2 buffer wrap around 00: Host reads buffer 0 01: Host reads buffer 1 10: Host reads buffer 0 11: Host reads buffer 1 |
| 5:4 | FF_DURATION_EDMP_WPTR | Read only register field: LSB indicates SRAM address for eDMP to write; MSB indicates size 2 buffer wrap around 00: eDMP writes to buffer 0 01: eDMP writes to buffer 1 10: eDMP writes to buffer 0 11: eDMP writes to buffer 1 |
| 3:2 | STEP_COUNT_HOST_RPTR | LSB indicates SRAM address for host to read; MSB indicates size 2 buffer wrap around 00: Host reads buffer 0 01: Host reads buffer 1 10: Host reads buffer 0 11: Host reads buffer 1 |
| 1:0 | STEP_COUNT_EDMP_WPTR | Read only register field: LSB indicates SRAM address for eDMP to write; MSB indicates size 2 buffer wrap around 00: eDMP writes to buffer 0 01: eDMP writes to buffer 1 10: eDMP writes to buffer 0 11: eDMP writes to buffer 1 |

17.41 INTF_CONFIG0

| Name: INTF_CONFIG0 Address: 44 (2Ch) Serial IF: R/W (bits 1 and 0 are Read only) Reset value: 0x9A Clock Domain: MCLK | | |
|---|----------------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1 | AP_SPI_34_MODE | Read only register field, shows OTP trim for UI interface SPI in 3-wire or 4-wire mode 0: 3-wire mode 1: 4-wire mode |
| 0 | AP_SPI_MODE | Read only register field, shows OTP trim for UI interface SPI mode selection 0: SPI mode 0 or 3 1: SPI mode 1 or 2 |

17.42 INTF_CONFIG1_OVRD

| Name: INTF_CONFIG1_OVRD Address: 45 (2Dh) Serial IF: R/W Reset value: 0x0C Clock Domain: SCLK | | |
|---|-------------------------|---|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3 | AP_SPI_34_MODE_OVRD | 0: Override disable for AP interface SPI 4-wire/3-wire modes 1: Override enable for AP interface SPI 4-wire/3-wire modes |
| 2 | AP_SPI_34_MODE_OVRD_VAL | Override value for AP interface SPI 4-wire/3-wire modes 0: SPI 3-wire mode 1: SPI 4-wire mode |
| 1 | AP_SPI_MODE_OVRD | 0: Override disable for AP interface SPI_MODE value 1: Override enable for AP interface SPI_MODE value |
| 0 | AP_SPI_MODE_OVRD_VAL | Override value for AP interface SPI Mode 0: SPI mode 0 or 3 1: SPI mode 1 or 2 |

17.43 IOC_PAD_SCENARIO

| Name: IOC_PAD_SCENARIO Address: 47 (2Fh) Serial IF: R Reset value: 0x09 Clock Domain: MCLK | | |
|--|-------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:1 | AUX1_MODE | Read only register field, effective only when AUX1_ENABLE is 1. Selects AUX1 mode: 00: Reserved 01: AUX1 in I2C Master mode 10: AUX1 in I2C Master Bypass mode (Enable only when AP is not in SPI mode) 11: Reserved |
| 0 | AUX1_ENABLE | Read only register field, enable or disable AUX1 0: AUX1 disabled 1: AUX1 enabled |

17.44 IOC_PAD_SCENARIO_AUX_OVRD

| Name: IOC_PAD_SCENARIO_AUX_OVRD Address: 48 (30h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:5 | - | Reserved |
| 4 | AUX1_MODE_OVRD | Override enable for AUX1_MODE 0: Disable 1: Enable |
| 3:2 | AUX1_ENABLE_OVRD_VAL | Override value for AUX1_ENABLE. Effective only when AUX1_ENABLE is 1. Selects modes of AUX1 use: 0: Reserved 1: AUX1 in I2C Master mode 2: AUX1 in I2C Master Bypass mode (enable only when AP is not in SPI mode) Note: When enabling the I2C Master Bypass mode, this register should be programmed individually, not as part of a burst transaction. |
| 1 | AUX1_ENABLE_OVRD | Override enable for AUX1_ENABLE 0: Disable 1: Enable |
| 0 | AUX1_ENABLE_OVRD_VAL | Override value for AUX1_ENABLE 0: AUX1 disabled 1: AUX1 enabled |

17.45 DRIVE_CONFIG0

| Name: DRIVE_CONFIG0 Address: 50 (32h) Serial IF: R/W Reset value: 0x6C Clock Domain: MCLK | | |
|---|---------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6:4 | PADS_I2C_SLEW | <p>Slew rate control for any pin in the I²C mode of operation, including pins on the AP serial interface when device is a client device of an I²C bus, including pins on the AUX1 serial interface when device is a master device of an I²C bus. Setting of the slew rate takes effect 1.5μs after the register is programmed.</p> <p>000: MIN: 3 ns; TYP: 20 ns; MAX: 136 ns 010: MIN: 2 ns; TYP: 7 ns; MAX: 84 ns Others: Reserved</p> |
| 3:1 | PADS_SPI_SLEW | <p>Slew rate control for any pin in the SPI mode of operation. Setting of the slew rate takes effect 1.5μs after the register is programmed.</p> <p>000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns</p> |
| 0 | - | Reserved |

17.46 DRIVE_CONFIG1

| Name: DRIVE_CONFIG1 Address: 51 (33h) Serial IF: R/W Reset value: 0x36 Clock Domain: MCLK | | |
|---|-------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:3 | PADS_I3C_DDR_SLEW | Slew rate control when device is in I3C SM DDR protocol. Setting of the slew rate takes effect 1.5 μ s after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns |
| 2:0 | PADS_I3C_SDR_SLEW | Slew rate control when device is in I3C SM SDR protocol. Setting of the slew rate takes effect 1.5 μ s after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns |

17.47 DRIVE_CONFIG2

| Name: DRIVE_CONFIG2 Address: 52 (34h) Serial IF: R/W Reset value: 0x06 Clock Domain: MCLK | | |
|---|-----------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | PADS_SLEW | Slew rate control for INT1 pin at all times. Slew rate control for all pins before OTP copy operation is completed. Setting of the slew rate takes effect 1.5 μ s after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns |

17.48 REG_MISC1

| Name: REG_MISC1 Address: 53 (35h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-------------|---|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:0 | OSC_ID_OVRD | Selects MCLK source. 0000: MCLK source requested by internal logic (default) 0010: Requests internal relaxation oscillator 1000: Requests external clock Rest: Reserved The selected clock source is the highest index that's requested and that is ready. |

17.49 INT_APEX_CONFIG0

| Name: INT_APEX_CONFIG0 Address: 57 (39h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|-----------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | INT_STATUS_MASK_PIN_R2W_WAKE_DET | Enable interrupt pin assertion when the INT_STATUS_R2W_WAKE_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 6 | INT_STATUS_MASK_PIN_FF_DET | Enable interrupt pin assertion when the INT_STATUS_FF_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 5 | INT_STATUS_MASK_PIN_STEP_DET | Enable interrupt pin assertion when the INT_STATUS_STEP_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 4 | INT_STATUS_MASK_PIN_STEP_CNT_OVFL | Enable interrupt pin assertion when the INT_STATUS_STEP_CNT_OVFL status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 3 | INT_STATUS_MASK_PIN_TILT_DET | Enable interrupt pin assertion when the INT_STATUS_TILT_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 2 | INT_STATUS_MASK_PIN_LOW_G_DET | Enable interrupt pin assertion when the INT_STATUS_LOW_G_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 1 | INT_STATUS_MASK_PIN_HIGH_G_DET | Enable interrupt pin assertion when the INT_STATUS_HIGH_G_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |
| 0 | INT_STATUS_MASK_PIN_TAP_DET | Enable interrupt pin assertion when the INT_STATUS_TAP_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion |

17.50 INT_APEX_CONFIG1

| Name: INT_APEX_CONFIG1 Address: 58 (3Ah) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:5 | - | Reserved |
| 4 | INT_STATUS_MASK_PIN_SA_DONE | 0: Enable interrupt generation when Secure Authentication is done 1: Disable interrupt generation for Secure Authentication |
| 3 | - | Reserved |
| 2 | INT_STATUS_MASK_PIN_SELF_TEST_DONE | 0: Enable interrupt generation when self-test is done 1: Disable interrupt generation for self-test |
| 1 | INT_STATUS_MASK_PIN_SMD_DET | 0: Enable interrupt generation for Significant Motion Detection (SMD) 1: Disable interrupt generation for Significant Motion Detection (SMD) |
| 0 | INT_STATUS_MASK_PIN_R2W_SLEEP_DET | 0: Enable interrupt generation for Wake Sleep Detection 1: Disable interrupt generation for Wake Sleep Detection |

17.51 INT_APEX_STATUS0

| Name: INT_APEX_STATUS0 Address: 59 (3Bh) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | INT_STATUS_R2W_WAKE_DET | 0: Wake interrupt did not occur. 1: Wake interrupt occurred. |
| 6 | INT_STATUS_FF_DET | 0: Freefall interrupt did not occur. 1: Freefall interrupt occurred. |
| 5 | INT_STATUS_STEP_DET | 0: Step Detection interrupt did not occur. 1: Step Detection interrupt occurred. |
| 4 | INT_STATUS_STEP_CNT_OVERFLOW | 0: Step-Count Overflow interrupt did not occur. 1: Step-Count Overflow interrupt occurred. |
| 3 | INT_STATUS_TILT_DET | 0: Tilt Detection interrupt did not occur. 1: Tilt Detection interrupt occurred. |
| 2 | INT_STATUS_LOW_G_DET | 0: LowG Detection interrupt did not occur. 1: LowG Detection interrupt occurred. |
| 1 | INT_STATUS_HIGH_G_DET | 0: HighG Detection interrupt did not occur. 1: HighG Detection interrupt occurred. |
| 0 | INT_STATUS_TAP_DET | 0: Tap Detection interrupt did not occur. 1: Tap Detection interrupt occurred. |

17.52 INT_APEX_STATUS1

| Name: INT_APEX_STATUS1 Address: 60 (3Ch) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:5 | - | Reserved |
| 4 | INT_STATUS_SA_DONE | For EDMP_OUT interface. 0: Secure Authentication interrupt did not occur. 1: Secure Authentication interrupt occurred. |
| 3 | - | Reserved |
| 2 | INT_STATUS_SELFTEST_DONE | 0: Self-Test interrupt did not occur. 1: Self-Test interrupt occurred. |
| 1 | INT_STATUS_SMD_DET | This bit is set to 1 when Significant Motion Detection (SMD) interrupt is generated 0: Significant Motion Detection (SMD) interrupt did not occur. 1: Significant Motion Detection (SMD) interrupt occurred. |
| 0 | INT_STATUS_R2W_SLEEP_DE T | 0: Sleep interrupt did not occur. 1: Sleep interrupt occurred. |

17.53 INT2_CONFIG0

| Name: INT2_CONFIG0 Address: 86 (56h) Serial IF: R/W Reset value: 0x80 Clock Domain: MCLK | | |
|--|-------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | INT2_STATUS_EN_RESET_DONE | Enable interrupt status bit to flag the occurrence of Reset Done event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface. |
| 6 | INT2_STATUS_EN_AUX1_AGC_RDY | Enable interrupt status bit to flag the occurrence of AUX1 AGC Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface. |
| 5 | INT2_STATUS_EN_AP_AGC_RDY | Enable interrupt status bit to flag the occurrence of UI AGC Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface. |
| 4 | INT2_STATUS_EN_AP_FSYNC | Enable interrupt status bit to flag the occurrence of UI FSYNC event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface. |
| 3 | INT2_STATUS_EN_AUX1_DRDY | Enable interrupt status bit to flag the occurrence of AUX1 Data Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface. |
| 2 | INT2_STATUS_EN_DRDY | Enable interrupt status bit to flag the occurrence of UI Data Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface. |
| 1 | INT2_STATUS_EN_FIFO_THRESHOLD | Enable interrupt status bit to flag the occurrence of FIFO count \geq FIFO threshold event on INT2 |

| | | |
|---|--------------------------|---|
| | | <p>0: Disable interrupt. 1: Enable interrupt.</p> <p>Setting can be changed by UI or AUX1 interface.</p> |
| 0 | INT2_STATUS_EN_FIFO_FULL | <p>Enable interrupt status bit to flag the occurrence of FIFO full event on INT2</p> <p>0: Disable interrupt. 1: Enable interrupt.</p> <p>Setting can be changed by UI or AUX1 interface.</p> |

17.54 INT2_CONFIG1

| Name: INT2_CONFIG1 Address: 87 (57h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|---------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | INT2_STATUS_EN_APEX_EVENT | Enable interrupt status bit to flag the occurrence of APEX event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 5 | INT2_STATUS_EN_I2CM_DONE | Enable interrupt status bit to flag the completion of I ² C master event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 4 | INT2_STATUS_EN_I3C_PROTOCOL_ERR | Enable interrupt status bit to flag the occurrence of I3C Protocol Error event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 3 | INT2_STATUS_EN_WOM_Z | Enable interrupt status bit to flag the occurrence of WOM on Z-axis event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 2 | INT2_STATUS_EN_WOM_Y | Enable interrupt status bit to flag the occurrence of WOM on Y-axis event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 1 | INT2_STATUS_EN_WOM_X | Enable interrupt status bit to flag the occurrence of WOM on X-axis event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface. |
| 0 | INT2_STATUS_EN_PLL_RDY | Enable interrupt status bit to flag the occurrence of PLL Ready event on INT2 0: Disable interrupt. |

| | | |
|--|--|---|
| | | 1: Enable interrupt. Setting can be changed by UI interface. |
|--|--|---|

17.55 INT2_CONFIG2

| Name: INT2_CONFIG2 Address: 88 (58h) Serial IF: R/W Reset value: 0x04 Clock Domain: MCLK | | |
|--|---------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2 | INT2_DRIVE | Sets INT2 to open-drain or push-pull 0: Push-pull 1: Open-drain |
| 1 | INT2_MODE | INT2 interrupt mode 0: Pulse mode 1: Latch mode Setting can be changed only when all interrupts of the corresponding serial interface are disabled |
| 0 | INT2_POLARITY | INT2 interrupt polarity 0: Active low 1: Active high Setting can be changed only when all interrupts of the corresponding serial interface are disabled |

17.56 INT2_STATUS0

| Name: INT2_STATUS0 Address: 89 (59h) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | INT2_STATUS_RESET_DONE | Flags the occurrence of Reset Done event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 6 | INT2_STATUS_AUX1_AGC_RDY | Flags the occurrence of AUX1 AGC Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 5 | INT2_STATUS_AP_AGC_RDY | Flags the occurrence of UI AGC Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 4 | INT2_STATUS_AP_FSYNC | Flags the occurrence of UI FSYNC event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 3 | INT2_STATUS_AUX1_DRDY | Flags the occurrence of AUX1 Data Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 2 | INT2_STATUS_DRDY | Flags the occurrence of UI Data Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 1 | INT2_STATUS_FIFO_THS | Flags the occurrence of FIFO count \geq FIFO threshold event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 0 | INT2_STATUS_FIFO_FULL | Flags the occurrence of FIFO full event on INT2 0: Interrupt did not occur 1: Interrupt occurred |

17.57 INT2_STATUS1

| Name: INT2_STATUS1 Address: 90 (5Ah) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|------------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | INT2_STATUS_APEX_EVENT | Flags the occurrence of APEX event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 5 | INT2_STATUS_I2CM_DONE | Flags the occurrence of I ² C Master Done event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 4 | INT2_STATUS_I3C_PROTOCOL_ERR | Flags the occurrence of I3C SM Protocol Error event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 3 | INT2_STATUS_WOM_Z | Flags the occurrence of Z-axis WOM event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 2 | INT2_STATUS_WOM_Y | Flags the occurrence of Y-axis WOM event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 1 | INT2_STATUS_WOM_X | Flags the occurrence of X-axis WOM event on INT2 0: Interrupt did not occur 1: Interrupt occurred |
| 0 | INT2_STATUS_PLL_RDY | Flags the occurrence of PLL Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred |

17.58 WHO_AM_I

| Name: WHO_AM_I Address: 114 (72h) Serial IF: R Reset value: 0xE5 Clock Domain: ALL | | |
|--|--------|---|
| BIT | NAME | FUNCTION |
| 7:0 | WHOAMI | Register to indicate to user which device is being accessed |

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0xE5. This is different from the I²C address of the device as seen on the slave I²C controller by the applications processor.

17.59 REG_HOST_MSG

| Name: REG_HOST_MSG Address: 115 (73h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK | | |
|---|-------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | EDMP_ON_DEMAND_EN | When set, a trigger will be sent which will cause the eDMP to run once. It is automatically reset to 0. |
| 4:1 | - | Reserved |
| 0 | TESTOPENABLE | 1: Enable test operation |

17.60 IREG_ADDR_15_8

| Name: IREG_ADDR_15_8 Address: 124 (7Ch) Serial IF: R/W Reset value: 0xAF Clock Domain: SCLK | | |
|---|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | IREG_ADDR_15_8 | Address bit[15:8] of the 16-bit indirect address for assessing indirect access registers (IREG) Can be changed on-the-fly. |

17.61 IREG_ADDR_7_0

| Name: IREG_ADDR_7_0 Address: 125 (7Dh) Serial IF: R/W Reset value: 0x06 Clock Domain: SCLK | | |
|--|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | IREG_ADDR_7_0 | Address bit[7:0] of the 16-bit indirect address for assessing indirect access registers (IREG) Can be changed on-the-fly. |

17.62 IREG_DATA

| Name: IREG_DATA Address: 126 (7Eh) Serial IF: R/W Reset value: 0x02 Clock Domain: SCLK | | |
|--|-----------|---|
| BIT | NAME | FUNCTION |
| 7:0 | IREG_DATA | Register for indirect access registers (IREG) data read/write operations. Can be changed on-the-fly. |

17.63 REG_MISC2

| Name: REG_MISC2 Address: 127 (7Fh) Serial IF: R/W Reset value: 0x01 Clock Domain: SCLK | | |
|--|-----------|---|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1 | SOFT_RST | 0: Soft reset not enabled. 1: Triggers soft reset operation. The programmed value of 1 is self-cleared to 0 upon completion of soft reset operation. Can be changed on-the-fly. |
| 0 | IREG_DONE | 0: Indicates that an indirect register access operation is in progress. No new indirect register access should be triggered. 1: Indirect register access has completed. New indirect register access can be triggered. |

18 USER BANK IMEM_SRAM REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SRAM. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

18.1 IMEM_SRAM_REG_0

| Name: IMEM_SRAM_REG_0 Address: 00 (00h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_X_STR_FT[7:0] | Self-test response for gyro X-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps. |

18.2 IMEM_SRAM_REG_1

| Name: IMEM_SRAM_REG_1 Address: 01 (01h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_X_STR_FT[15:8] | Self-test response for gyro X-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps. |

18.3 IMEM_SRAM_REG_2

| Name: IMEM_SRAM_REG_2 Address: 02 (02h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Y_STR_FT[7:0] | Self-test response for gyro Y-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps. |

18.4 IMEM_SRAM_REG_3

| Name: IMEM_SRAM_REG_3 Address: 03 (03h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Y_STR_FT[15:8] | Self-test response for gyro Y-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps. |

18.5 IMEM_SRAM_REG_4

| Name: IMEM_SRAM_REG_4 Address: 04 (04h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Z_STR_FT[7:0] | Self-test response for gyro Z-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps. |

18.6 IMEM_SRAM_REG_5

| Name: IMEM_SRAM_REG_5 Address: 05 (05h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Z_STR_FT[15:8] | Self-test response for gyro Z-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps. |

18.7 IMEM_SRAM_REG_6

| Name: IMEM_SRAM_REG_6 Address: 06 (06h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_X_CMOS_GAIN_FT[7:0] | Gyro X-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps. |

18.8 IMEM_SRAM_REG_7

| Name: IMEM_SRAM_REG_7 Address: 07 (07h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------------|---|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:0 | GYRO_X_CMOS_GAIN_FT[11:8] | Gyro X-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps. |

18.9 IMEM_SRAM_REG_8

| Name: IMEM_SRAM_REG_8 Address: 08 (08h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Y_CMOS_GAIN_FT[7:0] | Gyro Y-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps. |

18.10 IMEM_SRAM_REG_9

| Name: IMEM_SRAM_REG_9 Address: 09 (09h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------------|---|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:0 | GYRO_Y_CMOS_GAIN_FT [11:8] | Gyro Y-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps. |

18.11 IMEM_SRAM_REG_10

| Name: IMEM_SRAM_REG_10 Address: 10 (0Ah) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Z_CMOS_GAIN_FT[7:0] | Gyro Z-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps. |

18.12 IMEM_SRAM_REG_11

| Name: IMEM_SRAM_REG_11 Address: 11 (0Bh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------------------------|---|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:0 | GYRO_Z_CMOS_GAIN_FT [11:8] | Gyro Z-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps. |

18.13 IMEM_SRAM_REG_56

| Name: IMEM_SRAM_REG_56 Address: 56 (38h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7 | ST_AVG_TIME[0] | Averaging time used to perform self-test (ST_AVG_TIME[2:1] in IMEM_SRAM_REG_57) 000: 10ms 001: 20ms 010: 40ms 011: 80ms 100: 160ms 101: 320ms Rest: Reserved |
| 6:3 | - | Reserved |
| 2 | ST_GYRO_EN | 1: Enable gyro self-test operation |
| 1 | ST_ACCEL_EN | 1: Enable accel self-test operation |
| 0 | STC_INIT_EN | 1: Initializes self-test parameters |

18.14 IMEM_SRAM_REG_57

| Name: IMEM_SRAM_REG_57 Address: 57 (39h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------------|--|
| BIT | NAME | FUNCTION |
| 7:5 | ST_GYRO_LIMIT | Tolerance between factory trim and gyro self-test response 000: 5% 001: 10% 010: 15% 011: 20% 100: 25% 101: 30% 110: 40% 111: 50% |
| 4:2 | ST_ACCEL_LIMIT | Tolerance between factory trim and accel self-test response 000: 5% 001: 10% 010: 15% 011: 20% 100: 25% 101: 30% 110: 40% 111: 50% |

| | | |
|-----|------------------|--|
| 1:0 | ST_AVG_TIME[2:1] | <p>Averaging time used to perform self-test (ST_AVG_TIME[0] in IMEM_SRAM_REG_56)</p> <p>000: 10ms 001: 20ms 010: 40ms 011: 80ms 100: 160ms 101: 320ms Rest: Reserved</p> |
|-----|------------------|--|

18.15 IMEM_SRAM_REG_64

| <p>Name: IMEM_SRAM_REG_64 Address: 64 (40h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK</p> | | |
|---|-------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | ST_DEBUG_EN | Debug capability of self-test feature. Must be set to 0 whenever self-test is requested. |

18.16 IMEM_SRAM_REG_68

| <p>Name: IMEM_SRAM_REG_68 Address: 68 (44h) Serial IF: R Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK</p> | | |
|---|------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | ST_STATUS | <p>Self-test status (gyro or accel)</p> <p>00: Done 01: In Progress 10: Error 11: Reserved</p> |
| 5 | GZ_ST_PASS | 1: Gyro Z-axis self-test passed |
| 4 | GY_ST_PASS | 1: Gyro Y-axis self-test passed |
| 3 | GX_ST_PASS | 1: Gyro X-axis self-test passed |
| 2 | AZ_ST_PASS | 1: Accel Z-axis self-test passed |
| 1 | AY_ST_PASS | 1: Accel Y-axis self-test passed |
| 0 | AX_ST_PASS | 1: Accel X-axis self-test passed |

18.17 IMEM_SRAM_REG_92

| Name: IMEM_SRAM_REG_92 Address: 92 (5Ch) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|---------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | QUAT_RESET_EN | Set 1 to force reset 3-axis quaternion when next tilt reset is done. This is applicable only if TILT_RESET_EN is also set to 1. Range: [0 – 1] Default: 0 |

18.18 IMEM_SRAM_REG_96

| Name: IMEM_SRAM_REG_96 Address: 96 (60h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GX[7:0] | Gyro measurements for X-axis in s32.16 for gyro self-test |

18.19 IMEM_SRAM_REG_97

| Name: IMEM_SRAM_REG_97 Address: 97 (61h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GX[15:8] | Gyro measurements for X-axis in s32.16 for gyro self-test |

18.20 IMEM_SRAM_REG_98

| Name: IMEM_SRAM_REG_98 Address: 98 (62h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|--------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GX[23:16] | Gyro measurements for X-axis in s32.16 for gyro self-test |

18.21 IMEM_SRAM_REG_99

| Name: IMEM_SRAM_REG_99 | | |
|---|--------------------|---|
| Address: 99 (63h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GX[31:24] | Gyro measurements for X-axis in s32.16 for gyro self-test |

18.22 IMEM_SRAM_REG_100

| Name: IMEM_SRAM_REG_100 | | |
|---|------------------|---|
| Address: 100 (64h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GY[7:0] | Gyro measurements for Y-axis in s32.16 for gyro self-test |

18.23 IMEM_SRAM_REG_101

| Name: IMEM_SRAM_REG_101 | | |
|---|-------------------|---|
| Address: 101 (65h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GY[15:8] | Gyro measurements for Y-axis in s32.16 for gyro self-test |

18.24 IMEM_SRAM_REG_102

| Name: IMEM_SRAM_REG_102 | | |
|---|--------------------|---|
| Address: 102 (66h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GY[23:16] | Gyro measurements for Y-axis in s32.16 for gyro self-test |

18.25 IMEM_SRAM_REG_103

| Name: IMEM_SRAM_REG_103 | | |
|---|--------------------|---|
| Address: 103 (67h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GY[31:24] | Gyro measurements for Y-axis in s32.16 for gyro self-test |

18.26 IMEM_SRAM_REG_104

| Name: IMEM_SRAM_REG_104 | | |
|---|------------------|---|
| Address: 104 (68h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GZ[7:0] | Gyro measurements for Z-axis in s32.16 for gyro self-test |

18.27 IMEM_SRAM_REG_105

| Name: IMEM_SRAM_REG_105 | | |
|---|-------------------|---|
| Address: 105 (69h) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GZ[15:8] | Gyro measurements for Z-axis in s32.16 for gyro self-test |

18.28 IMEM_SRAM_REG_106

| Name: IMEM_SRAM_REG_106 | | |
|---|--------------------|---|
| Address: 106 (6Ah) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GZ[23:16] | Gyro measurements for Z-axis in s32.16 for gyro self-test |

18.29 IMEM_SRAM_REG_107

| Name: IMEM_SRAM_REG_107 | | |
|---|--------------------|---|
| Address: 107 (6Bh) | | |
| Serial IF: R/W | | |
| Reset value: Random value after reset until host runs EDMP_INIT procedure | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | STC_GAIN_GZ[31:24] | Gyro measurements for Z-axis in s32.16 for gyro self-test |

18.30 IMEM_SRAM_REG_136

| Name: IMEM_SRAM_REG_136 Address: 136 (88h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DURATION_BUF1[7:0] | Duration of the freefall in number of samples. Filled in alternatively with FF_DURATION_BUF2. Unit: Number of samples. Freefall duration in seconds is FF_DURATION_BUF1 / ACCEL_ODR (in Hz) |

18.31 IMEM_SRAM_REG_137

| Name: IMEM_SRAM_REG_137 Address: 137 (89h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DURATION_BUF1[15:8] | Duration of the freefall in number of samples. Filled in alternatively with FF_DURATION_BUF2. Unit: Number of samples. Freefall duration in seconds is FF_DURATION_BUF1 / ACCEL_ODR (in Hz) |

18.32 IMEM_SRAM_REG_138

| Name: IMEM_SRAM_REG_138 Address: 138 (8Ah) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DURATION_BUF2[7:0] | Duration of the freefall in number of samples. Filled in alternatively with FF_DURATION_BUF1. Unit: Number of samples. Freefall duration in seconds is FF_DURATION_BUF2 / ACCEL_ODR (in Hz) |

18.33 IMEM_SRAM_REG_139

| Name: IMEM_SRAM_REG_139 Address: 139 (8Bh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DURATION_BUF2[15:8] | Duration of the freefall in number of samples. Filled in alternatively with FF_DURATION_BUF1. Unit: Number of samples. Freefall duration in seconds is FF_DURATION_BUF2 / ACCEL_ODR (in Hz) |

18.34 IMEM_SRAM_REG_141

| Name: IMEM_SRAM_REG_141 Address: 141 (8Dh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|---------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_NUM | Type of the last reported TAP event: 0: no tap, 1: single tap, 2: double tap |

18.35 IMEM_SRAM_REG_142

| Name: IMEM_SRAM_REG_142 Address: 142 (8Eh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_AXIS | Indicates the axis of the tap in the device frame 0: AX, 1: AY, 2: AZ |

18.36 IMEM_SRAM_REG_143

| Name: IMEM_SRAM_REG_143 Address: 143 (8Fh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|---------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_DIR | Indicates the direction of the tap in the device frame 0: Positive, 1: Negative |

18.37 IMEM_SRAM_REG_144

| Name: IMEM_SRAM_REG_144 Address: 144 (90h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | DOUBLE_TAP_TIMING | Indicate in case of double tap, the sample count between the 2 detected pulses In case of double tap, indicates the sample count between the two detected pulses. Double tap timing in seconds is DOUBLE_TAP_TIMING / ACCEL_ODR (in Hz). |

18.38 IMEM_SRAM_REG_146

| Name: IMEM_SRAM_REG_146 Address: 146 (92h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|---------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TILT_RESET_EN | Set 1 to reset tilt prior to any further tilt processing on next sensor data. Range: [0 - 1] Default: 0 |

18.39 IMEM_SRAM_REG_154

| Name: IMEM_SRAM_REG_154 Address: 154 (9Ah) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CNT_BUF1[7:0] | Number of steps done since the last init of the pedometer feature. Filled in alternatively with PED_STEP_CNT_BUF2. Unit: number of steps |

18.40 IMEM_SRAM_REG_155

| Name: IMEM_SRAM_REG_155 Address: 155 (9Bh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CNT_BUF1[15:8] | Number of steps done since the last init of the pedometer feature. Filled in alternatively with PED_STEP_CNT_BUF2. Unit: number of steps |

18.41 IMEM_SRAM_REG_156

| Name: IMEM_SRAM_REG_156 Address: 156 (9Ch) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CNT_BUF2[7:0] | Number of steps done since the last init of the pedometer feature. Filled in alternatively with PED_STEP_CNT_BUF1. Unit: number of steps |

18.42 IMEM_SRAM_REG_157

| Name: IMEM_SRAM_REG_157 Address: 157 (9Dh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CNT_BUF2[15:8]] | Number of steps done since the last init of the pedometer feature. Filled in alternatively with PED_STEP_CNT_BUF1. Unit: number of steps |

18.43 IMEM_SRAM_REG_159

| Name: IMEM_SRAM_REG_159 Address: 159 (9Fh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CADENCE | Instant step cadence measured by the algorithm Unit: 4*number of samples between two consecutive steps. Cadency (step/s) = (ped_step_cadence / 4) / (pedometer_ODR). |

18.44 IMEM_SRAM_REG_160

| Name: IMEM_SRAM_REG_160 Address: 160 (A0h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | POWER_ACTIVITY_CLASS | Activity classification of step detected 00000000: Unknown 00000001: Walk 00000010: Run Others: Reserved |

18.45 IMEM_SRAM_REG_182

| Name: IMEM_SRAM_REG_182 Address: 182 (B6h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-----------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | ES_RAM_IMAGE_EN | Set 1 to load device specific RAM image for external sensor support, otherwise set 0 |

18.46 IMEM_SRAM_REG_185

| Name: IMEM_SRAM_REG_185 Address: 185 (B9h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | ES0_COMPASS_EN | Set 1 for compass support with es0, for other external sensors with es0, set 0 |

18.47 IMEM_SRAM_REG_186

| Name: IMEM_SRAM_REG_186 Address: 186 (BAh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|---------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | ES_POWER_MODE | Set 1 for possibility of power savings when APEX features utilization is minimal. Set 0 when APEX features utilization is at maximum. |

18.48 IMEM_SRAM_REG_196

| Name: IMEM_SRAM_REG_196 Address: 196 (C4h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | POWER_SAVE_TIME[7:0] | Time of inactivity after which eDMP goes into power save mode. Units: Time in sample number Range: [0 - 4294967295] Default: 6400 corresponding to 8s for ODR = 800Hz |

18.49 IMEM_SRAM_REG_197

| Name: IMEM_SRAM_REG_197 Address: 197 (C5h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | POWER_SAVE_TIME[15:8] | Time of inactivity after which eDMP goes into power save mode. Units: Time in sample number Range: [0 - 4294967295] Default: 6400 corresponding to 8s for ODR = 800Hz |

18.50 IMEM_SRAM_REG_198

| Name: IMEM_SRAM_REG_198 Address: 198 (C6h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | POWER_SAVE_TIME[23:16] | Time of inactivity after which eDMP goes into power save mode. Units: Time in sample number Range: [0 - 4294967295] Default: 6400 corresponding to 8s for ODR = 800Hz |

18.51 IMEM_SRAM_REG_199

| Name: IMEM_SRAM_REG_199 Address: 199 (C7h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | POWER_SAVE_TIME[31:24] | Time of inactivity after which eDMP goes into power save mode. Units: Time in sample number Range: [0 - 4294967295] Default: 6400 corresponding to 8s for ODR = 800Hz |

18.52 IMEM_SRAM_REG_288

| Name: IMEM_SRAM_REG_288 Address: 288 (120h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MIN_DURATION[7:0] | Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms) |

18.53 IMEM_SRAM_REG_289

| Name: IMEM_SRAM_REG_289 Address: 289 (121h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MIN_DURATION[15:8] | Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms) |

18.54 IMEM_SRAM_REG_290

| Name: IMEM_SRAM_REG_290 Address: 290 (122h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MIN_DURATION[23:16] | Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms) |

18.55 IMEM_SRAM_REG_291

| Name: IMEM_SRAM_REG_291 Address: 291 (123h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MIN_DURATION[31:24] | Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms) |

18.56 IMEM_SRAM_REG_292

| Name: IMEM_SRAM_REG_292 Address: 292 (124h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MAX_DURATION[7:0] | Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms) |

18.57 IMEM_SRAM_REG_293

| Name: IMEM_SRAM_REG_293 Address: 293 (125h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MAX_DURATION[15:8] | Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms) |

18.58 IMEM_SRAM_REG_294

| Name: IMEM_SRAM_REG_294 Address: 294 (126h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MAX_DURATION[23:16] | Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms) |

18.59 IMEM_SRAM_REG_295

| Name: IMEM_SRAM_REG_295 Address: 295 (127h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | FF_MAX_DURATION[31:24] | Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms) |

18.60 IMEM_SRAM_REG_296

| Name: IMEM_SRAM_REG_296 Address: 296 (128h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DEBOUNCE_DURATION [7:0] | Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s) |

18.61 IMEM_SRAM_REG_297

| Name: IMEM_SRAM_REG_297 Address: 297 (129h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DEBOUNCE_DURATION [15:8] | Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s) |

18.62 IMEM_SRAM_REG_298

| Name: IMEM_SRAM_REG_298 Address: 298 (12Ah) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DEBOUNCE_DURATION [23:16] | Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s) |

18.63 IMEM_SRAM_REG_299

| Name: IMEM_SRAM_REG_299 Address: 299 (12Bh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | FF_DEBOUNCE_DURATION [31:24] | Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s) |

18.64 IMEM_SRAM_REG_304

| Name: IMEM_SRAM_REG_304 Address: 304 (130h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | HIGHG_PEAK_TH[7:0] | Threshold for accel values above which high-g state is detected. Unit: g in q12 Range: [1024 - 32768] Default: 29696 |

18.65 IMEM_SRAM_REG_305

| Name: IMEM_SRAM_REG_305 Address: 305 (131h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | HIGHG_PEAK_TH[15:8] | Threshold for accel values above which high-g state is detected. Unit: g in q12 Range: [1024 - 32768] Default: 29696 |

18.66 IMEM_SRAM_REG_306

| Name: IMEM_SRAM_REG_306 Address: 306 (132h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | HIGHG_PEAK_TH_HYST[7:0] | Hysteresis value subtracted from the high-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 640 |

18.67 IMEM_SRAM_REG_307

| Name: IMEM_SRAM_REG_307 Address: 307 (133h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | HIGHG_PEAK_TH_HYST[15:8] | Hysteresis value subtracted from the high-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 640 |

18.68 IMEM_SRAM_REG_308

| Name: IMEM_SRAM_REG_308 Address: 308 (134h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | HIGHG_TIME_TH[7:0] | Threshold for accel values above which high-g state is detected. Unit: time in samples number Range: [1-300] Default: 1 (set for default ODR = 800 Hz, equivalent to 1.25 ms) |

18.69 IMEM_SRAM_REG_309

| Name: IMEM_SRAM_REG_309 Address: 309 (135h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | HIGHG_TIME_TH[15:8] | Threshold for accel values above which high-g state is detected. Unit: time in samples number Range: [1-300] Default: 1 (set for default ODR = 800 Hz, equivalent to 1.25 ms) |

18.70 IMEM_SRAM_REG_316

| Name: IMEM_SRAM_REG_316 Address: 316 (13Ch) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | LOWG_PEAK_TH[7:0] | Threshold for accel values below which low-g state is detected. Unit: g in q12 Range: [128 - 4096] Default: 2048 |

18.71 IMEM_SRAM_REG_317

| Name: IMEM_SRAM_REG_317 Address: 317 (13Dh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | LOWG_PEAK_TH[15:8] | Threshold for accel values below which low-g state is detected. Unit: g in q12 Range: [128 - 4096] Default: 2048 |

18.72 IMEM_SRAM_REG_318

| Name: IMEM_SRAM_REG_318 Address: 318 (13Eh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | LOWG_PEAK_TH_HYST[7:0] | Hysteresis value added to the low-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 128 |

18.73 IMEM_SRAM_REG_319

| Name: IMEM_SRAM_REG_319 Address: 319 (13Fh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | LOWG_PEAK_TH_HYST[15:8] | Hysteresis value added to the low-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 128 |

18.74 IMEM_SRAM_REG_320

| Name: IMEM_SRAM_REG_320 Address: 320 (140h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | LOWG_TIME_TH[7:0] | Number of samples required to enter low-g state. Unit: time in samples number Range: [1 - 300] Default: 13 (set for default ODR = 800 Hz, equivalent to 16 ms) |

18.75 IMEM_SRAM_REG_321

| Name: IMEM_SRAM_REG_321 Address: 321 (141h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | LOWG_TIME_TH[15:8] | Number of samples required to enter low-g state. Unit: time in samples number Range: [1 - 300] Default: 13 (set for default ODR = 800 Hz, equivalent to 16 ms) |

18.76 IMEM_SRAM_REG_392

| Name: IMEM_SRAM_REG_392 Address: 392 (188h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TILT_WAIT_TIME[7:0] | Minimum duration for which the device should be tilted before signaling event. Unit: time in sample number Range: [0 - 65536] Default: 200 for ODR = 50Hz, 100 for ODR = 25Hz |

18.77 IMEM_SRAM_REG_393

| Name: IMEM_SRAM_REG_393 Address: 393 (189h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TILT_WAIT_TIME[15:8] | Minimum duration for which the device should be tilted before signaling event. Unit: time in sample number Range: [0 - 65536] Default: 200 for ODR = 50Hz, 100 for ODR = 25Hz |

18.78 IMEM_SRAM_REG_400

| Name: IMEM_SRAM_REG_400 Address: 400 (190h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_TMAX[7:0] | Size of the analysis window to detect tap events (single-tap or double-tap) unit: time in sample number range: [49 – 496] default: 99 (set for default ODR = 200Hz, equivalent to. 0.5s) |

18.79 IMEM_SRAM_REG_401

| Name: IMEM_SRAM_REG_401 Address: 401 (191h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_TMAX[15:8] | Size of the analysis window to detect tap events (single-tap or double-tap) unit: time in sample number range: [49 – 496] default: 99 (set for default ODR = 200Hz, equivalent to. 0.5s) |

18.80 IMEM_SRAM_REG_402

| Name: IMEM_SRAM_REG_402 Address: 402 (192h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_TMIN | Single tap window, sub-windows within Tmax to detect single-tap event. Unit: time in sample number Range: [24 – 184] Default: 33 (set for default ODR = 200Hz, equivalent to. 0.165s) |

18.81 IMEM_SRAM_REG_403

| Name: IMEM_SRAM_REG_403 Address: 403 (193h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_MIN_JERK | The minimal value of jerk to be considered as a tap candidate. Unit: g in q6 Range: [0 - 64] Default: 17 |

18.82 IMEM_SRAM_REG_404

| Name: IMEM_SRAM_REG_404 Address: 404 (194h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_SMUDGE_REJECT_THR | Max acceptable number of samples (jerk value) over TAP_MAX_PEAK_TOL during the Tmin window. Over this value, Tap event is rejected unit: time in number of samples range: [13 – 92] Default: 17 (set for default ODR = 200Hz, equivalent to 0.085s) |

18.83 IMEM_SRAM_REG_405

| Name: IMEM_SRAM_REG_405 Address: 405 (195h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_MAX_PEAK_TOL | Maximum peak tolerance is the percentage of pulse amplitude to get the smudge threshold for rejection. Range: [1 (12.5%) 2 (25.0%) 3 (37.5%) 4 (50.0 %)] Default: 2 Default: 17 |

18.84 IMEM_SRAM_REG_406

| Name: IMEM_SRAM_REG_406 Address: 406 (196h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------|--|
| BIT | NAME | FUNCTION |
| 7:0 | TAP_TAVG | Energy measurement window size to determine the tap axis associated with the 1st tap. Unit: time in sample number Range: [1 ; 2 ; 4 ; 8] Default: 8 |

18.85 IMEM_SRAM_REG_540

| Name: IMEM_SRAM_REG_540 Address: 540 (21Ch) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_TIME_OUT[7:0] | Defines the duration after wake event to report sleep event no matter if position changes or not. Unit: time in ms (millisecond) Range: [100 - 10000] Default: 640 (equivalent to 0.64s) |

18.86 IMEM_SRAM_REG_541

| Name: IMEM_SRAM_REG_541 Address: 541 (21Dh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_TIME_OUT[15:8] | Defines the duration after wake event to report sleep event no matter if position changes or not. Unit: time in ms (millisecond) Range: [100 - 10000] Default: 640 (equivalent to 0.64s) |

18.87 IMEM_SRAM_REG_542

| Name: IMEM_SRAM_REG_542 Address: 542 (21Eh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_TIME_OUT[23:16] | Defines the duration after wake event to report sleep event no matter if position changes or not. Unit: time in ms (millisecond) Range: [100 - 10000] Default: 640 (equivalent to 0.64s) |

18.88 IMEM_SRAM_REG_543

| Name: IMEM_SRAM_REG_543 Address: 543 (21Fh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_TIME_OUT[31:24] | Defines the duration after wake event to report sleep event no matter if position changes or not. Unit: time in ms (millisecond) Range: [100 - 10000] Default: 640 (equivalent to 0.64s) |

18.89 IMEM_SRAM_REG_544

| Name: IMEM_SRAM_REG_544 Address: 544 (220h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_GESTURE_DELAY[7:0] | Defines the minimal duration of sleep position before trigger the sleep event. Unit: time in ms (millisecond) Range: [0 - 256] Default: 96 (equivalent to 0.096s) |

18.90 IMEM_SRAM_REG_545

| Name: IMEM_SRAM_REG_545 Address: 545 (221h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_GESTURE_DELAY[15:8] | Defines the minimal duration of sleep position before trigger the sleep event. Unit: time in ms (millisecond) Range: [0 - 256] Default: 96 (equivalent to 0.096s) |

18.91 IMEM_SRAM_REG_546

| Name: IMEM_SRAM_REG_546 Address: 546 (222h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_GESTURE_DELAY[23:16] | Defines the minimal duration of sleep position before trigger the sleep event. Unit: time in ms (millisecond) Range: [0 - 256] Default: 96 (equivalent to 0.096s) |

18.92 IMEM_SRAM_REG_547

| Name: IMEM_SRAM_REG_547 Address: 547 (223h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_SLEEP_GESTURE_DELAY[31:24] | Defines the minimal duration of sleep position before trigger the sleep event. Unit: time in ms (millisecond) Range: [0 - 256] Default: 96 (equivalent to 0.096s) |

18.93 IMEM_SRAM_REG_548

| Name: IMEM_SRAM_REG_548 Address: 548 (224h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOUNTING_MATRIX [7:0] | Mounting matrix to rotate data from chip frame to device frame. Range: 3 lower bits only are used [b2 b1 b0]: - b2 = 1 swap X and Y - b1 = 1 flip X sign - b0 = 1 flip Y sign Default: 0 (device frame aligned with android frame) |

18.94 IMEM_SRAM_REG_549

| Name: IMEM_SRAM_REG_549 Address: 549 (225h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOUNTING_MATRIX [15:8] | Mounting matrix to rotate data from chip frame to device frame. Range: 3 lower bits only are used [b2 b1 b0]: - b2 = 1 swap X and Y - b1 = 1 flip X sign - b0 = 1 flip Y sign Default: 0 (device frame aligned with android frame) |

18.95 IMEM_SRAM_REG_550

| Name: IMEM_SRAM_REG_550 Address: 550 (226h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOUNTING_MATRIX [23:16] | Mounting matrix to rotate data from chip frame to device frame. Range: 3 lower bits only are used [b2 b1 b0]: - b2 = 1 swap X and Y - b1 = 1 flip X sign - b0 = 1 flip Y sign Default: 0 (device frame aligned with android frame) |

18.96 IMEM_SRAM_REG_551

| Name: IMEM_SRAM_REG_551 Address: 551 (227h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOUNTING_MATRIX [31:24] | Mounting matrix to rotate data from chip frame to device frame. Range: 3 lower bits only are used [b2 b1 b0]: - b2 = 1 swap X and Y - b1 = 1 flip X sign - b0 = 1 flip Y sign Default: 0 (device frame aligned with android frame) |

18.97 IMEM_SRAM_REG_556

| Name: IMEM_SRAM_REG_556 Address: 556 (22Ch) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GRAVITY_FILTER_GAIN[7:0] | Gain used to filter the accelerometer to obtain an estimation of the gravity (low-pass filter), defined as: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32), and 100Hz. Range: [2-16] Default: 6 for ODR = 50Hz, 8 for ODR = 25Hz |

18.98 IMEM_SRAM_REG_557

| Name: IMEM_SRAM_REG_557 Address: 557 (22Dh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GRAVITY_FILTER_GAIN[15:8] | Gain used to filter the accelerometer to obtain an estimation of the gravity (low-pass filter), defined as: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32), and 100Hz. Range: [2-16] Default: 6 for ODR = 50Hz, 8 for ODR = 25Hz |

18.99 IMEM_SRAM_REG_558

| Name: IMEM_SRAM_REG_558 Address: 558 (22Eh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GRAVITY_FILTER_GAIN[23:16] | Gain used to filter the accelerometer to obtain an estimation of the gravity (low-pass filter), defined as: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32), and 100Hz. Range: [2-16] Default: 6 for ODR = 50Hz, 8 for ODR = 25Hz |

18.100 IMEM_SRAM_REG_559

| Name: IMEM_SRAM_REG_559 Address: 559 (22Fh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GRAVITY_FILTER_GAIN[31:24] | Gain used to filter the accelerometer to obtain an estimation of the gravity (low-pass filter), defined as: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32), and 100Hz. Range: [2-16] Default: 6 for ODR = 50Hz, 8 for ODR = 25Hz |

18.101 IMEM_SRAM_REG_560

| Name: IMEM_SRAM_REG_560 Address: 560 (230h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_ANGLE_COSINE[7:0] | Set the minimal angle that needed to be applied to device to detect R2W Unit: fixed point value q30 of cosine of the angle Range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Default: 1046221864, corresponding to an angle of 13 degrees |

18.102 IMEM_SRAM_REG_561

| Name: IMEM_SRAM_REG_561 Address: 561 (231h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_ANGLE_COSINE[15:8] | Set the minimal angle that needed to be applied to device to detect R2W Unit: fixed point value q30 of cosine of the angle Range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Default: 1046221864, corresponding to an angle of 13 degrees |

18.103 IMEM_SRAM_REG_562

| Name: IMEM_SRAM_REG_562 Address: 562 (232h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_ANGLE_COSINE[23:16] | Set the minimal angle that needed to be applied to device to detect R2W Unit: fixed point value q30 of cosine of the angle Range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Default: 1046221864, corresponding to an angle of 13 degrees |

18.104 IMEM_SRAM_REG_563

| Name: IMEM_SRAM_REG_563 Address: 563 (233h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_ANGLE_COSINE[31:24] | Set the minimal angle that needed to be applied to device to detect R2W Unit: fixed point value q30 of cosine of the angle Range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Default: 1046221864, corresponding to an angle of 13 degrees |

18.105 IMEM_SRAM_REG_564

| Name: IMEM_SRAM_REG_564 Address: 564 (234h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIMER_FAST[7:0] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.106 IMEM_SRAM_REG_565

| Name: IMEM_SRAM_REG_565 Address: 565 (235h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_FAST[15:8] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.107 IMEM_SRAM_REG_566

| Name: IMEM_SRAM_REG_566 Address: 566 (236h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_FAST[23:16] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.108 IMEM_SRAM_REG_567

| Name: IMEM_SRAM_REG_567 Address: 567 (237h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_FAST[31:24] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.109 IMEM_SRAM_REG_568

| Name: IMEM_SRAM_REG_568 Address: 568 (238h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_SLOW[7:0] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.110 IMEM_SRAM_REG_569

| Name: IMEM_SRAM_REG_569 Address: 569 (239h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_SLOW[15:8] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.111 IMEM_SRAM_REG_570

| Name: IMEM_SRAM_REG_570 Address: 570 (23Ah) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_SLOW[23:16] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.112 IMEM_SRAM_REG_571

| Name: IMEM_SRAM_REG_571 Address: 571 (23Bh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_THR_TIME R_SLOW[31:24] | Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240 |

18.113 IMEM_SRAM_REG_572

| Name: IMEM_SRAM_REG_572 Address: 572 (23Ch) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_PREV_GRA VITY_TIMEOUT[7:0] | Time delay to update internal value of previous gravity when no motion is detected. Longer time enables detection motion during slower gesture. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 300 |

18.114 IMEM_SRAM_REG_573

| Name: IMEM_SRAM_REG_573 Address: 573 (23Dh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_PREV_GRA VITY_TIMEOUT[15:8] | Time delay to update internal value of previous gravity when no motion is detected. Longer time enables detection motion during slower gesture. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 300 |

18.115 IMEM_SRAM_REG_574

| Name: IMEM_SRAM_REG_574 Address: 574 (23Eh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_PREV_GRAVITY_TIMEOUT[23:16] | Time delay to update internal value of previous gravity when no motion is detected. Longer time enables detection motion during slower gesture. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 300 |

18.116 IMEM_SRAM_REG_575

| Name: IMEM_SRAM_REG_575 Address: 575 (23Fh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_MOTION_PREV_GRAVITY_TIMEOUT[31:24] | Time delay to update internal value of previous gravity when no motion is detected. Longer time enables detection motion during slower gesture. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 300 |

18.117 IMEM_SRAM_REG_576

| Name: IMEM_SRAM_REG_576 Address: 576 (240h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_MOTION_TIMER[7:0] | Time delay to update the current gravity estimator when no motion is detected. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 480 |

18.118 IMEM_SRAM_REG_577

| Name: IMEM_SRAM_REG_577 Address: 577 (241h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_MOTION_TIMER[15:8] | Time delay to update the current gravity estimator when no motion is detected. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 480 |

18.119 IMEM_SRAM_REG_578

| Name: IMEM_SRAM_REG_578 Address: 578 (242h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_MOTION_TIMER[23:16] | Time delay to update the current gravity estimator when no motion is detected. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 480 |

18.120 IMEM_SRAM_REG_579

| Name: IMEM_SRAM_REG_579 Address: 579 (243h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_MOTION_TIMER[31:24] | Time delay to update the current gravity estimator when no motion is detected. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 480 |

18.121 IMEM_SRAM_REG_580

| Name: IMEM_SRAM_REG_580 Address: 580 (244h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_TIME_OUT[7:0] | Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [1000 - 10000] Default: 2600 |

18.122 IMEM_SRAM_REG_581

| Name: IMEM_SRAM_REG_581 Address: 581 (245h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_TIME_OUT[15:8] | Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [1000 - 10000] Default: 2600 |

18.123 IMEM_SRAM_REG_582

| Name: IMEM_SRAM_REG_582 Address: 582 (246h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_TIME_OUT[23:16] | Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [1000 - 10000] Default: 2600 |

18.124 IMEM_SRAM_REG_583

| Name: IMEM_SRAM_REG_583 Address: 583 (247h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_LAST_GRAVITY_TIME_OUT[31:24] | Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [1000 - 10000] Default: 2600 |

18.125 IMEM_SRAM_REG_584

| Name: IMEM_SRAM_REG_584 Address: 584 (248h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GESTURE_VALIDITY_TIMEOUT[7:0] | If gesture is not completed in this timeout limit, gesture is invalid. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 240 |

18.126 IMEM_SRAM_REG_585

| Name: IMEM_SRAM_REG_585 Address: 585 (249h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GESTURE_VALIDITY_TIMEOUT[15:8] | If gesture is not completed in this timeout limit, gesture is invalid. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 240 |

18.127 IMEM_SRAM_REG_586

| Name: IMEM_SRAM_REG_586 Address: 586 (24Ah) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GESTURE_VALIDITY_TIMEOUT[23:16] | If gesture is not completed in this timeout limit, gesture is invalid. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 240 |

18.128 IMEM_SRAM_REG_587

| Name: IMEM_SRAM_REG_587 Address: 587 (24Bh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | R2W_GESTURE_VALIDITY_TIMEOUT[31:24] | If gesture is not completed in this timeout limit, gesture is invalid. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 240 |

18.129 IMEM_SRAM_REG_988

| Name: IMEM_SRAM_REG_988 Address: 988 (3DCh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CNT_TH[7:0] | Minimum number of steps that must be detected before step count is incremented. Low values reduce latency but increase false positives. High values increase step count accuracy but increase latency Unit: Number of steps Range: [0-15] Default: 5 |

18.130 IMEM_SRAM_REG_989

| Name: IMEM_SRAM_REG_989 Address: 989 (3DDh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_CNT_TH[15:8] | Minimum number of steps that must be detected before step count is incremented. Low values reduce latency but increase false positives. High values increase step count accuracy but increase latency Unit: Number of steps Range: [0-15] Default: 5 |

18.131 IMEM_SRAM_REG_990

| Name: IMEM_SRAM_REG_990 Address: 990 (3DEh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_DET_TH[7:0] | Minimum number of steps that must be detected before step event is signaled. Low values reduce latency but increase false positives. High values increase step event validity but increase latency. Unit: number of steps Range: [0-7] Default: 2 |

18.132 IMEM_SRAM_REG_991

| Name: IMEM_SRAM_REG_991 Address: 991 (3DFh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_STEP_DET_TH[15:8] | Minimum number of steps that must be detected before step event is signaled. Low values reduce latency but increase false positives. High values increase step event validity but increase latency. Unit: number of steps Range: [0-7] Default: 2 |

18.133 IMEM_SRAM_REG_994

| Name: IMEM_SRAM_REG_994 Address: 994 (3E2h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | PED_SB_TIMER_TH[7:0] | While in the step buffer state, the step buffer count resets to 0 if a new step isn't detected for this amount of time (user is considered to have "stopped walking"). Unit: time in samples number Range: [0 - 225] Default: 150 for ODR = 50Hz |

18.134 IMEM_SRAM_REG_995

| Name: IMEM_SRAM_REG_995 Address: 995 (3E3h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-----------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | PED_SB_TIMER_TH[15:8] | While in the step buffer state, the step buffer count resets to 0 if a new step isn't detected for this amount of time (user is considered to have "stopped walking"). Unit: time in samples number Range: [0 - 225] Default: 150 for ODR = 50Hz |

18.135 IMEM_SRAM_REG_1000

| Name: IMEM_SRAM_REG_1000 Address: 1000 (3E8h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|------------------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | PED_LOW_EN_AMP_TH[7:0] | Threshold to select a valid step. Used to increase step detection for slow walk use case only. Unit: g in q25. Range: [1006632 - 3523215] Default: 2684354 |

18.136 IMEM_SRAM_REG_1001

Name: IMEM_SRAM_REG_1001
 Address: 1001 (3E9h)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|-------------------------|---|
| 7:0 | PED_LOW_EN_AMP_TH[15:8] | Threshold to select a valid step. Used to increase step detection for slow walk use case only. Unit: g in q25. Range: [1006632 - 3523215] Default: 2684354 |

18.137 IMEM_SRAM_REG_1002

Name: IMEM_SRAM_REG_1002
 Address: 1002 (3EAh)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|--------------------------|---|
| 7:0 | PED_LOW_EN_AMP_TH[23:16] | Threshold to select a valid step. Used to increase step detection for slow walk use case only. Unit: g in q25. Range: [1006632 - 3523215] Default: 2684354 |

18.138 IMEM_SRAM_REG_1003

Name: IMEM_SRAM_REG_1003
 Address: 1003 (3EBh)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|--------------------------|---|
| 7:0 | PED_LOW_EN_AMP_TH[31:24] | Threshold to select a valid step. Used to increase step detection for slow walk use case only. Unit: g in q25. Range: [1006632 - 3523215] Default: 2684354 |

18.139 IMEM_SRAM_REG_1004

Name: IMEM_SRAM_REG_1004
 Address: 1004 (3ECh)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|----------------------|--|
| 7:0 | PED_SENSITIVITY_MODE | Pedometer sensitivity mode. Slow walk mode improves slow walk detection (<1 Hz) but the number of false positives may increase Range: 0: Normal 1: Slow walk Default: 0 |

18.140 IMEM_SRAM_REG_1008

Name: IMEM_SRAM_REG_1008
 Address: 1008 (3F0h)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|-----------------|--|
| 7:0 | PED_AMP_TH[7:0] | Threshold of step detection sensitivity. Low values increase detection sensitivity; reduce miss-detection. High values reduce detection sensitivity; reduce false-positive. Unit: g in q25. Range: [1006632 - 3019898] Default: 2080374 |

18.141 IMEM_SRAM_REG_1009

Name: IMEM_SRAM_REG_1009
 Address: 1009 (3F1h)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|------------------|--|
| 7:0 | PED_AMP_TH[15:8] | Threshold of step detection sensitivity. Low values increase detection sensitivity; reduce miss-detection. High values reduce detection sensitivity; reduce false-positive. Unit: g in q25. Range: [1006632 - 3019898] Default: 2080374 |

18.142 IMEM_SRAM_REG_1010

| Name: IMEM_SRAM_REG_1010 Address: 1010 (3F2h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_AMP_TH[23:16] | Threshold of step detection sensitivity. Low values increase detection sensitivity: reduce miss-detection. High values reduce detection sensitivity: reduce false-positive. Unit: g in q25. Range: [1006632 - 3019898] Default: 2080374 |

18.143 IMEM_SRAM_REG_1011

| Name: IMEM_SRAM_REG_1011 Address: 1011 (3F3h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_AMP_TH[31:24] | Threshold of step detection sensitivity. Low values increase detection sensitivity: reduce miss-detection. High values reduce detection sensitivity: reduce false-positive. Unit: g in q25. Range: [1006632 - 3019898] Default: 2080374 |

18.144 IMEM_SRAM_REG_1016

| Name: IMEM_SRAM_REG_1016 Address: 1016 (3F8h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|-------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_HI_EN_TH[7:0] | Threshold to classify acceleration signal as motion not due to steps High values improve vibration rejection. Low values improve detection. Unit: g in q25. Range: [2949120 - 5210112] Default: 3506176 |

18.145 IMEM_SRAM_REG_1017

| Name: IMEM_SRAM_REG_1017 Address: 1017 (3F9h) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|--------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_HI_EN_TH[15:8] | Threshold to classify acceleration signal as motion not due to steps High values improve vibration rejection. Low values improve detection. Unit: g in q25. Range: [2949120 - 5210112] Default: 3506176 |

18.146 IMEM_SRAM_REG_1018

| Name: IMEM_SRAM_REG_1018 Address: 1018 (3FAh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_HI_EN_TH[23:16] | Threshold to classify acceleration signal as motion not due to steps High values improve vibration rejection. Low values improve detection. Unit: g in q25. Range: [2949120 - 5210112] Default: 3506176 |

18.147 IMEM_SRAM_REG_1019

| Name: IMEM_SRAM_REG_1019 Address: 1019 (3FBh) Serial IF: R/W Reset value: Random value after reset until host runs EDMP_INIT procedure Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PED_HI_EN_TH[31:24] | Threshold to classify acceleration signal as motion not due to steps High values improve vibration rejection. Low values improve detection. Unit: g in q25. Range: [2949120 - 5210112] Default: 3506176 |

18.148 IMEM_SRAM_REG_1042

Name: IMEM_SRAM_REG_1042
 Address: 1042 (412h)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|-----------------|---|
| 7:0 | SMD_SENSITIVITY | Parameter to tune SMD algorithm robustness to rejection, ranging from 0 to 4 (values higher than 4 are reserved). Low values increase detection rate but increase false positives. High values reduce false positives but reduce detection rate (especially for transport use cases). Range: [0 - 4] Default: 0 |

18.149 IMEM_SRAM_REG_1168 TO IMEM_SRAM_REG_1203

Name: IMEM_SRAM_REG_1168 to IMEM_SRAM_REG_1203
 Address: 1168 to 1203 (490h to 4B3h)
 Serial IF: R/W
 Reset value: Random value after reset until host runs EDMP_INIT procedure
 Clock Domain: MCLK

| BIT | NAME | FUNCTION |
|-----|-------------------------------------|--|
| 7:0 | SOFT_IRON_SENSITIVITY_MATRIX[287:0] | Input 3x3 calibration matrix in q14 format applied to uncalibrated data. |

19 USER BANK IPREG_BAR REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_BAR. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

19.1 IPREG_BAR_REG_57

| Name: IPREG_BAR_REG_57 | | |
|------------------------|---------|---|
| Address: 57 (39h) | | |
| Serial IF: R/W | | |
| Reset value: 0x33 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | IO_OPT0 | Set this register field to 1 for optimal speed of IOs. IO_OPT1 must be also set to 1 if IO_OPT0 is set to 1. Can be changed on-the-fly. |
| 5 | IO_OPT1 | Set this register field to 1 for optimal speed of IOs. Can be changed on-the-fly. |
| 4:0 | - | Reserved |

19.2 IPREG_BAR_REG_58

| Name: IPREG_BAR_REG_58 Address: 58 (3Ah) Serial IF: R/W Reset value: 0xD9 Clock Domain: MCLK | | |
|--|---------------------------|---|
| BIT | NAME | FUNCTION |
| 7 | PADS_AP_SCLK_PUD_TRIM_D2A | Selects internal resistor pull direction for AP_SCLK pin (pin 13) 0: Down 1: Up Can be changed on-the-fly. |
| 6 | PADS_AP_SCLK_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for AP_SCLK pin (pin 13), depending on direction selected by bit 7. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 5 | - | Reserved |
| 4 | PADS_AP_CS_PUD_TRIM_D2A | Selects internal resistor pull direction for AP_CS pin (pin 12) 0: Down 1: Up Can be changed on-the-fly. |
| 3 | PADS_AP_CS_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for AP_CS pin (pin 12), depending on direction selected by bit 4. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 2:1 | - | Reserved |
| 0 | IO_OPT2 | Set this register field to 1 for optimal speed of IOs. IO_OPT1 must be also set to 1 if IO_OPT2 is set to 1 Can be changed on-the-fly. |

19.3 IPREG_BAR_REG_59

| Name: IPREG_BAR_REG_59 Address: 59 (3Bh) Serial IF: R/W Reset value: 0xB6 Clock Domain: MCLK | | |
|--|--------------------------|--|
| BIT | NAME | FUNCTION |
| 7 | PADS_PIN7_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for pin 7, depending on direction selected by bit 0 of register IPREG_BAR_REG_60 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 6 | - | Reserved |
| 5 | PADS_AP_SDO_PUD_TRIM_D2A | Selects internal resistor pull direction for AP_SDO pin (pin 1) 0: Down 1: Up Can be changed on-the-fly. |
| 4 | PADS_AP_SDO_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for AP_SDO pin (pin 1), depending on direction selected by bit 5. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 3 | - | Reserved |
| 2 | PADS_AP_SDI_PUD_TRIM_D2A | Selects internal resistor pull direction for AP_SDI pin (pin 14) 0: Down 1: Up Can be changed on-the-fly. |
| 1 | PADS_AP_SDI_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for AP_SDI pin (pin 14), depending on direction selected by bit 2. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 0 | - | Reserved |

19.4 IPREG_BAR_REG_60

| Name: IPREG_BAR_REG_60 Address: 60 (3Ch) Serial IF: R/W Reset value: 0x6D Clock Domain: MCLK | | |
|--|---|--|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | PADS_AUX1_SCLK_PUD_TRIM_D2A | Enables internal pull resistor to pull up or down for AUX1_SCLK pin (pin 3), depending on direction selected by bit 5. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 5 | PADS_AUX1_SCLK_PE_TRIM_D2A | Selects internal resistor pull direction for AUX1_SCLK pin (pin 3) 0: Down 1: Up Can be changed on-the-fly. |
| 4 | PADS_AUX_SCLK_TP2_FROM_PAD_DISABLE_TRIM_D2A | Set this bit to 1 if using I ² C master mode. Set it to 0 otherwise. |
| 3 | PADS_AUX1_CS_PUD_TRIM_D2A | Enables internal pull resistor to pull up or down for AUX1_CS pin (pin 10), depending on direction selected by bit 2. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 2 | PADS_AUX1_CS_PE_TRIM_D2A | Selects internal resistor pull direction for AUX1_CS pin (pin 10) 0: Down 1: Up Can be changed on-the-fly. |
| 1 | - | Reserved |
| 0 | PADS_PIN7_CS_PUD_TRIM_D2A | Selects internal resistor pull direction for pin 7 0: Down 1: Up Can be changed on-the-fly. |

19.5 IPREG_BAR_REG_61

| Name: IPREG_BAR_REG_61 Address: 61 (3Dh) Serial IF: R/W Reset value: 0xBB Clock Domain: MCLK | | |
|--|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7 | PADS_INT1_PUD_TRIM_D2A | Enables internal pull resistor to pull up or down for INT1 pin (pin 4), depending on direction selected by bit 6. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 6 | PADS_INT1_PE_TRIM_D2A | Selects internal resistor pull direction for INT1 pin (pin 4) 0: Down 1: Up Can be changed on-the-fly. |
| 5 | - | Reserved |
| 4 | PADS_AUX1_SDO_PUD_TRIM_D2A | Selects internal resistor pull direction for AUX1_SDO pin (pin 11) 0: Down 1: Up Can be changed on-the-fly. |
| 3 | PADS_AUX1_SDO_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for AUX1_SDO pin (pin 11), depending on direction selected by bit 4. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 2 | - | Reserved |
| 1 | PADS_AUX1_SDI_PUD_TRIM_D2A | Enables internal pull resistor to pull up or down for AUX1_SDI pin (pin 2), depending on direction selected by bit 0. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 0 | PADS_AUX1_SDI_PE_TRIM_D2A | Selects internal resistor pull direction for AUX1_SDI pin (pin 2) 0: Down 1: Up Can be changed on-the-fly. |

19.6 IPREG_BAR_REG_62

| Name: IPREG_BAR_REG_62 Address: 62 (3Eh) Serial IF: R/W Reset value: 0x06 Clock Domain: MCLK | | |
|--|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2 | PADS_INT2_PUD_TRIM_D2 A | Selects internal resistor pull direction for INT2 pin (pin 9) 0: Down 1: Up Can be changed on-the-fly. |
| 1 | PADS_INT2_PE_TRIM_D2A | Enables internal pull resistor to pull up or down for INT2 pin (pin 9), depending on direction selected by bit 2. 0: Not enabled 1: Enabled Can be changed on-the-fly. |
| 0 | - | Reserved |

20 USER BANK IPREG_TOP1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_TOP1. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

20.1 I2CM_COMMAND_0

| Name: I2CM_COMMAND_0 (I ² C master command buffer 0) Address: 06 (06h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|------------|---|
| BIT | NAME | FUNCTION |
| 7 | ENDFLAG_0 | Indicates if the current entry is the last I ² C master communication with the external slave device. |
| 6 | CH_SEL_0 | Specifies the channel number for I ² C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID "ID1" 1: Specify the other external sensor with device ID "ID2" "ID1" and "ID2" should be replaced by the actual device ID of the chosen external devices. |
| 5:4 | R_W_0 | I ² C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved |
| 3:0 | BURSTLEN_0 | Specifies the burst length of I ² C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111. |

20.2 I2CM_COMMAND_1

| Name: I2CM_COMMAND_1 (I ² C master command buffer 1) Address: 07 (07h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|------------|---|
| BIT | NAME | FUNCTION |
| 7 | ENDFLAG_1 | Indicates if the current entry is the last I ² C master communication with the external slave device. |
| 6 | CH_SEL_1 | Specifies the channel number for I ² C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID "ID1" 1: Specify the other external sensor with device ID "ID2" "ID1" and "ID2" should be replaced by the actual device ID of the chosen external devices. |
| 5:4 | R_W_1 | I ² C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved |
| 3:0 | BURSTLEN_1 | Specifies the burst length of I ² C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111. |

20.3 I2CM_COMMAND_2

| Name: I2CM_COMMAND_2 (I ² C master command buffer 2) Address: 08 (08h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|------------|---|
| BIT | NAME | FUNCTION |
| 7 | ENDFLAG_2 | Indicates if the current entry is the last I ² C master communication with the external slave device. |
| 6 | CH_SEL_2 | Specifies the channel number for I ² C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID "ID1" 1: Specify the other external sensor with device ID "ID2" "ID1" and "ID2" should be replaced by the actual device ID of the chosen external devices. |
| 5:4 | R_W_2 | I ² C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved |
| 3:0 | BURSTLEN_2 | Specifies the burst length of I ² C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111. |

20.4 I2CM_COMMAND_3

| Name: I2CM_COMMAND_3 (I ² C master command buffer 3) Address: 09 (09h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|------------|---|
| BIT | NAME | FUNCTION |
| 7 | ENDFLAG_3 | Indicates if the current entry is the last I ² C master communication with the external slave device. |
| 6 | CH_SEL_3 | Specifies the channel number for I ² C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID "ID1" 1: Specify the other external sensor with device ID "ID2" "ID1" and "ID2" should be replaced by the actual device ID of the chosen external devices. |
| 5:4 | R_W_3 | I ² C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved |
| 3:0 | BURSTLEN_3 | Specifies the burst length of I ² C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111. |

20.5 I2CM_DEV_PROFILE0

| Name: I2CM_DEV_PROFILE0 | | |
|-------------------------|--------------|--|
| Address: 14 (0Eh) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | RD_ADDRESS_0 | Specifies the read address for channel 0 I ² C master transaction |

20.6 I2CM_DEV_PROFILE1

| Name: I2CM_DEV_PROFILE1 | | |
|-------------------------|----------|--|
| Address: 15 (0Fh) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6:0 | DEV_ID_0 | Specifies the slave ID for channel 0 I ² C master transaction |

20.7 I2CM_DEV_PROFILE2

| Name: I2CM_DEV_PROFILE2 | | |
|-------------------------|--------------|--|
| Address: 16 (10h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | RD_ADDRESS_1 | Specifies the read address for channel 1 I ² C master transaction |

20.8 I2CM_DEV_PROFILE3

| Name: I2CM_DEV_PROFILE3 | | |
|-------------------------|----------|--|
| Address: 17 (11h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6:0 | DEV_ID_1 | Specifies the slave ID for channel 1 I ² C master transaction |

20.9 I2CM_CONTROL

| Name: I2CM_CONTROL | | |
|--------------------|-----------------|---|
| Address: 22 (16h) | | |
| Serial IF: RWS | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6 | I2CM_RESTART_EN | 0: No Restart is used 1: In an I2C register read transaction, the Restart is used to bridge the register-address write transaction and register-data read transaction. This bit is not programmable by MCU when I2CM_BUSY = 1. |
| 5:4 | - | Reserved |
| 3 | I2CM_SPEED | 0: I ² C Fast Mode 1: I ² C Standard Mode |
| 2:1 | - | Reserved |
| 0 | I2CM_GO | 1: Kicks off I ² C master operation. Clears to 0 after I ² C master operation is completed. This bit is not programmable when I2CM_BUSY = 1 |

20.10 I2CM_STATUS

| Name: I2CM_STATUS | | |
|--------------------|------------------|--|
| Address: 24 (18h) | | |
| Serial IF: R | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | I2CM_SDA_ERR | I2C master SDA error indication |
| 4 | I2CM_SCL_ERR | I2C master SCL error indication |
| 3 | I2CM_SRST_ERR | I2C master SRST error indication |
| 2 | I2CM_TIMEOUT_ERR | I2C master timeout error indication |
| 1 | I2CM_DONE | 1: Status bit, indicates I ² C master operation has completed, with or without errors. This bit is cleared due to (a) MCU read or (b) when I2CM_GO is programmed to 1 or (c) ODR event for fetching sensor data from the external sensor. |
| 0 | I2CM_BUSY | 0: Indicates no I ² C master operation is running 1: Indicates I ² C master operation is running |

20.11 I2CM_EXT_DEV_STATUS

| Name: I2CM_EXT_DEV_STATUS Address: 26 (1Ah) Serial IF: R/C Reset value: 0x0F Clock Domain: MCLK | | |
|---|---------------------|---|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:0 | I2CM_EXT_DEV_STATUS | <p>Indicates ACK/NACK feedback from the external device per each entry of the command buffer. I2CM_EXT_DEV_STATUS is set to 0xF whenever I²C master operation is kicked off.</p> <p>Bit 0 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_0. 0: ACK 1: NACK</p> <p>Bit 1 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_1. 0: ACK 1: NACK</p> <p>Bit 2 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_2. 0: ACK 1: NACK</p> <p>Bit 3 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_3. 0: ACK 1: NACK</p> |

20.12 I2CM_RD_DATA0

| Name: I2CM_RD_DATA0 Address: 27 (1Bh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA0 | <p>The 1st byte received from I²C slave.</p> <p>Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.</p> |

20.13 I2CM_RD_DATA1

| Name: I2CM_RD_DATA1 Address: 28 (1Ch) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA1 | The 2 nd byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.14 I2CM_RD_DATA2

| Name: I2CM_RD_DATA2 Address: 29 (1Dh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA2 | The 3 rd byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.15 I2CM_RD_DATA3

| Name: I2CM_RD_DATA3 Address: 30 (1Eh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA3 | The 4 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.16 I2CM_RD_DATA4

| Name: I2CM_RD_DATA4 Address: 31 (1Fh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA4 | The 5 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.17 I2CM_RD_DATA5

| Name: I2CM_RD_DATA5 Address: 32 (20h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA5 | The 6 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.18 I2CM_RD_DATA6

| Name: I2CM_RD_DATA6 Address: 33 (21h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA6 | The 7 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.19 I2CM_RD_DATA7

| Name: I2CM_RD_DATA7 Address: 34 (22h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA7 | The 8 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.20 I2CM_RD_DATA8

| Name: I2CM_RD_DATA8 Address: 35 (23h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA8 | The 9 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.21 I2CM_RD_DATA9

| Name: I2CM_RD_DATA9 Address: 36 (24h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA9 | The 10 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.22 I2CM_RD_DATA10

| Name: I2CM_RD_DATA10 Address: 37 (25h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA10 | The 11 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.23 I2CM_RD_DATA11

| Name: I2CM_RD_DATA11 Address: 38 (26h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA11 | The 12 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.24 I2CM_RD_DATA12

| Name: I2CM_RD_DATA12 Address: 39 (27h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA12 | The 13 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.25 I2CM_RD_DATA13

| Name: I2CM_RD_DATA13 Address: 40 (28h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA13 | The 14 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.26 I2CM_RD_DATA14

| Name: I2CM_RD_DATA14 Address: 41 (29h) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA14 | The 15 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.27 I2CM_RD_DATA15

| Name: I2CM_RD_DATA15 Address: 42 (2Ah) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA15 | The 16 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.28 I2CM_RD_DATA16

| Name: I2CM_RD_DATA16 Address: 43 (2Bh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA16 | The 17 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.29 I2CM_RD_DATA17

| Name: I2CM_RD_DATA17 Address: 44 (2Ch) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA17 | The 18 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.30 I2CM_RD_DATA18

| Name: I2CM_RD_DATA18 Address: 45 (2Dh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA18 | The 19 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.31 I2CM_RD_DATA19

| Name: I2CM_RD_DATA19 Address: 46 (2Eh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA19 | The 20 th byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.32 I2CM_RD_STATUS20

| Name: I2CM_RD_DATA20 Address: 47 (2Fh) Serial IF: RWS Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|---|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_RD_DATA20 | The 21 st byte received from I ² C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor. |

20.33 I2CM_WR_DATA0

| Name: I2CM_WR_DATA0 Address: 51 (33h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_WR_DATA0 | The data/address byte for a Write transaction. |

20.34 I2CM_WR_DATA1

| Name: I2CM_WR_DATA1 Address: 52 (34h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_WR_DATA1 | The data/address byte for a Write transaction. |

20.35 I2CM_WR_DATA2

| Name: I2CM_WR_DATA2 | | |
|---------------------|---------------|--|
| Address: 53 (35h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_WR_DATA2 | The data/address byte for a Write transaction. |

20.36 I2CM_WR_DATA3

| Name: I2CM_WR_DATA3 | | |
|---------------------|---------------|--|
| Address: 54 (36h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_WR_DATA3 | The data/address byte for a Write transaction. |

20.37 I2CM_WR_DATA4

| Name: I2CM_WR_DATA4 | | |
|---------------------|---------------|--|
| Address: 55 (37h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_WR_DATA4 | The data/address byte for a Write transaction. |

20.38 I2CM_WR_DATA5

| Name: I2CM_WR_DATA5 | | |
|---------------------|---------------|--|
| Address: 56 (38h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:0 | I2CM_WR_DATA5 | The data/address byte for a Write transaction. |

20.39 SIFS_IXC_ERROR_STATUS

| Name: SIFS_IXC_ERROR_STATUS Address: 75 (4Bh) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------------------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1 | AUX1_SIFS_IXC_TIMEOUT_ERR | 0: No timeout error. 1: Indicates than an lxC timeout error occurred in AUX1 SIFS. No clock toggle condition from host for 32ms while an lxC transaction was ongoing (after START and before STOP). |
| 0 | SIFS_IXC_TIMEOUT_ERR | 0: No timeout error or when SPI slave is selected for serial transfers. 1: Indicates than an lxC timeout error occurred in SIFS. No clock toggle condition from host for 32ms while an lxC transaction was ongoing (after START and before STOP). |

20.40 EDMP_PRGRM_IRQ0_0

| Name: EDMP_PRGRM_IRQ0_0 Address: 79 (4Fh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PRGRM_STRT_ADDR_IRQ0[7:0] | Start address of IRQ_0 vector. Can be changed on-the-fly. |

20.41 EDMP_PRGRM_IRQ0_1

| Name: EDMP_PRGRM_IRQ0_1 Address: 80 (50h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PRGRM_STRT_ADDR_IRQ0[15:8] | Start address of IRQ_0 vector. Can be changed on-the-fly. |

20.42 EDMP_PRGRM_IRQ1_0

| Name: EDMP_PRGRM_IRQ1_0 Address: 81 (51h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PRGRM_STRT_ADDR_IRQ_1[7:0] | Start address of IRQ_1 vector. Can be changed on-the-fly. |

20.43 EDMP_PRGRM_IRQ1_1

| Name: EDMP_PRGRM_IRQ1_1 Address: 82 (52h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PRGRM_STRT_ADDR_IRQ_1[15:8] | Start address of IRQ_1 vector. Can be changed on-the-fly. |

20.44 EDMP_PRGRM_IRQ2_0

| Name: EDMP_PRGRM_IRQ2_0 Address: 83 (53h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PRGRM_STRT_ADDR_IRQ_2[7:0] | Start address of IRQ_2 vector. Can be changed on-the-fly. |

20.45 EDMP_PRGRM_IRQ2_1

| Name: EDMP_PRGRM_IRQ2_1 Address: 84 (54h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | PRGRM_STRT_ADDR_IRQ_2[15:8] | Start address of IRQ_2 vector. Can be changed on-the-fly. |

20.46 EDMP_SP_START_ADDR

| Name: EDMP_SP_START_ADDR Address: 85 (55h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|--------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | EDMP_SP_START_ADDR | Sets eDMP stack address. Can be changed on-the-fly. |

20.47 SMC_CONTROL_0

| Name: SMC_CONTROL_0 Address: 88 (58h) Serial IF: R/W Reset value: 0x60 Clock Domain: MCLK | | |
|---|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:5 | - | Reserved |
| 4 | ACCEL_LP_CLK_SEL | <p>This bit is applicable to host interface operation.</p> <p>A. When RTC mode is not enabled (or RTC_MODE = 0):</p> <p>This bit is effective when the host interface is in accel only operation with ACCEL_MODE set to LP mode.</p> <p>0: Host interface is in AULP mode. 1: Host interface is in ALP mode.</p> <p>When I3CSM Synchronous Timing Control function is enabled on host interface, if the host interface is in accel only operation with ACCEL_MODE set to LP mode, ACCEL_LP_CLK_SEL must be set to 1. I3CSM Synchronous Timing Control may not generate correct timing if ACCEL_LP_CLK_SEL is set to 0.</p> <p>B. When RTC mode is enabled (or RTC_MODE = 1):</p> <p>Independent of enabling/disabling of I3CSM Synchronous timing control function, ACCEL_LP_CLK_SEL must be set to 1.</p> <p>Dynamic Change Supported.</p> |
| 3 | TEMP_DIS | 0: Temperature Sensor not disabled. 1: Temperature Sensor disabled. |
| 2 | TMST_FORCE_AUX_FINE_EN | 0: Time Stamp fine counting enabled only on UI interface. 1: Time Stamp fine counting enabled on AUX interfaces in addition to UI interface. |
| 1 | TMST_FSYNC_EN | Time Stamp register FSYNC Enable. 0: Timestamp feature of FSYNC not enabled. |

| | | |
|---|---------|--|
| | | 1: Timestamp feature of FSYNC enabled. |
| 0 | TMST_EN | 0: Timestamp not enabled. 1: Timestamp enabled. |

20.48 SMC_CONTROL_1

| Name: SMC_CONTROL_1 Address: 89 (59h) Serial IF: R/W Reset value: 0x04 Clock Domain: MCLK | | |
|---|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3 | SREG_AUX_ACCEL_ONLY_EN | 0: Sensor data register read from AUX1 interface is supported only if gyro sensor is enabled. 1: Sensor data register read from AUX1 interface is supported even if gyro sensor is not enabled. |
| 2:0 | - | Reserved |

20.49 STC_CONFIG

| Name: STC_CONFIG Address: 99 (63h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------|--|
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:2 | STC_SENSOR_SEL | Sensor that controls STC: 0 or 1: Slowest ODR sensor 2: Accel 3: Gyro |
| 1:0 | - | Reserved |

20.50 SREG_CTRL

| Name: SREG_CTRL Address: 103 (67h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1 | SREG_DATA_ENDIAN_SEL | Selects Endianness of Sensor Data Registers and FIFO data 0: Sensor data, FIFO data, and FIFO count is in Little Endian format 1: Sensor data, FIFO data, and FIFO count is in Big Endian format Note: User must set register field SREG_DATA_ENDIAN_SEL to 1, to enable Big Endian data format for data in Sensor Data Registers and FIFO, and for FIFO Count. |
| 0 | - | Reserved |

20.51 SIFS_I3C_STC_CFG

| Name: SIFS_I3C_STC_CFG Address: 104 (68h) Serial IF: R/W Reset value: 0x23 Clock Domain: MCLK | | |
|---|--------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2 | I3C_STC_MODE | Enable the STC controller 0: Disable I3C STC. 1: Enable I3C STC. Toggling this bit restarts the ODR frequency and phase correction operation as if the chip is out of reset. The STC functionality can be enabled only if ACCEL_LP_CLK_SEL is set to 1; otherwise device may not behave as expected. |
| 1:0 | - | Reserved |

20.52 INT_PULSE_MIN_ON_INTF0

| Name: INT_PULSE_MIN_ON_INTF0 Address: 105 (69h) Serial IF: R/W Reset value: 0x01 Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | INT0_TPULSE_DURATION | INT0 interrupt pulse minimum “on” duration for host interface, when in pulse mode. 0: 100µs (use only if ODR < 4kHz) 1: 8µs (required if ODR ≥ 4kHz, optional for ODR < 4kHz) Other Settings: Reserved |

20.53 INT_PULSE_MIN_ON_INTF1

| Name: INT_PULSE_MIN_ON_INTF1 Address: 106 (6Ah) Serial IF: R/W Reset value: 0x01 Clock Domain: MCLK | | |
|---|----------------------|---|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | INT1_TPULSE_DURATION | INT1 interrupt pulse minimum “on” duration for host interface, when in pulse mode. 0: 100µs (use only if ODR < 4kHz) 1: 8µs (required if ODR ≥ 4kHz, optional for ODR < 4kHz) Other Settings: Reserved |

20.54 INT_PULSE_MIN_OFF_INTF0

| Name: INT_PULSE_MIN_OFF_INTF0 Address: 107 (6Bh) Serial IF: R/W Reset value: 0x01 Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | INT0_TDEASSERT_DISABLE | INT0 interrupt pulse minimum “off” duration for host interface, indicates minimum interrupt de-assertion duration. 0: 100µs 1: 8µs Other Settings: Reserved |

20.55 INT_PULSE_MIN_OFF_INTF1

| Name: INT_PULSE_MIN_OFF_INTF1 Address: 108 (6Ch) Serial IF: R/W Reset value: 0x01 Clock Domain: MCLK | | |
|--|------------------------|--|
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | INT1_TDEASSERT_DISABLE | INT1 interrupt pulse minimum "off" duration for host interface, indicates minimum interrupt de-assertion duration. 0: 100µs 1: 8µs Other Settings: Reserved |

20.56 ISR_0_7

| Name: ISR_0_7 Address: 110 (6Eh) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|-------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | INT_STATUS_ON_DEMAND_PIN_0 | For IRQ0 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of on demand event. 0: Interrupt did not occur. 1: Interrupt occurred. |
| 4 | - | Reserved |
| 3 | INT_STATUS_EXT_ODR_DRDY_PIN_0 | For IRQ0 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of EXT ODR DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred. |
| 2:1 | - | Reserved |
| 0 | INT_STATUS_ACCEL_DRDY_PIN_0 | For IRQ0 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of Accel DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred. |

20.57 ISR_8_15

| Name: ISR_8_15 Address: 111 (6Fh) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|---|-------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | INT_STATUS_ON_DEMAND_PIN_1 | For IRQ1 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of on demand event. 0: Interrupt did not occur. 1: Interrupt occurred. |
| 4 | - | Reserved |
| 3 | INT_STATUS_EXT_ODR_DRDY_PIN_1 | For IRQ1 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of EXT ODR DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred. |
| 2:1 | - | Reserved |
| 0 | INT_STATUS_ACCEL_DRDY_PIN_1 | For IRQ1 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of Accel DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred. |

20.58 ISR_16_23

| Name: ISR_16_23 Address: 112 (70h) Serial IF: R/C Reset value: 0x00 Clock Domain: MCLK | | |
|--|-------------------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | INT_STATUS_ON_DEMAND_PIN_2 | For IRQ2 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of on demand event. 0: Interrupt did not occur. 1: Interrupt occurred. |
| 4 | - | Reserved |
| 3 | INT_STATUS_EXT_ODR_DRDY_PIN_2 | For IRQ2 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of EXT ODR DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred. |
| 2:1 | - | Reserved |
| 0 | INT_STATUS_ACCEL_DRDY_PIN_2 | For IRQ2 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of Accel DRDY event. 0: Interrupt did not occur. |

| | |
|--|------------------------|
| | 1: Interrupt occurred. |
|--|------------------------|

20.59 STATUS_MASK_PIN_0_7

| Name: STATUS_MASK_PIN_0_7 Address: 113 (71h) Serial IF: R/W Reset value: 0x3F Clock Domain: MCLK | | |
|--|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | INT_ON_DEMAND_PIN_0_DIS | For IRQ0, on-demand DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ON_DEMAND_PIN_0 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |
| 4 | - | Reserved |
| 3 | INT_EXT_ODR_DRDY_PIN_0_DIS | For IRQ0, ODR DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_EXT_ODR_DRDY_PIN_0 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |
| 2:1 | - | Reserved |
| 0 | INT_ACCEL_DRDY_PIN_0_DIS | For IRQ0, accel DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ACCEL_DRDY_PIN_0 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |

20.60 STATUS_MASK_PIN_8_15

| Name: STATUS_MASK_PIN_8_15 Address: 114 (72h) Serial IF: R/W Reset value: 0x3F Clock Domain: MCLK | | |
|---|----------------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | INT_ON_DEMAND_PIN_1_DIS | For IRQ1, on-demand DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ON_DEMAND_PIN_1 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |
| 4 | - | Reserved |
| 3 | INT_EXT_ODR_DRDY_PIN_1_DIS | For IRQ1, ODR DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_EXT_ODR_DRDY_PIN_1 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |
| 2:1 | - | Reserved |
| 0 | INT_ACCEL_DRDY_PIN_1_DIS | For IRQ1, accel DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ACCEL_DRDY_PIN_1 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |

20.61 STATUS_MASK_PIN_16_23

| Name: STATUS_MASK_PIN_16_23 Address: 115 (73h) Serial IF: R/W Reset value: 0x3F Clock Domain: MCLK | | |
|--|----------------------------|---|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | INT_ON_DEMAND_PIN_2_DIS | Enables the eDMP to be run once when IRQ2 is triggered by setting the EDMP_ON_DEMAND_EN bit. |
| 4 | - | Reserved |
| 3 | INT_EXT_ODR_DRDY_PIN_2_DIS | For IRQ2, ODR DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_EXT_ODR_DRDY_PIN_2 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |
| 2:1 | - | Reserved |
| 0 | INT_ACCEL_DRDY_PIN_2_DIS | For IRQ2, accel DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ACCEL_DRDY_PIN_2 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion. |

20.62 INT_I2CM_SOURCE

| Name: INT_I2CM_SOURCE Address: 116 (74h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|--------------------------------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1 | INT_STATUS_I2CM_SMC_EXT_ODR_EN | 0: Does not automatically trigger eDMP operation on target ODR 1: Automatically triggers eDMP operation on target ODR |
| 0 | - | Reserved |

20.63 ACCEL_WOM_X_THR

| Name: ACCEL_WOM_X_THR Address: 126 (7Eh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------|--|
| BIT | NAME | FUNCTION |
| 7:0 | WOM_X_TH | Set X-axis Wake on Motion threshold Wake on Motion thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256≈4mg) |

20.64 ACCEL_WOM_Y_THR

| Name: ACCEL_WOM_Y_THR Address: 127 (7Fh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------|---|
| BIT | NAME | FUNCTION |
| 7:0 | WOM_Y_TH | Set Y-axis Wake on Motion threshold Wake on Motion thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg) |

20.65 ACCEL_WOM_Z_THR

| Name: ACCEL_WOM_Z_THR Address: 128 (80h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|----------|---|
| BIT | NAME | FUNCTION |
| 7:0 | WOM_Z_TH | Set Z-axis Wake on Motion threshold Wake on Motion thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg) |

20.66 SELFTEST

| Name: SELFTEST Address: 144 (90h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5 | EN_GZ_ST | 0: Z-axis gyroscope self-test is not enabled 1: Z-axis gyroscope self-test is enabled Can be changed on-the-fly. |
| 4 | EN_GY_ST | 0: Y-axis gyroscope self-test is not enabled 1: Y-axis gyroscope self-test is enabled Can be changed on-the-fly. |
| 3 | EN_GX_ST | 0: X-axis gyroscope self-test is not enabled 1: X-axis gyroscope self-test is enabled Can be changed on-the-fly. |
| 2 | EN_AZ_ST | 0: Z-axis accelerometer self-test is not enabled 1: Z-axis accelerometer self-test is enabled Can be changed on-the-fly. |
| 1 | EN_AY_ST | 0: Y-axis accelerometer self-test is not enabled 1: Y-axis accelerometer self-test is enabled Can be changed on-the-fly. |
| 0 | EN_AX_ST | 0: X-axis accelerometer self-test is not enabled 1: X-axis accelerometer self-test is enabled Can be changed on-the-fly. |

20.67 IPREG_MISC

| Name: IPREG_MISC Address: 151 (97h) Serial IF: R Reset value: 0x02 Clock Domain: MCLK | | |
|---|-----------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1 | EDMP_IDLE | 0: Indicates eDMP is busy. 1: Indicates eDMP is idle. |
| 0 | - | Reserved |

20.68 SW_PLL1_TRIM

| Name: SW_PLL1_TRIM Address: 162 (A2h) Serial IF: R Reset value: 0x00 Clock Domain: MCLK | | |
|---|--------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | SW_PLL1_TRIM | Stores variation of PLL frequency test measurement vs. target value, used for SW applications. Value to trim = $(PLL_measurement - 6144000Hz) / 6144000Hz * 2540$. 6144000Hz is the target PLL freq. 2540 is the resolution coefficient: $max\ register\ range / max\ oscillator\ frequency\ error = (2^7 - 1) / 5\%$, with a sign bit. |

20.69 FIFO_SRAM_SLEEP

| Name: FIFO_SRAM_SLEEP Address: 167 (A7h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|--|-------------------------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1:0 | FIFO_GSLEEP_SHARED_SRAM | Set selected SRAM bank global sleep mode Bit 0: <ol style="list-style-type: none"> 1. When set to 1: SRAM bank-0 will remain enabled 2. When 0: permits SRAM bank-0 to go to sleep mode <ol style="list-style-type: none"> a. SRAM bank goes to sleep, if not allocated as FIFO memory space b. If allocated as FIFO memory space, remains active unless FIFO is empty and sensors are off Bit 1: <ol style="list-style-type: none"> 1. When set to 1: SRAM bank-1 will remain enabled 2. When 0: Permits SRAM bank-1 to go to sleep mode <ol style="list-style-type: none"> a. SRAM bank goes to sleep, if not allocated as FIFO memory space b. If allocated as FIFO memory space, remains active unless FIFO is empty and sensors are off |

21 USER BANK IPREG_SYS1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_SYS1. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

21.1 IPREG_SYS1_REG_42

| Name: IPREG_SYS1_REG_42 Address: 42 (2Ah) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_X_OFFUSER[7:0] | Low bits for X-gyro offset programmed by user. Range is ± 62.5 dps, resolution is 7.5mdps. |

21.2 IPREG_SYS1_REG_43

| Name: IPREG_SYS1_REG_43 Address: 43 (2Bh) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:0 | GYRO_X_OFFUSER[13:8] | Upper bits for X-gyro offset programmed by user. Range is ± 62.5 dps, resolution is 7.5mdps. |

21.3 IPREG_SYS1_REG_56

| Name: IPREG_SYS1_REG_56 Address: 56 (38h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Y_OFFUSER[7:0] | Low bits for Y-gyro offset programmed by user. Range is ± 62.5 dps, resolution is 7.5mdps. |

21.4 IPREG_SYS1_REG_57

| Name: IPREG_SYS1_REG_57 Address: 57 (39h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:0 | GYRO_Y_OFFUSER[13:8] | Upper bits for Y-gyro offset programmed by user. Range is ± 62.5 dps, resolution is 7.5mdps. |

21.5 IPREG_SYS1_REG_70

| Name: IPREG_SYS1_REG_70 Address: 70 (46h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|---------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | GYRO_Z_OFFUSER[7:0] | Low bits for Z-gyro offset programmed by user. Range is ± 62.5 dps, resolution is 7.5mdps. |

21.6 IPREG_SYS1_REG_71

| Name: IPREG_SYS1_REG_71 Address: 71 (47h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:0 | GYRO_Z_OFFUSER[13:8] | Upper bits for Z-gyro offset programmed by user. Range is ± 62.5 dps, resolution is 7.5mdps. |

21.7 IPREG_SYS1_REG_166

| Name: IPREG_SYS1_REG_166 Address: 166 (A6h) Serial IF: R/W Reset value: 0x1B Clock Domain: MCLK | | |
|---|---------------|---|
| BIT | NAME | FUNCTION |
| 7 | - | Reserved |
| 6:5 | GYRO_SRC_CTRL | Gyro SRC CTRL: 0: Interpolator and AAF FIR filter off 1: Interpolator off and AAF FIR filter on 2: Interpolator on and AAF FIR filter on 3: Reserved (debug mode) |
| 4:0 | - | Reserved |

21.8 IPREG_SYS1_REG_170

| Name: IPREG_SYS1_REG_170 | | |
|--------------------------|-----------------|---|
| Address: 170 (AAh) | | |
| Serial IF: R/W | | |
| Reset value: 0x0A | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:5 | - | Reserved |
| 4:1 | GYRO_LP_AVG_SEL | Gyro Low Power Mode Averaging Filter Selection 0000: 1x 0001: 2x 0010: 4x 0011: 5x 0100: 7x 0101: 8x 0110: 10x 0111: 11x 1000: 16x 1001: 18x 1010: 20x 1011: 32x 1100: 64x Others: Reserved |
| 0 | - | Reserved |

21.9 IPREG_SYS1_REG_172

| Name: IPREG_SYS1_REG_172 | | |
|--------------------------|-------------------|--|
| Address: 172 (ACh) | | |
| Serial IF: R/W | | |
| Reset value: 0x80 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | GYRO_UI_LPFBW_SEL | Selects cut-off bandwidth for Gyro UI path LPF 000: Bypass 001: ODR/4 010: ODR/8 011: ODR/16 100: ODR/32 101: ODR/64 110: ODR/128 111: ODR/128 |

Note: When the FIR AAF is enabled, the signal path BW is decided by the FIR AAF and UI LPF combination. Please refer to AN-000365 ICM-456xx User Guide for details.

22 USER BANK IPREG_SYS2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_SYS2. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

22.1 IPREG_SYS2_REG_24

| Name: IPREG_SYS2_REG_24 Address: 24 (18h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_X_OFFUSER[7:0] | Low bits for X-accel offset programmed by user. Range is $\pm 1g$, resolution is 0.125mg. |

22.2 IPREG_SYS2_REG_25

| Name: IPREG_SYS2_REG_25 Address: 25 (19h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:0 | ACCEL_X_OFFUSER[13:8] | Upper bits for X-accel offset programmed by user. Range is $\pm 1g$, resolution is 0.125mg. |

22.3 IPREG_SYS2_REG_32

| Name: IPREG_SYS2_REG_32 Address: 32 (20h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_Y_OFFUSER[7:0] | Low bits for Y-accel offset programmed by user. Range is $\pm 1g$, resolution is 0.125mg. |

22.4 IPREG_SYS2_REG_33

| Name: IPREG_SYS2_REG_33 Address: 33 (21h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:0 | ACCEL_Y_OFFUSER[13:8] | Upper bits for Y-accel offset programmed by user. Range is $\pm 1g$, resolution is 0.125mg. |

22.5 IPREG_SYS2_REG_40

| Name: IPREG_SYS2_REG_40 Address: 40 (28h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|----------------------|--|
| BIT | NAME | FUNCTION |
| 7:0 | ACCEL_Z_OFFUSER[7:0] | Low bits for Z-accel offset programmed by user. Range is $\pm 1g$, resolution is 0.125mg. |

22.6 IPREG_SYS2_REG_41

| Name: IPREG_SYS2_REG_41 Address: 41 (29h) Serial IF: R/W Reset value: 0x00 Clock Domain: MCLK | | |
|---|-----------------------|--|
| BIT | NAME | FUNCTION |
| 7:6 | - | Reserved |
| 5:0 | ACCEL_Z_OFFUSER[13:8] | Upper bits for Z-accel offset programmed by user. Range is $\pm 1g$, resolution is 0.125mg. |

22.7 IPREG_SYS2_REG_123

| Name: IPREG_SYS2_REG_123 Address: 123 (7Bh) Serial IF: R/W Reset value: 0x14 Clock Domain: MCLK | | |
|---|----------------|--|
| BIT | NAME | FUNCTION |
| 7:2 | - | Reserved |
| 1:0 | ACCEL_SRC_CTRL | Accel SRC CTRL: 0: Interpolator and AAF FIR filter off 1: Interpolator off and AAF FIR filter on 2: Interpolator on and AAF FIR filter on 3: Reserved (debug mode) |

22.8 IPREG_SYS2_REG_129

| Name: IPREG_SYS2_REG_129 | | |
|--------------------------|------------------|--|
| Address: 129 (81h) | | |
| Serial IF: R/W | | |
| Reset value: 0x02 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:4 | - | Reserved |
| 3:0 | ACCEL_LP_AVG_SEL | Accel Low Power Mode Averaging Filter Selection 0000: 1x 0001: 2x 0010: 4x 0011: 5x 0100: 7x 0101: 8x 0110: 10x 0111: 11x 1000: 16x 1001: 18x 1010: 20x 1011: 32x 1100: 64x Others: Reserved |

22.9 IPREG_SYS2_REG_131

| Name: IPREG_SYS2_REG_131 | | |
|--------------------------|--------------------|---|
| Address: 131 (83h) | | |
| Serial IF: R/W | | |
| Reset value: 0x00 | | |
| Clock Domain: MCLK | | |
| BIT | NAME | FUNCTION |
| 7:3 | - | Reserved |
| 2:0 | ACCEL_UI_LPFBW_SEL | Selects cut-off bandwidth for Accel UI path LPF 000: Bypass 001: ODR/4 010: ODR/8 011: ODR/16 100: ODR/32 101: ODR/64 110: ODR/128 111: ODR/128 |

Note: When the FIR AAF is enabled, the signal path BW is decided by the FIR AAF and UI LPF combination. Please refer to AN-000365 ICM-456xx User Guide for details.

23 REFERENCE

Please refer to the following application notes for additional information.

- IxM-4xxxx, IxM-2xxxx and MPU-6xxx Products PCB Design, Mounting, and Handling Guidelines (AN-000393)
- Understanding IMU Sensor Offset (AN-000257)
- TDK InvenSense IMU Calibration Application Note (AN-000265)
- ICM-456xx Errata Update (AN-000364)
- ICM-45605 & ICM-45686 User Guide (AN-000478)

24 REVISION HISTORY

| Revision Date | Revision | Description |
|---------------|----------|-----------------|
| 07/25/2024 | 1.0 | Initial Release |

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