



# BUK9M13-80L

N-channel 80 V, 13 mOhm logic level MOSFET in LPAK33

3 September 2024

Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LPAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Logic-level compatible
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automatic optical inspection

## 3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- LED lighting
- Circuit protection

## 4. Quick reference data

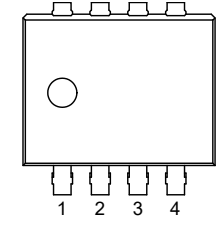
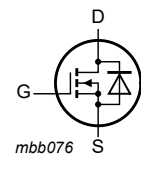
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	55	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	91	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	6.8	10.6	12.5	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 15\text{ A}$ ; $V_{DS} = 40\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	1.1	3.8	8.4	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 40\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 17</a>	-	30.8	-	nC

[1] 55 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M13-80L	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M13-80L	91380L

## 8. Limiting values

Table 5. Limiting values

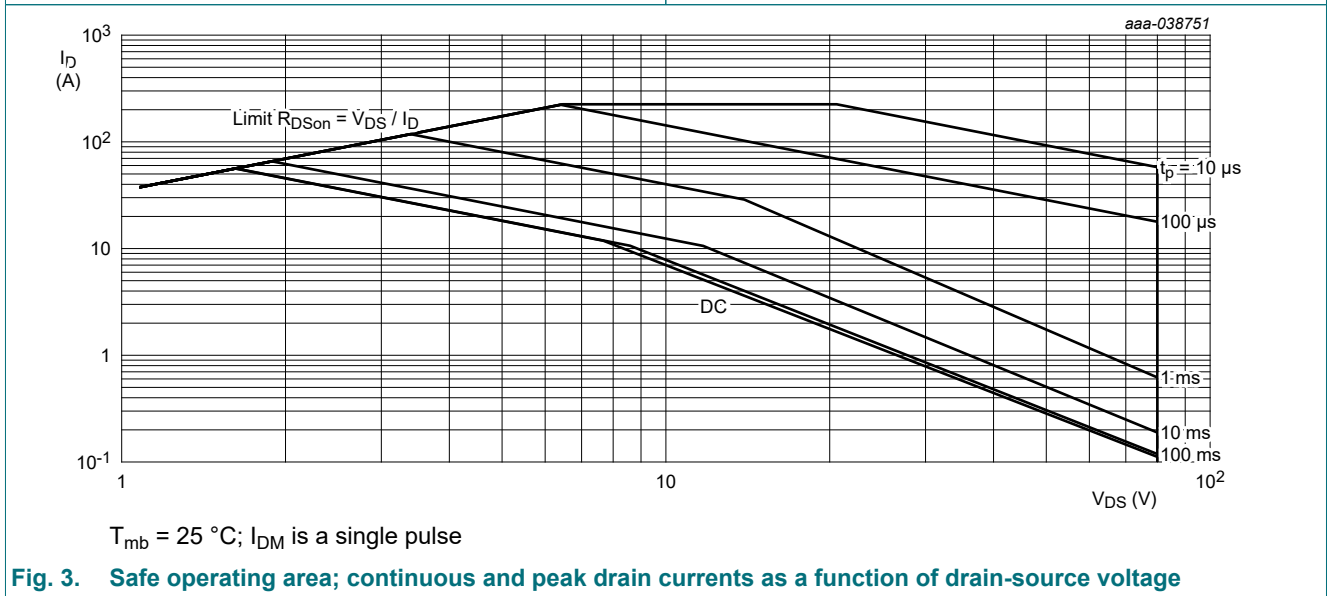
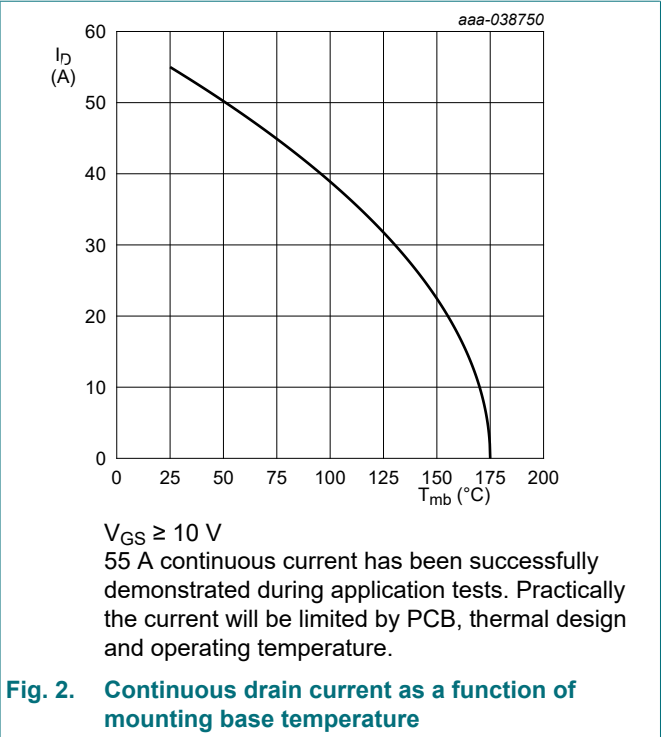
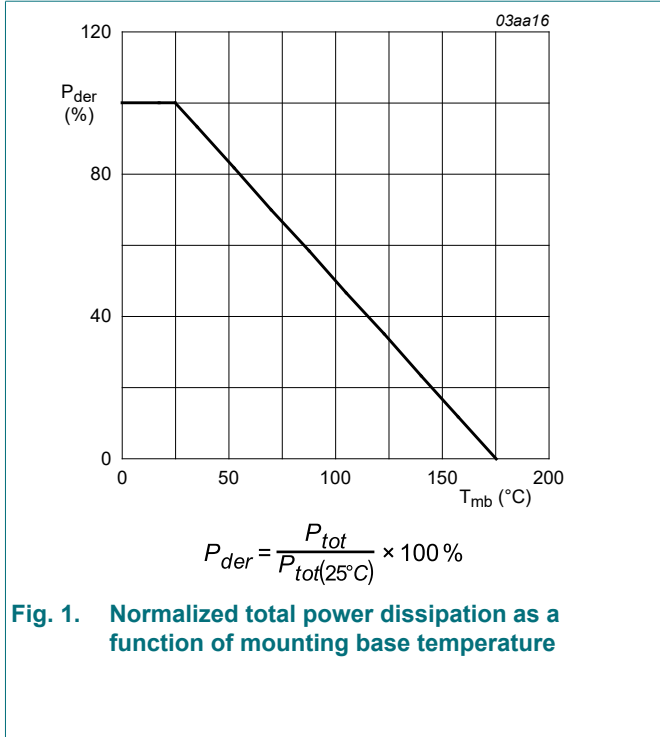
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

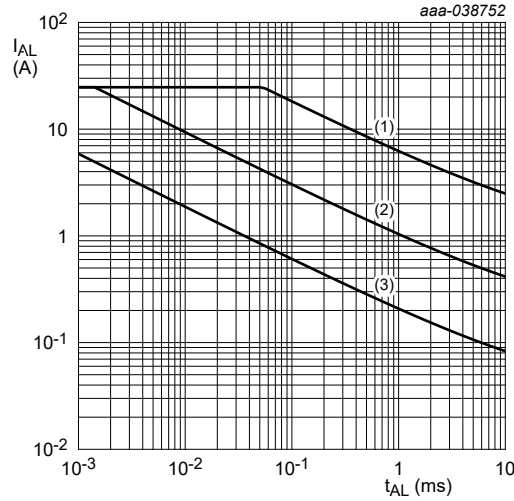
Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	80	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1		-	91	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	[1]	-	55	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2		-	39	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3		-	225	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	55	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	225	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 24.8\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; unclamped; $t_{AL} = 53\text{ }\mu\text{s}$ ; Fig. 4	[2] [3]	-	68.6	mJ

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Symbol	Parameter	Conditions	Min	Max	Unit	
$I_{AS}$	non-repetitive avalanche current	$V_{sup} = 80\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $R_{GS} = 50\text{ }\Omega$ ; Fig. 4	[2] [3]	-	24.8	A

- [1] 55 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.





(1)  $T_{j (init)} = 25\text{ }^{\circ}\text{C}$ ; (2)  $T_{j (init)} = 150\text{ }^{\circ}\text{C}$ ; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.4	1.65	K/W

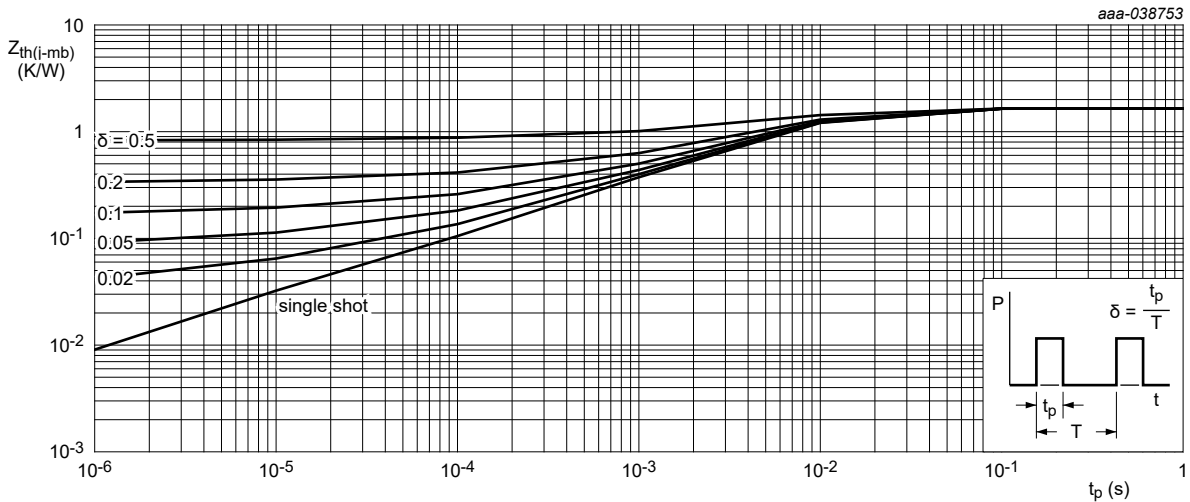


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	91	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	73.5	88.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	87	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.12 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	1.4	1.7	2.05	V
		$I_D = 0.12 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	0.5	-	-	V
		$I_D = 0.12 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.03	1	$\mu A$
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	20	100	$\mu A$
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	90	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	6.8	10.6	12.5	m $\Omega$
		$V_{GS} = 10 V; I_D = 15 A; T_j = 105 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	10	16.3	20.1	m $\Omega$
		$V_{GS} = 10 V; I_D = 15 A; T_j = 125 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	11	18	22.2	m $\Omega$
		$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	13.2	22	28.6	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	8.8	14.7	18.8	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 105 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	12.9	22.6	25.7	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 125 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	14.1	24.9	33.4	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	17.1	31.2	43	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	1	2	4	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 40 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	8.6	17.2	25.8	nC
		$I_D = 15 A; V_{DS} = 40 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	17.1	34.2	51.3	nC
$Q_{GS}$	gate-source charge	$I_D = 15 A; V_{DS} = 40 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	4	6.6	9.2	nC
$Q_{GD}$	gate-drain charge	$I_D = 15 A; V_{DS} = 40 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	1.1	3.8	8.4	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15 A; V_{DS} = 40 V; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 25 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 15</a>	1431	2386	3341	pF
$C_{oss}$	output capacitance	$V_{DS} = 25 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 15</a>	335	559	894	pF
$C_{rss}$	reverse transfer capacitance	$V_{DS} = 25 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 15</a>	13.6	34	54.3	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40\text{ V}; R_L = 2.6\ \Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	18	-	ns
$t_r$	rise time		-	20	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
$t_f$	fall time		-	10	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 16}$	-	0.87	1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	44	-	ns
$Q_r$	recovered charge	$V_{DS} = 40\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	30.8	-	nC

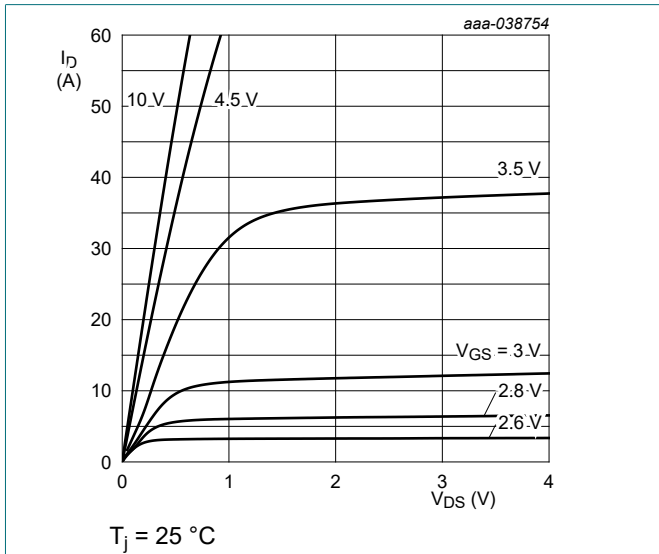


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

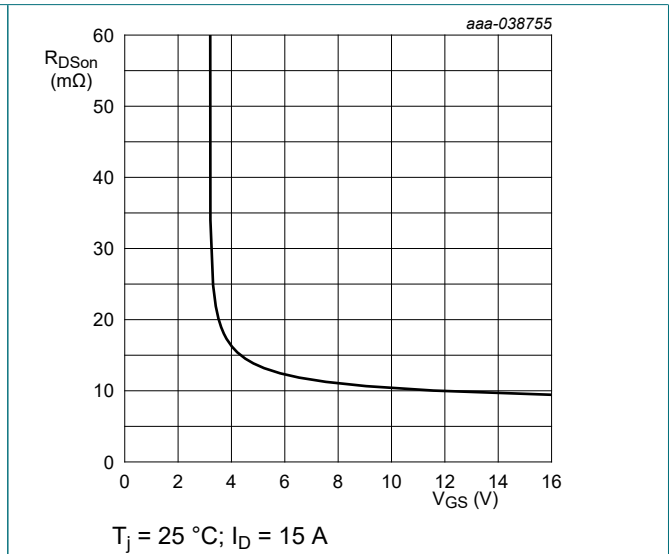


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

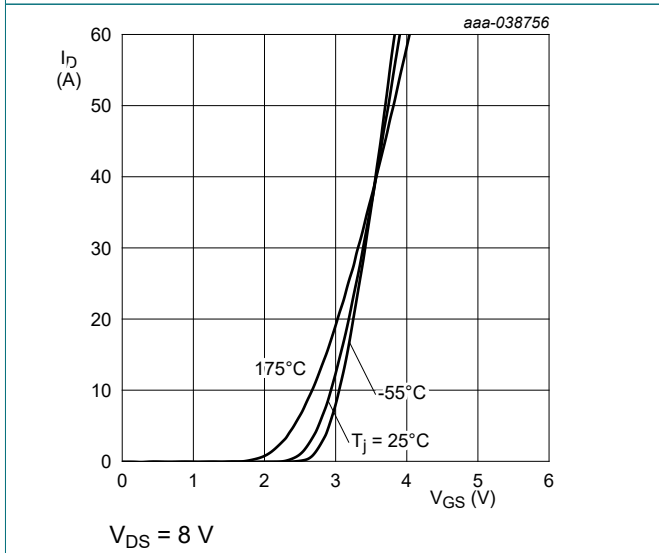


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

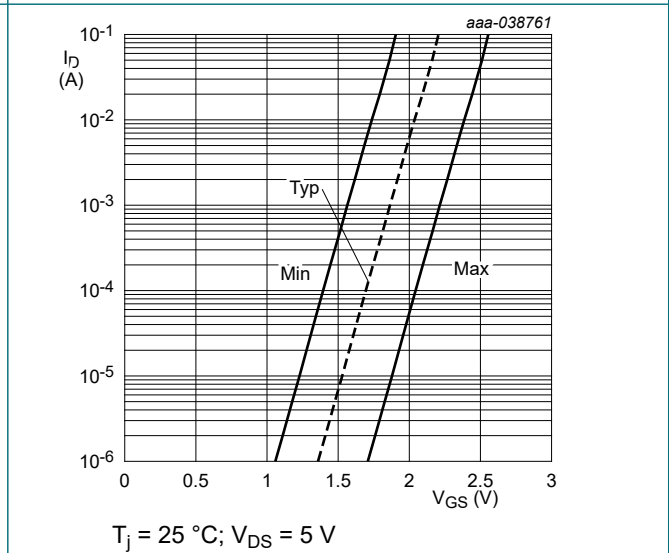


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

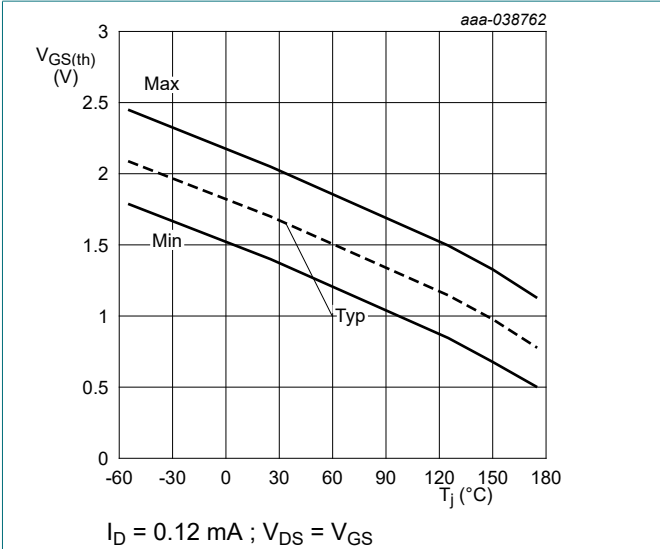


Fig. 10. Gate-source threshold voltage as a function of junction temperature

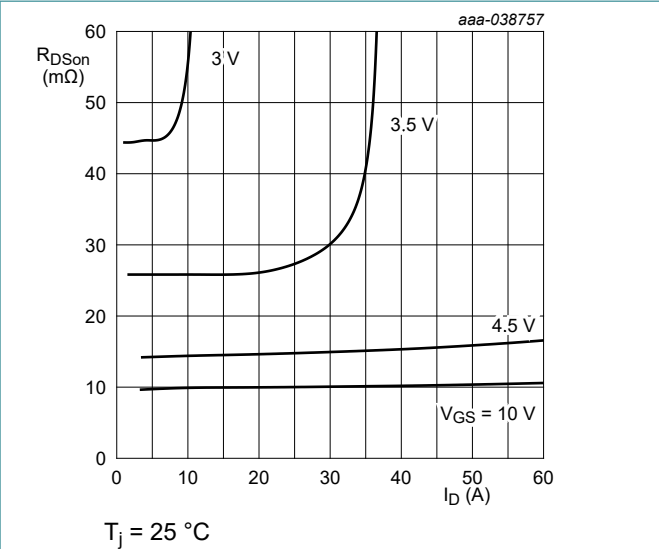


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

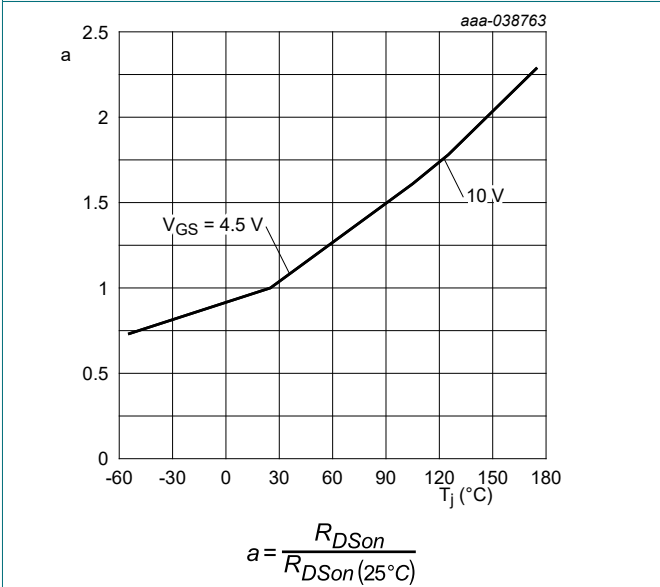


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

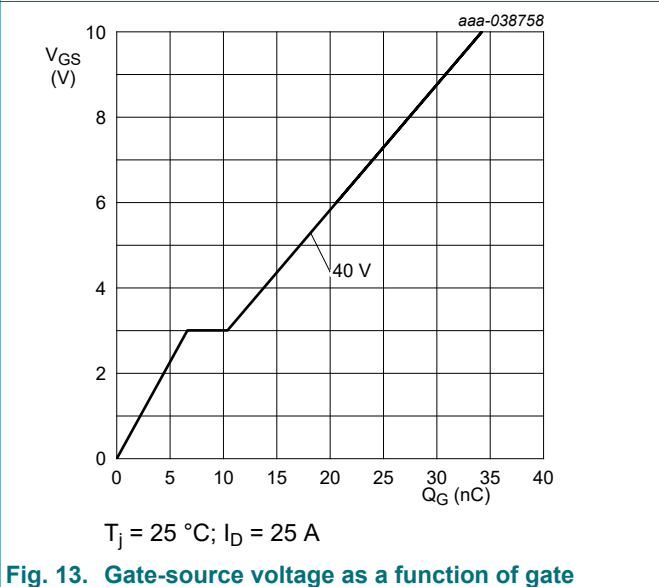


Fig. 13. Gate-source voltage as a function of gate charge; typical values

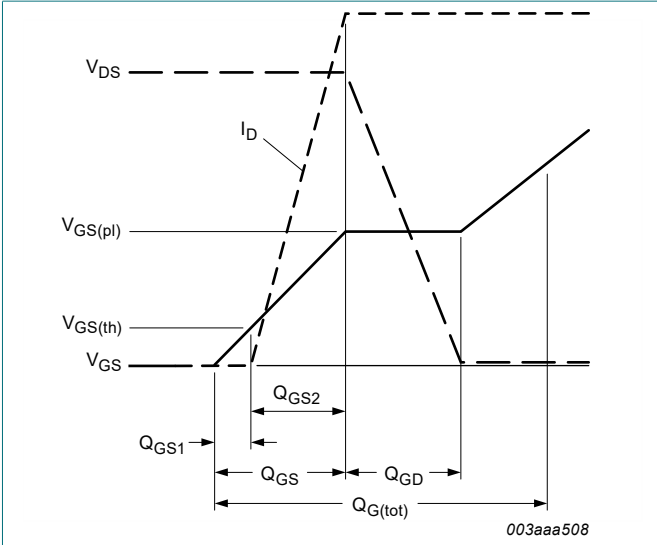


Fig. 14. Gate charge waveform definitions

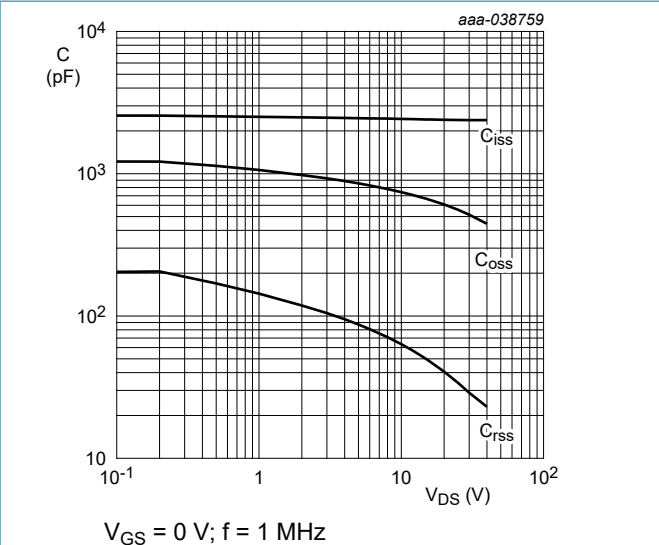


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

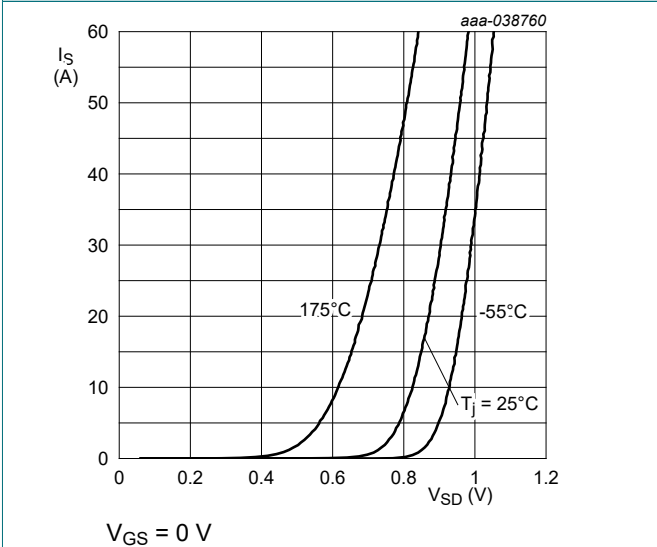


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

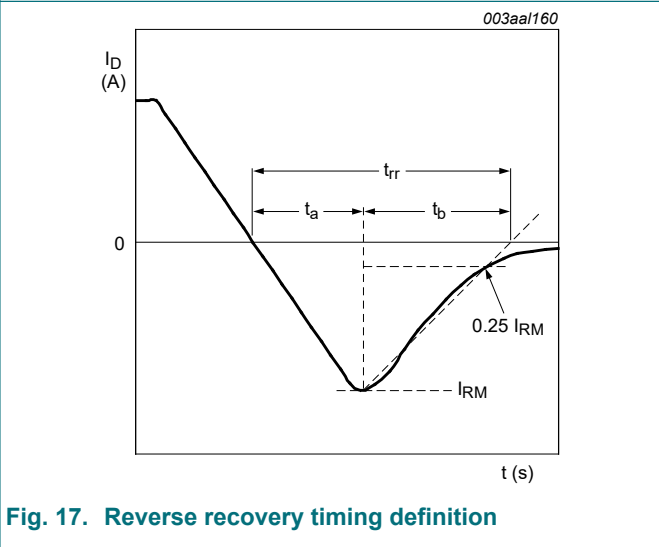


Fig. 17. Reverse recovery timing definition

### 11. Package outline

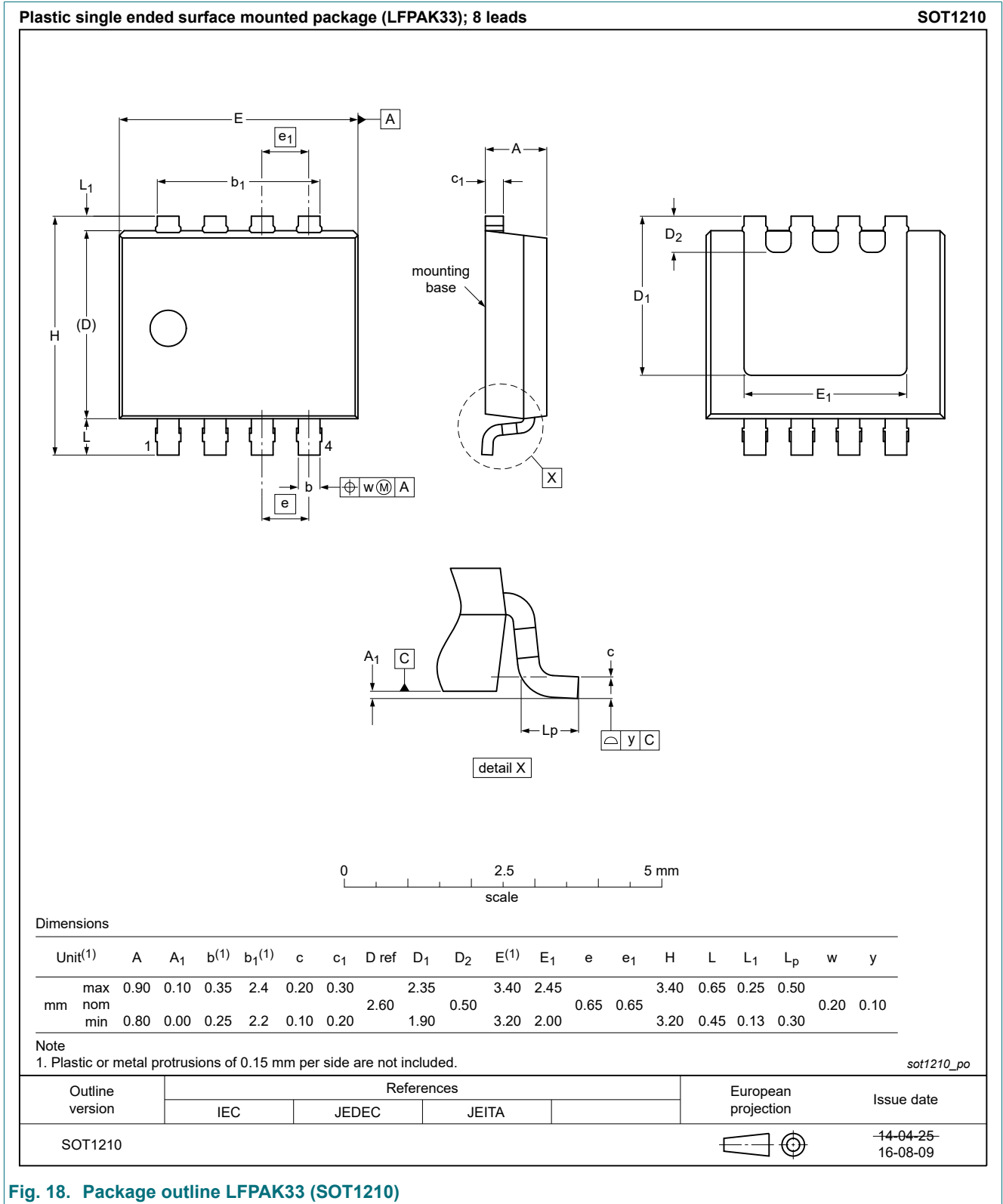
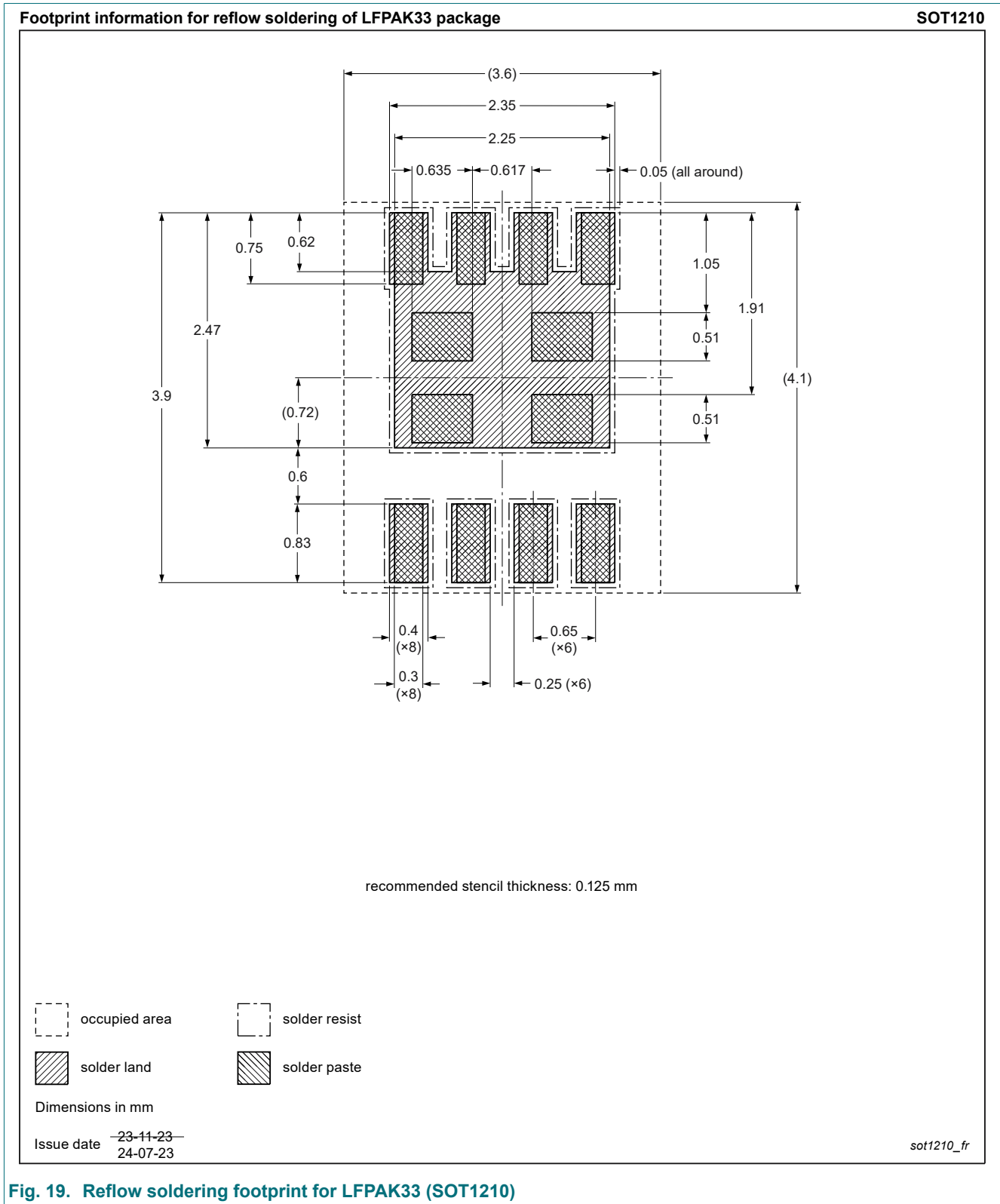


Fig. 18. Package outline LPAK33 (SOT1210)

## 12. Soldering



**Fig. 19. Reflow soldering footprint for LPAK33 (SOT1210)**

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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