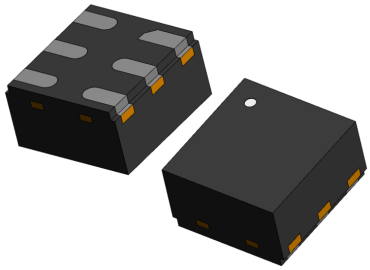
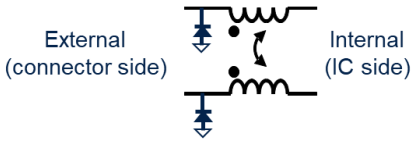
ECMF2-40A100M6Y

Datasheet

Automotive common mode filter for differential channels with integrated ESD protection



QFN-6L 1.4 x 1.35 mm
(DFN1414)



Functional schematic

Product label

Product status link

ECMF2-40A100M6Y

Features

- AEC-Q101 qualified
- 12.5 GHz differential bandwidth to comply with MIPI, FPD-link, GMSL, APIX, HDMI 2.0, HDMI 2.1, USB3.2 gen1/gen2 and USB4
- Common mode attenuation on LTE, BLE, Wi-Fi and V2x frequencies:
  - -15 dB at 2.4 GHz
  - -15 dB at 5.9 GHZ
- Low leakage current at V_{RM} (I_R < 70 nA)
- Wettable flank for automatic optical inspection
- Low PCB space consumption: 1.89 mm²
- ECOPACK2 RoHS compliant component
- Complies with ISO 10605 - C = 150 pF, R = 330 Ω
  - ±9 kV (contact discharge)
  - ±20 kV (air discharge)
- Complies with the following standards:
  - UL94, V0
  - J-STD-020 MSL level 1
  - IPC7531 footprint and JEDEC registered package

Application

High speed applications where common mode noise and electrostatic discharges must be suppressed such as:

- In-vehicle high speed network: SerDes, MIPI, LVDS
- Advanced driver assistance systems (ADAS), cameras, radar
- In-vehicle infotainment (IVI)
- Digital cluster

Description

The ECMF2-40A100M6Y is an integrated common mode filter designed to effectively suppress EMI/RFI common mode noise on high-speed data lines including MIPI A-PHY, FPD-link III, GMSL, APIX, USB2.0 USB3.2, USB4, HDMI2.0, HDMI2.1.

Engineered to replace traditional discrete common mode chokes or LTCC, this device integrates robust ESD protections on connector side to comply with ISO 10605 standards, making it an ideal choice for enhancing signal integrity. With this 2-in-1 combination, the ECMF2-40A100M6Y offers superior RF performance compared to discrete filters with external ESD protection.

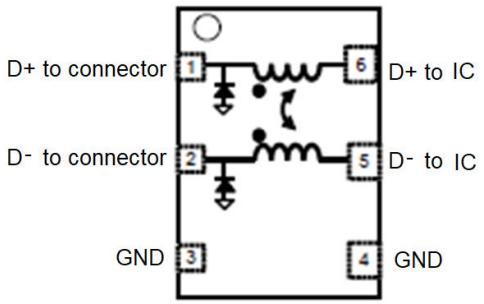
Its packaging in a QFN-6L (DFN1414) with wettable flanks guarantees compatibility with automatic visual inspection (AOI) systems. This component is perfect for designers looking to improve their products' EMI/RFI suppression capabilities with a space-efficient and reliable solution.

1 Pin configuration and function

Table 1. **Table 1. ECMF2-40A100M6Y pin description**

Pin #	Type	Description
1	I/O	D+ to connector
2	I/O	D- to connector
3	GND	Ground
4	GND	Ground
5	I/O	D- to IC
6	I/O	D+ to IC

Figure 1. **ECMF2-40A100M6Y pinout (top view)**



Pin layout

2 Characteristics

Table 2. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Pins	Value	Unit
V_{ESD}	Electrostatic discharge	ISO 10605 - C = 150 pF, R = 330 Ω: Contact discharge Air discharge	pin 1, pin 2	 ±9 ±20	kV
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins	±8	
I_{RMS}	RMS current			100	mA
T_j	Operating junction temperature range			-55 to +150	°C
T_{stg}	Storage temperature range			-65 to +175	
T_L	Maximum lead temperature for soldering during 10 s			260	

Figure 2. Electrical characteristics (definitions)

V_{RM} Maximum stand-off voltage
V_{CL} Clamping voltage at peak pulse current I_{PP}
I_{RM} Leakage current at V_{RM}
I_{PP} Peak pulse current
V_{BR} Breakdown voltage
R_{DC} DC serial resistance
f_C Differential cut off frequency

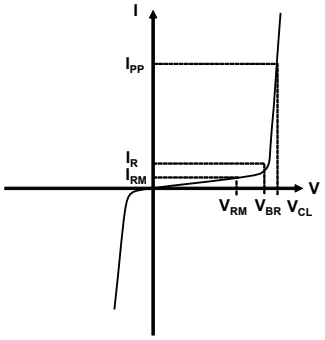


Table 3. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{RM}	Reverse Stand-Off voltage				5	V
V_{BR}	Reverse breakdown voltage	I_R = 1 mA	5.3	5.8		V
I_R	Reverse leakage current at V_R	V_R = 3.6 V			50	nA
I_{RM}	Reverse leakage current at V_{RM}	V_{RM} = 5 V			70	nA
R_{DC}	DC serial resistance	I_{DC} = 20 mA		2.9	4	Ω
f_c (1)(2)	Differential mode cut-off frequency	S_{DD21} = -3 dB		12.5		GHz
V_{CL} (1)	ESD clamping voltage	ISO 10605 (150 pF – 330 Ω), 8 kV contact discharge after 30 ns		20		V

1. *Specified by design – Not tested in production.*
2. *Normalized to attenuation at 10 MHz.*

2.1 Characteristics (curves)

Figure 3. Differential attenuation versus frequency (Z_{0_diff} = 100 Ω)

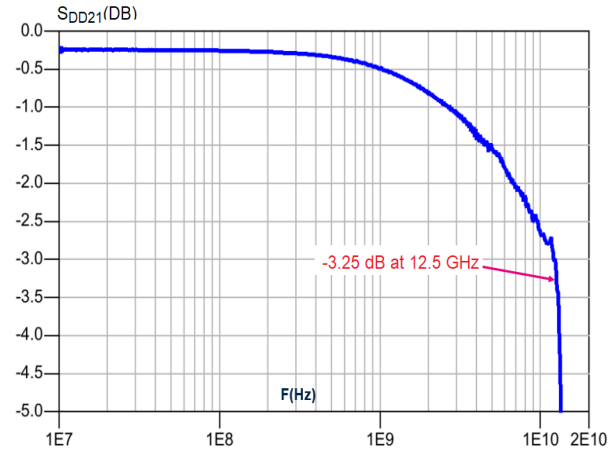


Figure 4. Common mode attenuation versus frequency (Z_{0_com} = 50 Ω)

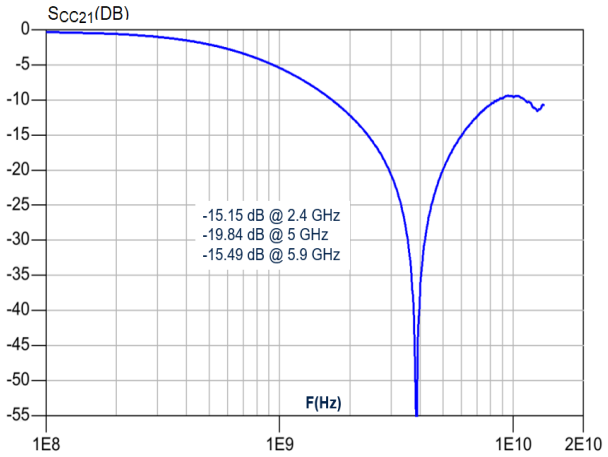


Figure 5. Differential mode return losses on connector side versus frequency (Z_{0_diff} = 100 Ω)

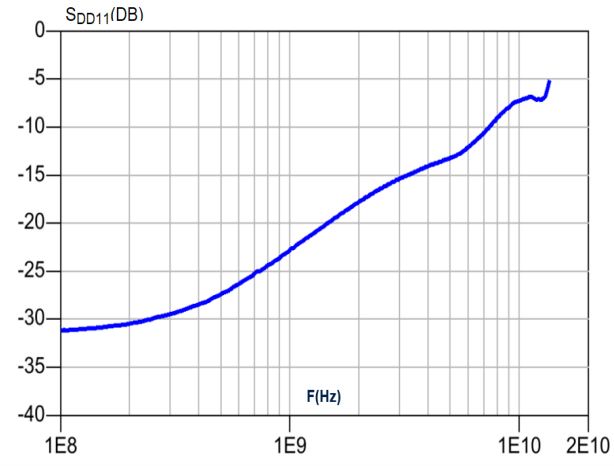


Figure 6. Differential mode return losses on IC side versus frequency (Z_{0_diff} = 100 Ω)

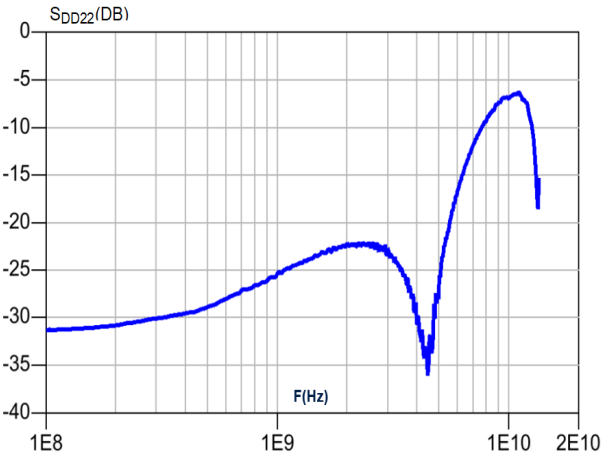


Figure 7. HDMI2.0 – 5.94 Gbps eye diagram without device (with worst cable and equaliser)

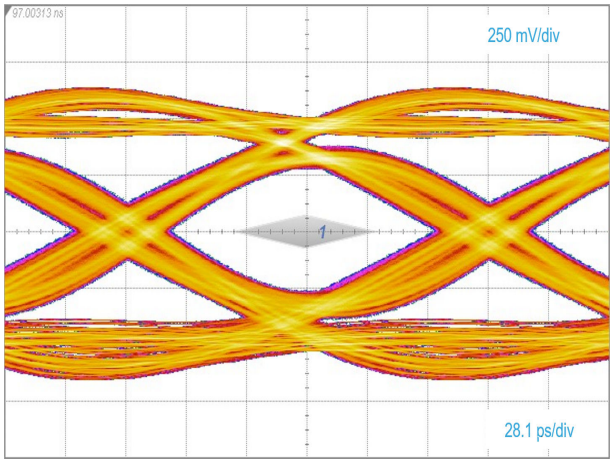


Figure 8. HDMI2.0 – 5.94 Gbps eye diagram with device (with worst cable and equaliser)

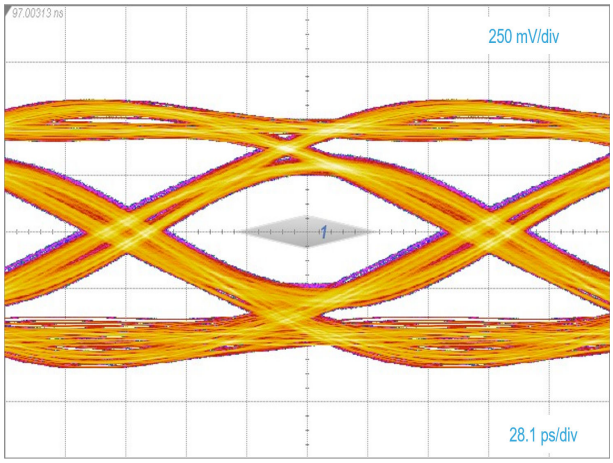


Figure 9. HDMI2.1 – 12 Gbps eye diagram without device (with worst cable model WCM3), EQ with 8 dB CTLE and one-tap DFE

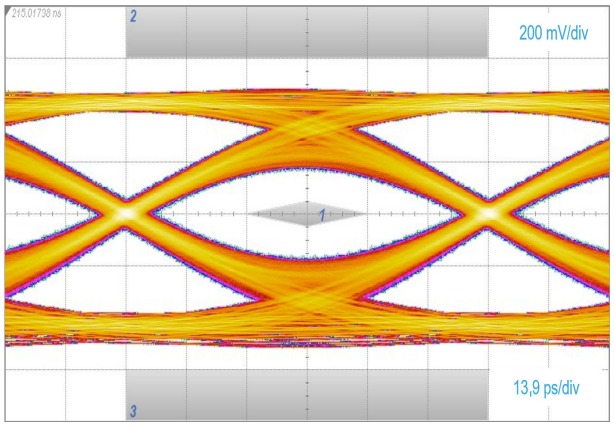


Figure 10. HDMI2.1 – 12 Gbps eye diagram with device (with worst cable model WCM3), EQ with 8 dB CTLE and one-tap DFE

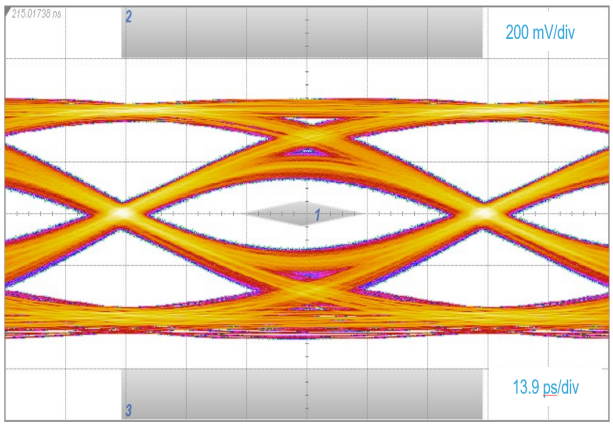


Figure 11. USB3.2 Gen1 – 5 Gbps Type-C eye diagram without device (with type C connector, reference cable and equalizer)

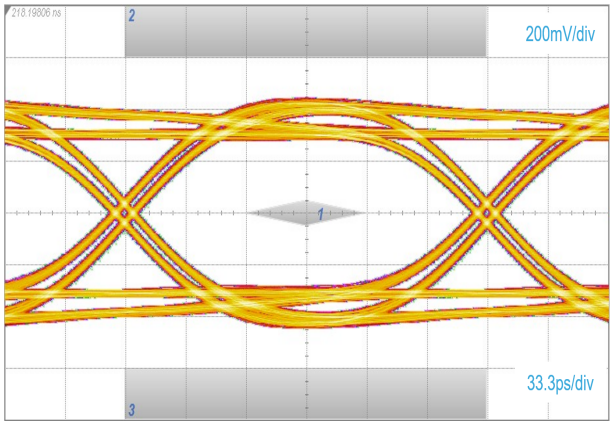


Figure 12. USB3.2 Gen1 – 5 Gbps Type-C eye diagram with device (with type C connector, reference cable and equalizer)

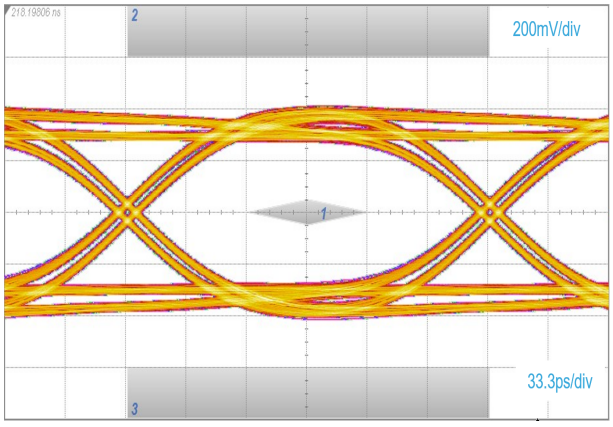


Figure 13. USB3.2 Gen2 – 10 Gbps eye diagram without device (with type C connector, reference cable, equalizer with ADC = 6 dB and DFE)

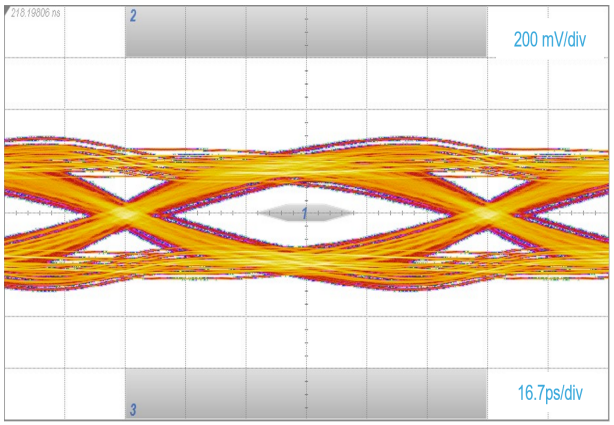


Figure 14. USB3.2 Gen2 – 10 Gbps eye diagram with device (with type C connector, reference cable, equalizer with ADC = 6 dB and DFE)

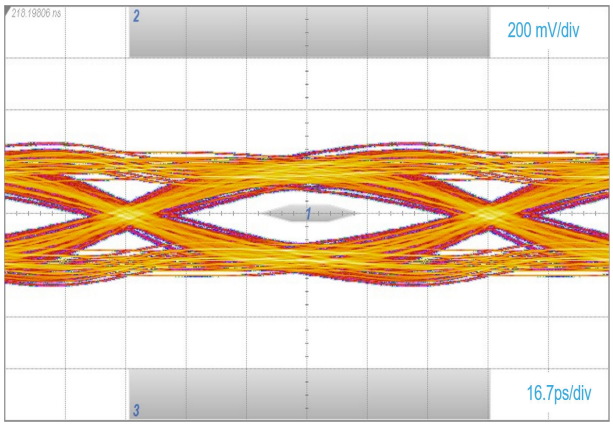


Figure 15. USB4 – 20 Gbps eye diagram without device (with type C connector, preset 0, reference cable 0.8m, equalizer with ADC = 0dB and DFE)

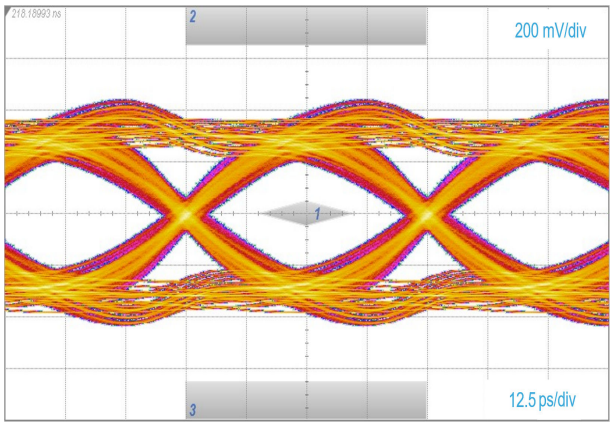


Figure 16. USB4 – 20 Gbps eye diagram with device (with type C connector, preset 0, reference cable 0.8m, equalizer with ADC = 0dB and DFE)

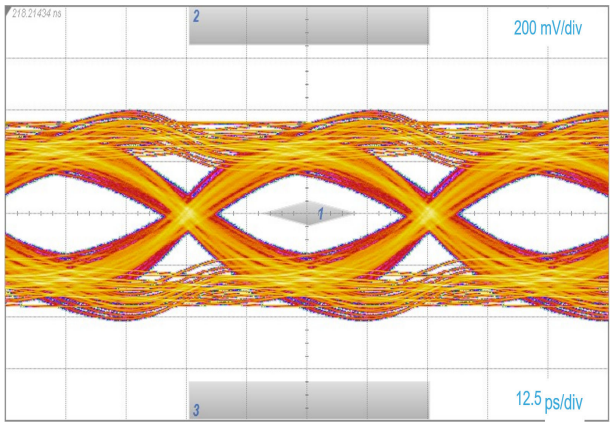


Figure 17. FPD LinkIII – 4.16 Gbps eye diagram – without device

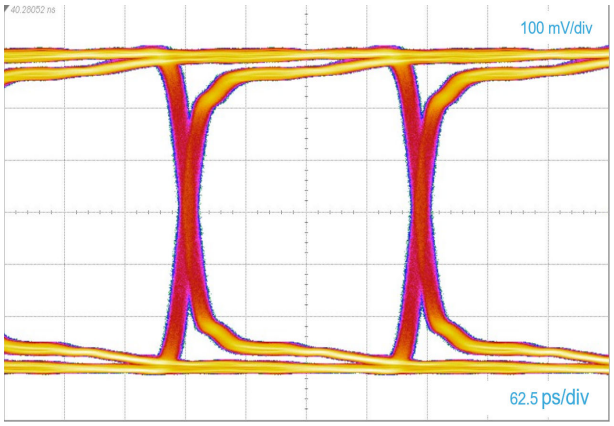


Figure 18. FPD LinkIII – 4.16 Gbps eye diagram – with device

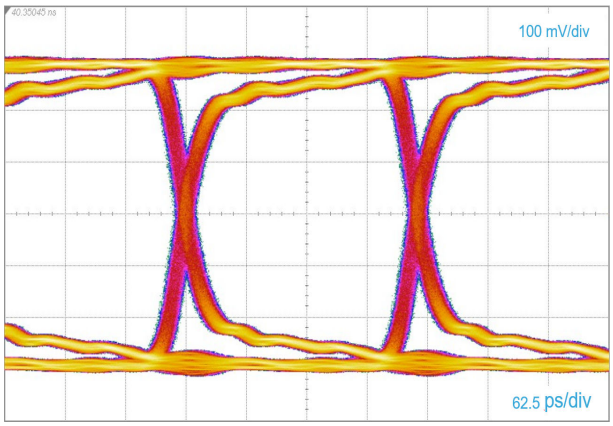


Figure 19. GMSL – 3.12 Gbps eye diagram without device

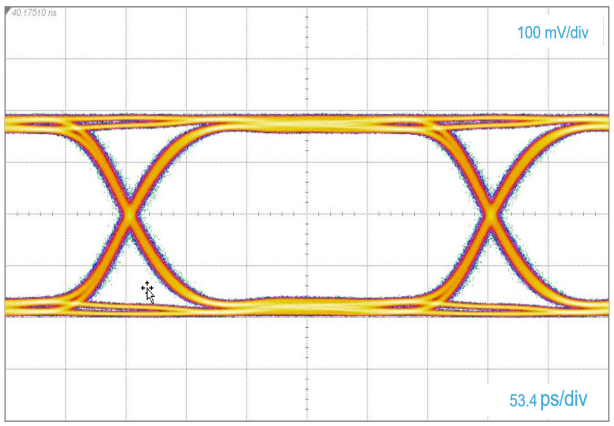


Figure 20. GMSL – 3.12 Gbps eye diagram with device

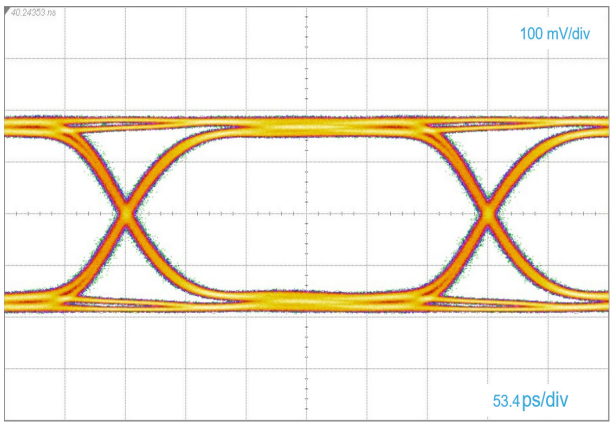


Figure 21. MIPI A-PHY G2 4 Gbps eye diagram – without device

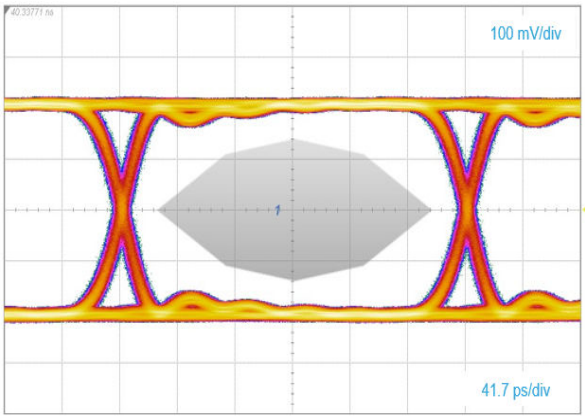


Figure 22. MIPI A-PHY G2 4 Gbps eye diagram – with device

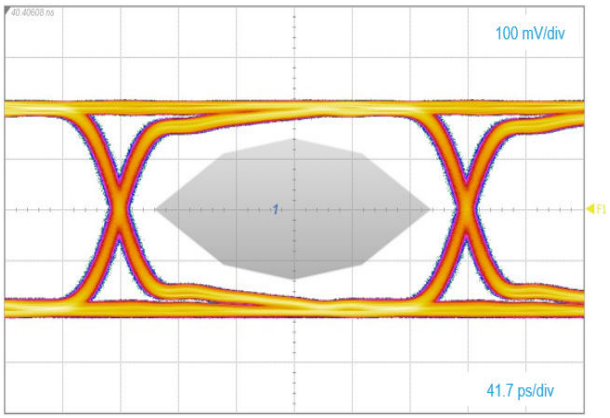


Figure 23. MIPI A-PHY G3 8 Gbps eye diagram – without device

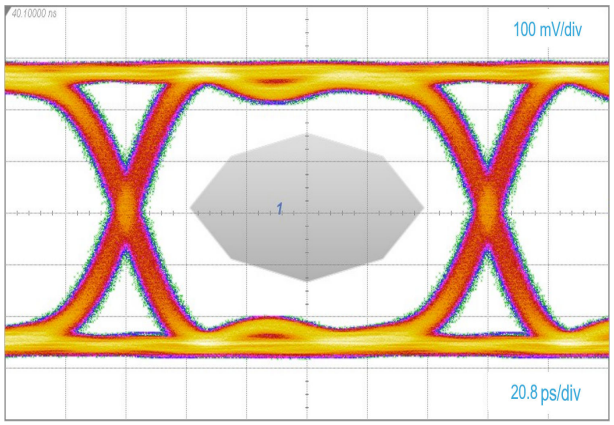


Figure 24. MIPI A-PHY G3 8 Gbps eye diagram – with device

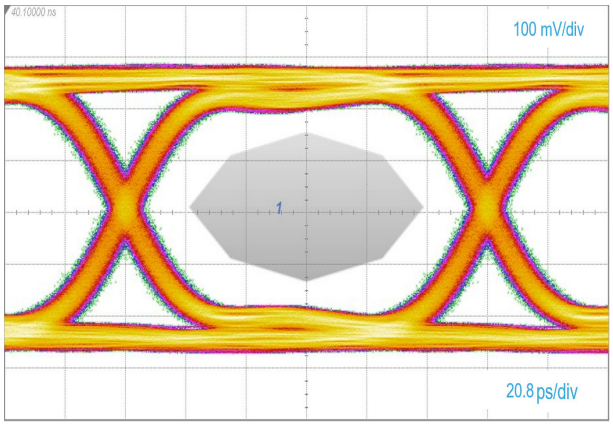


Figure 25. ISO 10605 - C = 150 pF, R = 330 Ω (+8 kV contact)

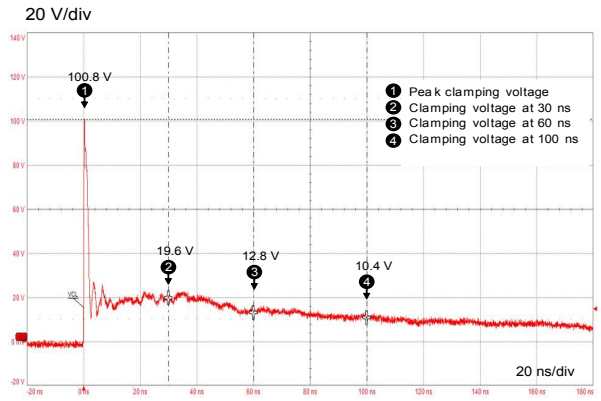


Figure 26. ISO 10605 - C = 150 pF, R = 330 Ω (-8 kV contact)

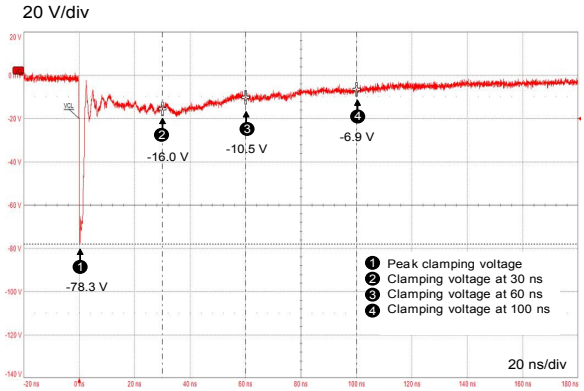
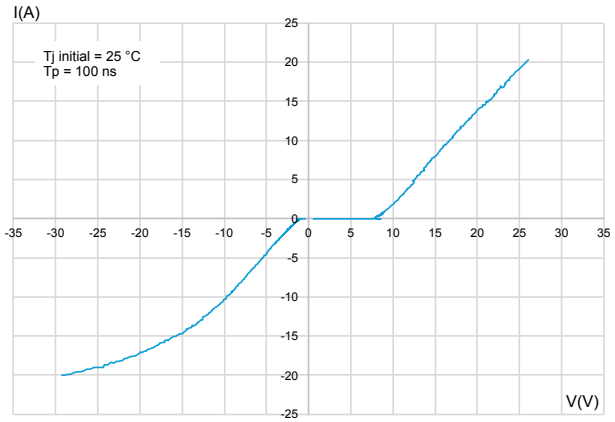


Figure 27. TLP characteristic



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 Package information

Figure 28. Package outline

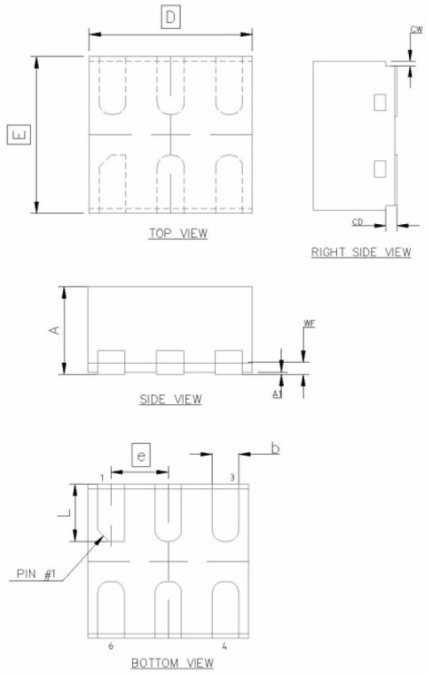


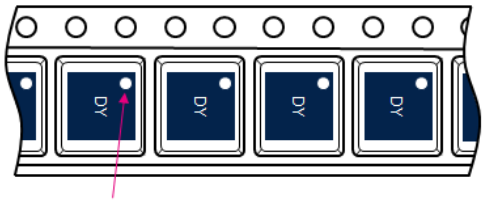
Table 4. Mechanical data

Symbol	Dimesions (milimeters)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.16	0.23	0.28
D	1.35	1.40	1.45
E	1.30	1.35	1.40
e		0.50	
L	0.40	0.50	0.60
CD	0.10		
CW	0.01	0.05	0.09
WF	0.10		

3.2 Packing information

Figure 29. **Marking**

Figure 30. **Package orientation in reel**



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Only pin 1 mark must be used to orient the component for its placement on a PCB.

Figure 31. **Tape and reel orientation**

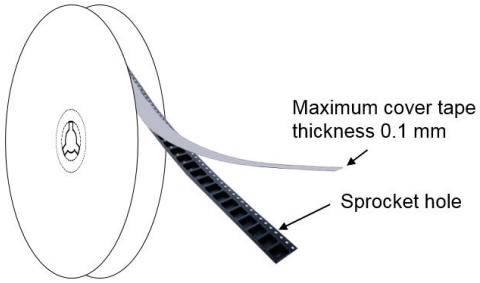


Figure 32. **Reel dimensions (mm)**

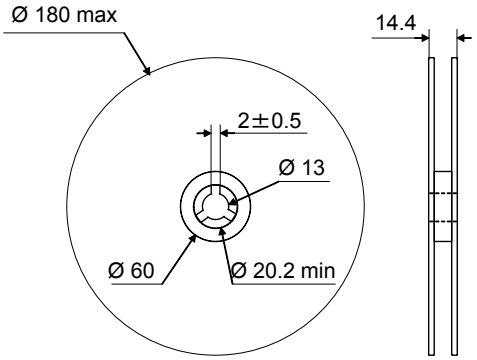


Figure 33. **Inner box dimensions (mm)**

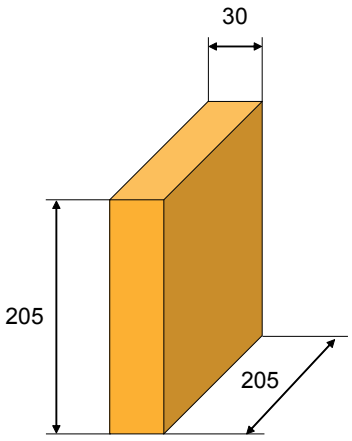
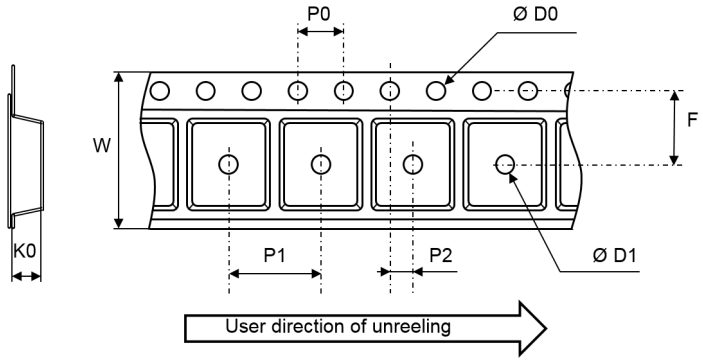


Figure 34. **Tape and reel outline**

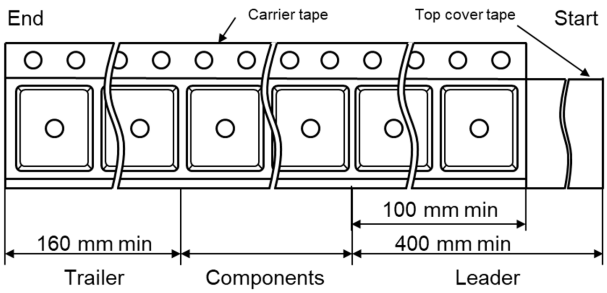


Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 5. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
ØD0	1.45	1.50	1.60
ØD1	0.45	0.50	0.55
F	3.45	3.50	3.55
K0	0.70	0.75	0.80
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.10

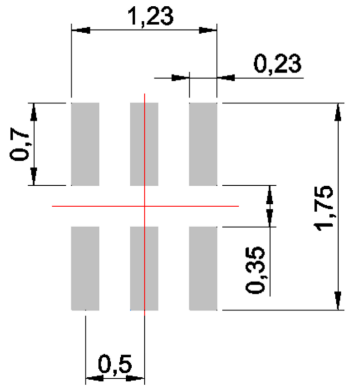
Figure 35. **Tape leader and trailer dimensions**



4 Recommendations on PCB assembly

4.1 Recommended footprint

Figure 36. **Recommended footprint in mm**



Note: Solder Mask Defined (SMD) recommended.

4.2 Stencil opening design

- Stencil opening thickness: 75 µm / 3 mils
- Stencil opening ratio : 90%

Figure 37. **Stencil opening recommendations**

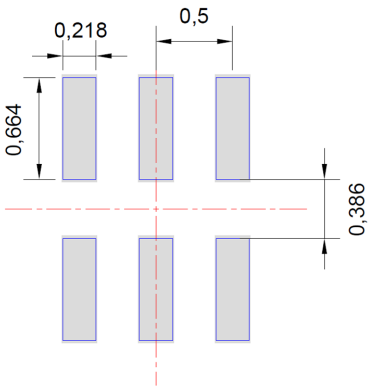


Figure 38. **Wettable flank profile**

4.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

4.4 Placement

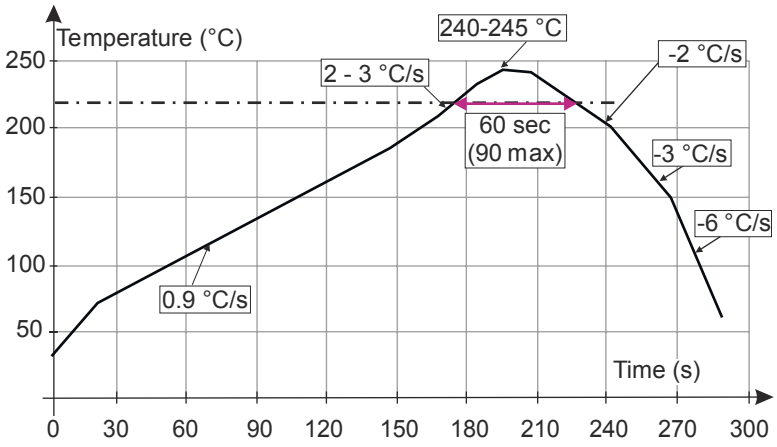
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

4.6 Reflow profile

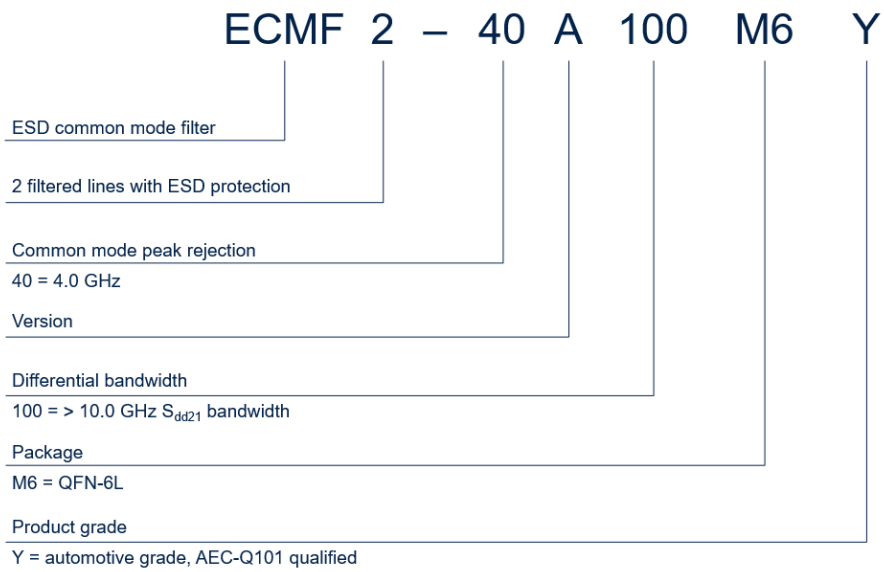
Figure 39. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 40. **Ordering information scheme**



Order code	Marking	Package	Weight	Base qty.	Delivery mode
ECMF2-40A100M6Y	DY(1)	QFN-6L	4.1 mg	3000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly locations.*

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
10-Nov-2023	1	Initial release.
03-Jun-2024	2	Updated *Features*, *Applications*, *Description*, and Table 3. Added Section 1: Pin configuration and function, and Figure 40.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.