



PSMN2R5-80SSE

N-channel 80 V, 2.5 mOhm MOSFET with enhanced SOA in LFPAK88

3 July 2024

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a LFPAK88 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN2R5-80SSE delivers very low R_{DSon} and enhanced safe operating area performance in a high-reliability copper-clip LFPAK88 package.

PSMN2R5-80SSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- LFPAK88 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	225	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	341	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	2	2.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15	4	13.4	31	nC
$Q_{G(tot)}$	total gate charge		58	116	174	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 147\text{ μs}$; Fig. 4	[1]	-	628	mJ

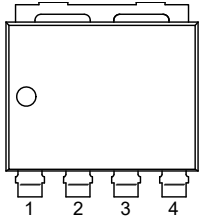
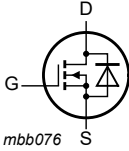
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 18	-	55	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFPAK88 (SOT1235)</p>	
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R5-80SSE	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R5-80SSE	X2E5S80S

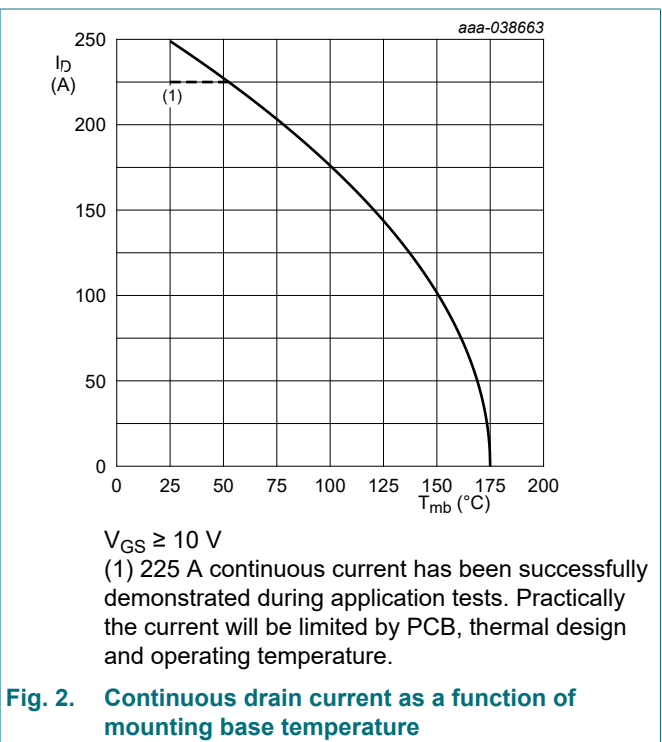
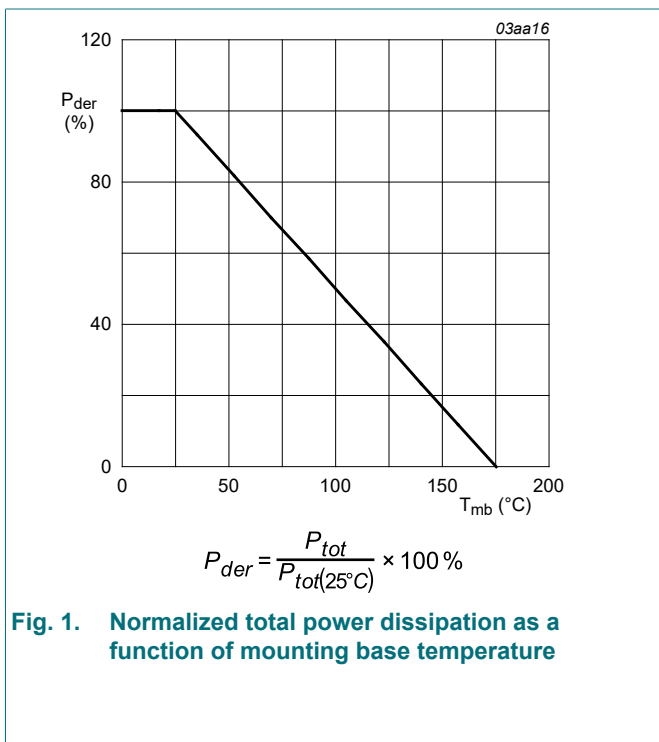
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	341	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	225	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	176	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	996	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	225	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	996	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; $t_p = 147\text{ }\mu\text{s}$; Fig. 4	[1]	-	628 mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[1]	-	82 A

[1] Protected by 100% test



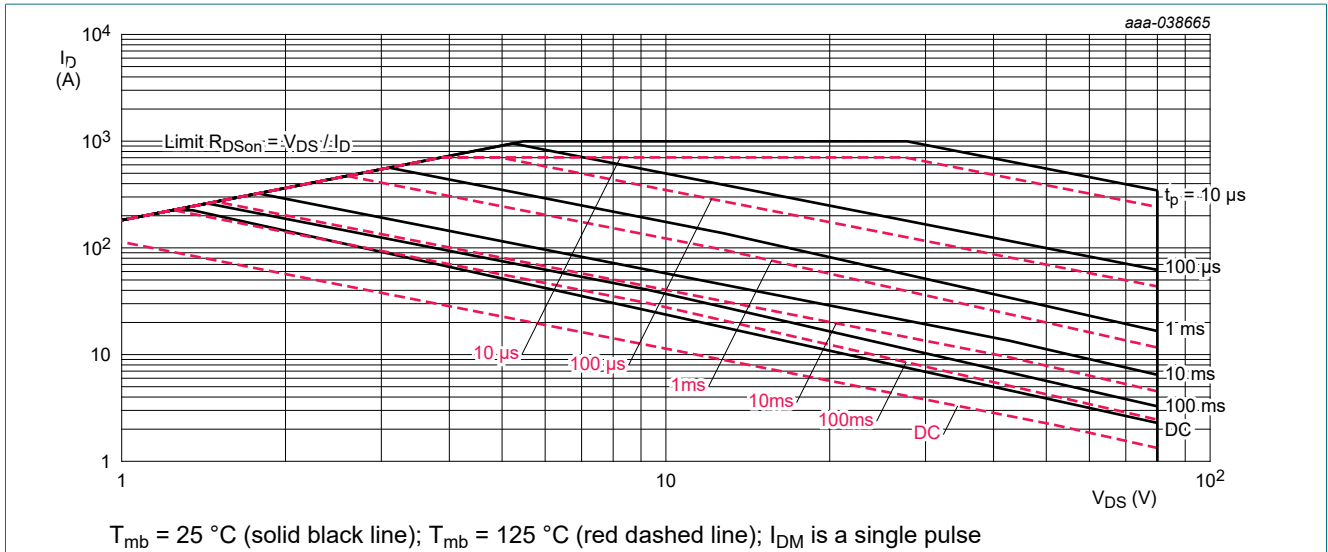


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

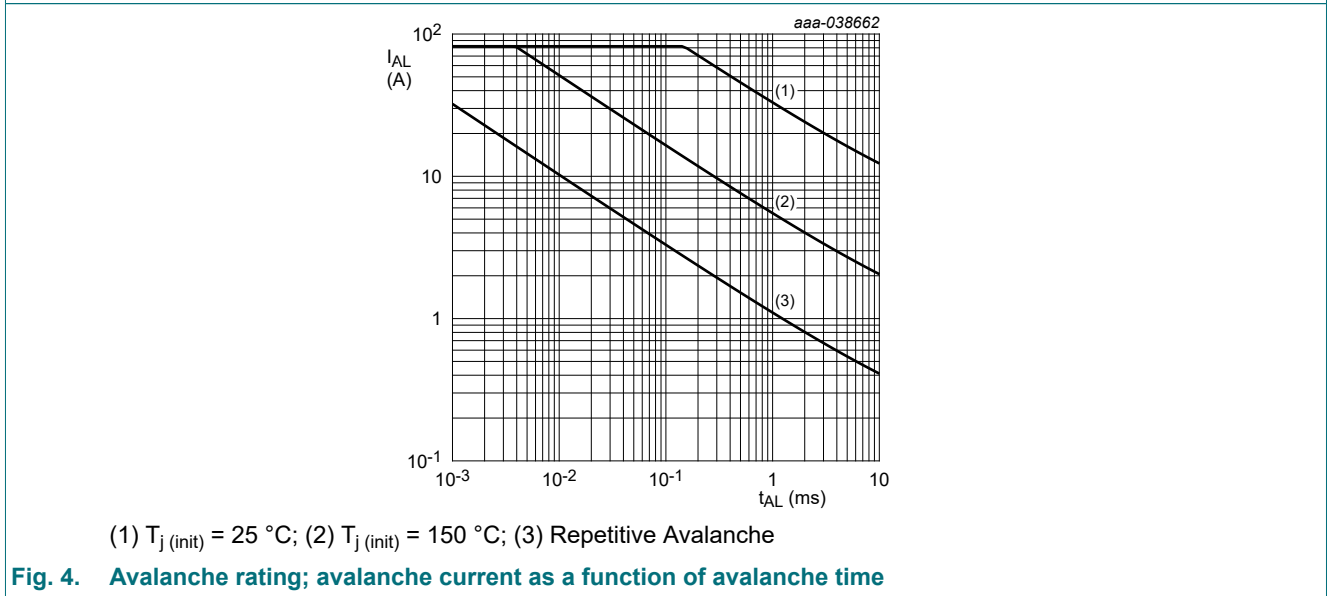


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.32	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	35	-	K/W
		Fig. 7	-	70	-	K/W

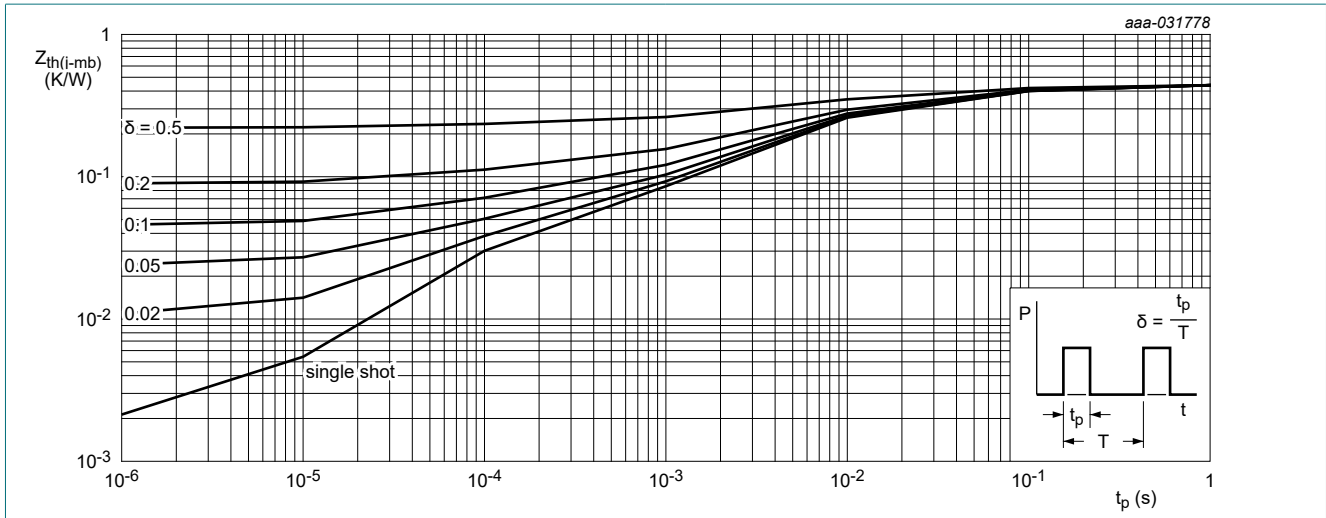


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

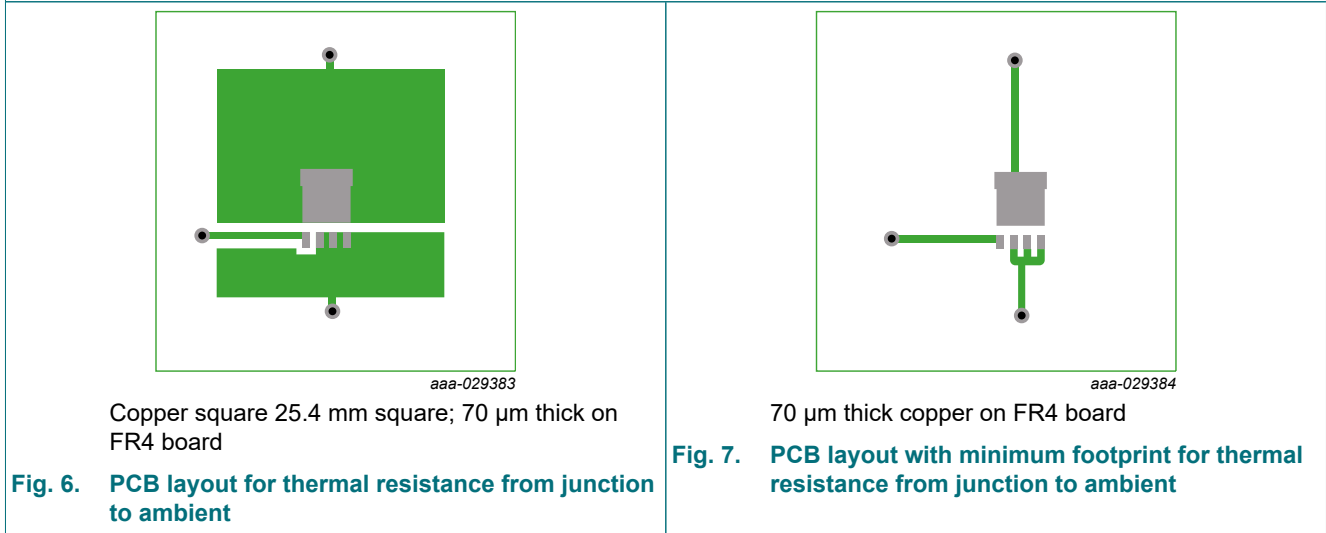


Fig. 6. PCB layout for thermal resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 11	2	2.6	3.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-6.6	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.06	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	20	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.7	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.7	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	2	2.5	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 13	-	2.9	3.8	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 13	-	4.1	5.5	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.6	1.3	2.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 14; Fig. 15	58	116	174	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C$	-	108	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 14; Fig. 15	27	45	63	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	27	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	18	-	nC
Q_{GD}	gate-drain charge		4	13.4	31	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; T_j = 25 \text{ }^\circ C;$ Fig. 14; Fig. 15	-	4.9	-	V
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 0.5 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ Fig. 16	5779	9632	13485	pF
C_{oss}	output capacitance		1505	2509	4014	pF
C_{rss}	reverse transfer capacitance		5	52	156	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	36	-	ns
t_r	rise time		-	32	-	ns
$t_{d(off)}$	turn-off delay time		-	59	-	ns
t_f	fall time		-	43	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C;$ Fig. 17	-	0.8	1	V

N-channel 80 V, 2.5 mOhm MOSFET with enhanced SOA in LPAK88

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	51	-	ns
Q_r	recovered charge	$V_{DS} = 40 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 18	-	55	-	nC

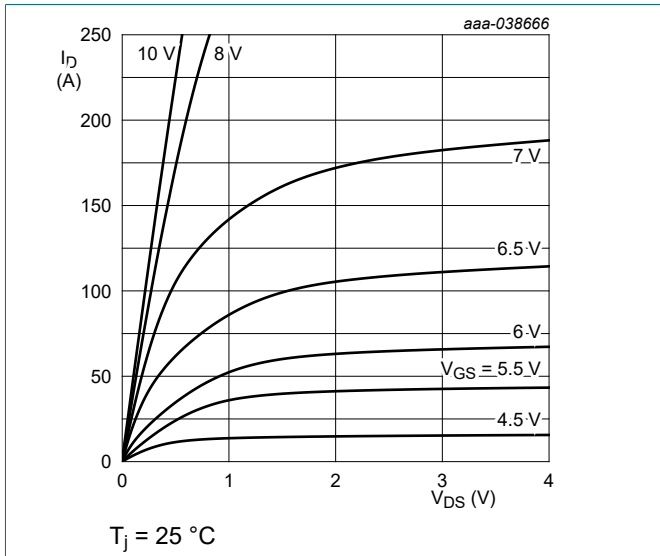


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

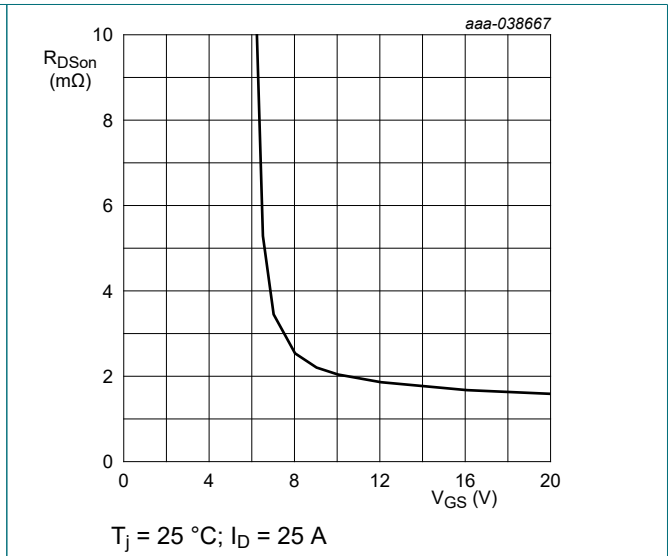


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

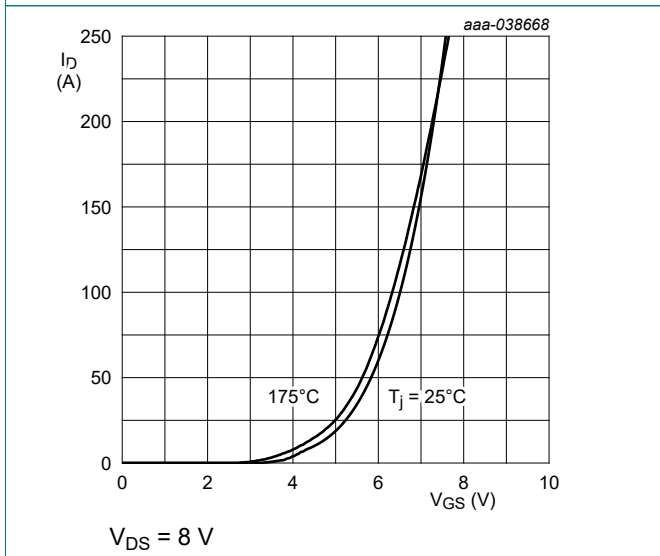


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

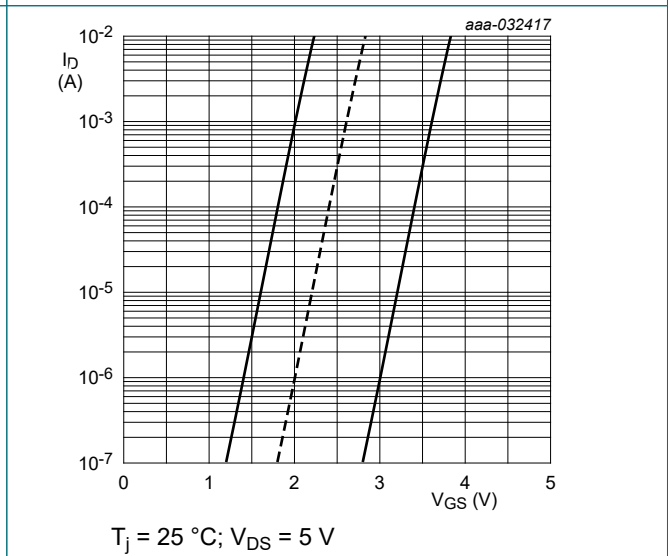


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

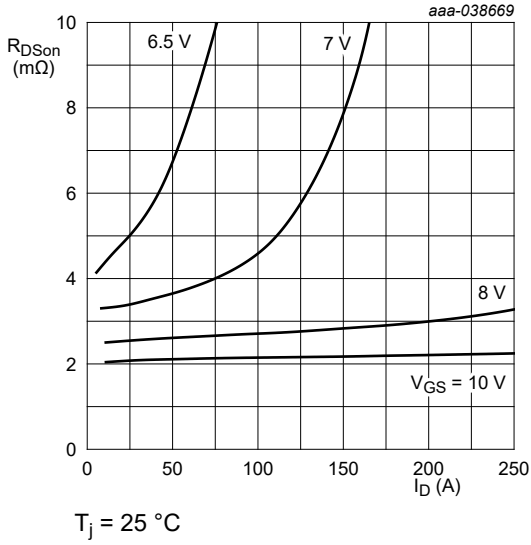
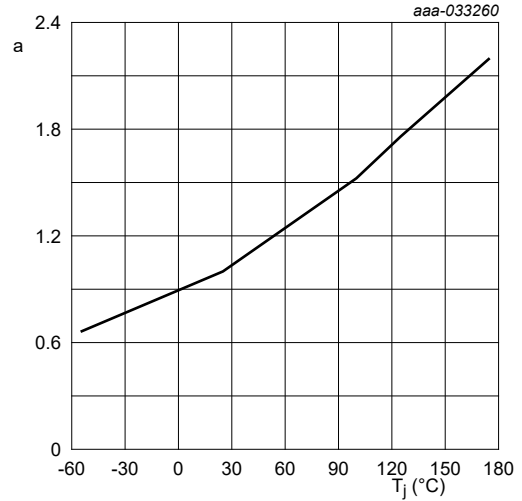


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DS(on)}}{R_{DS(on), (25^\circ\text{C})}}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

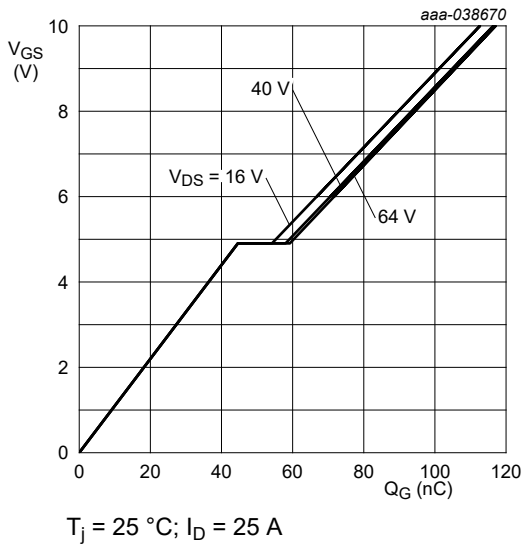


Fig. 14. Gate-source voltage as a function of gate charge; typical values

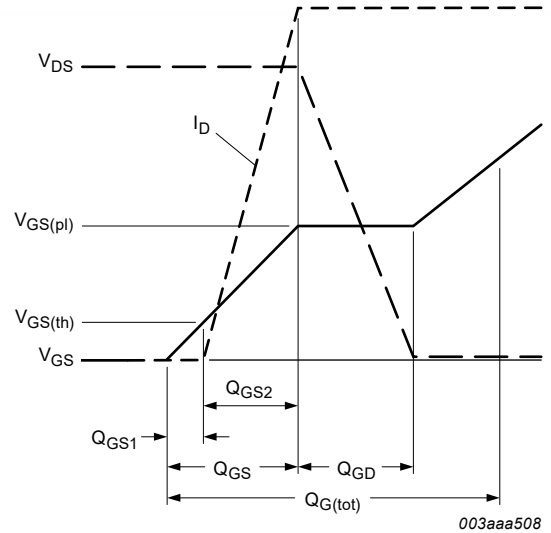


Fig. 15. Gate charge waveform definitions

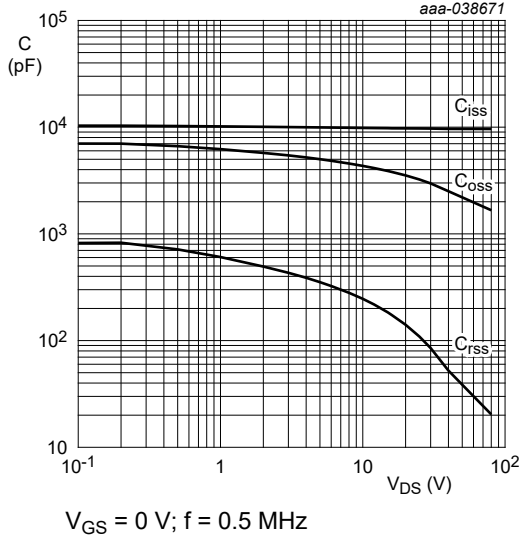


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

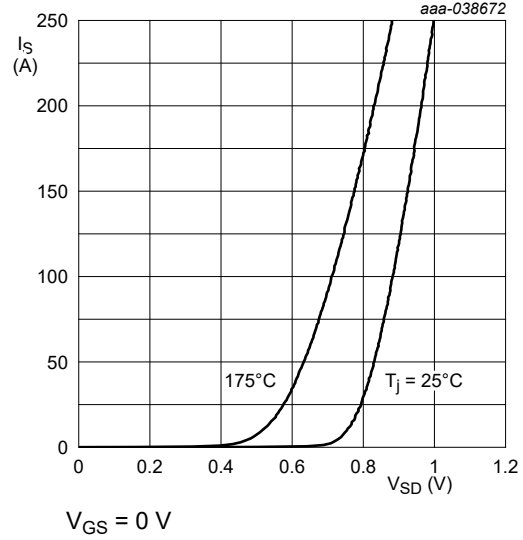


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

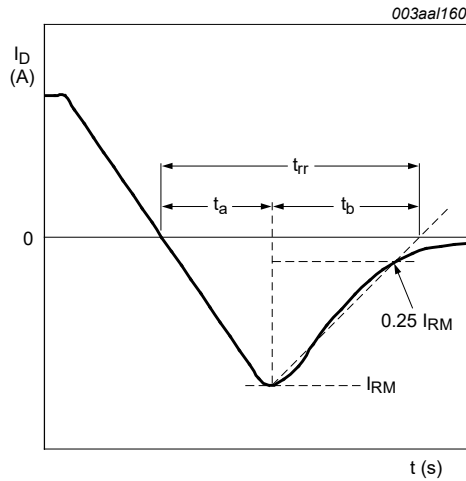


Fig. 18. Reverse recovery timing definition

11. Package outline

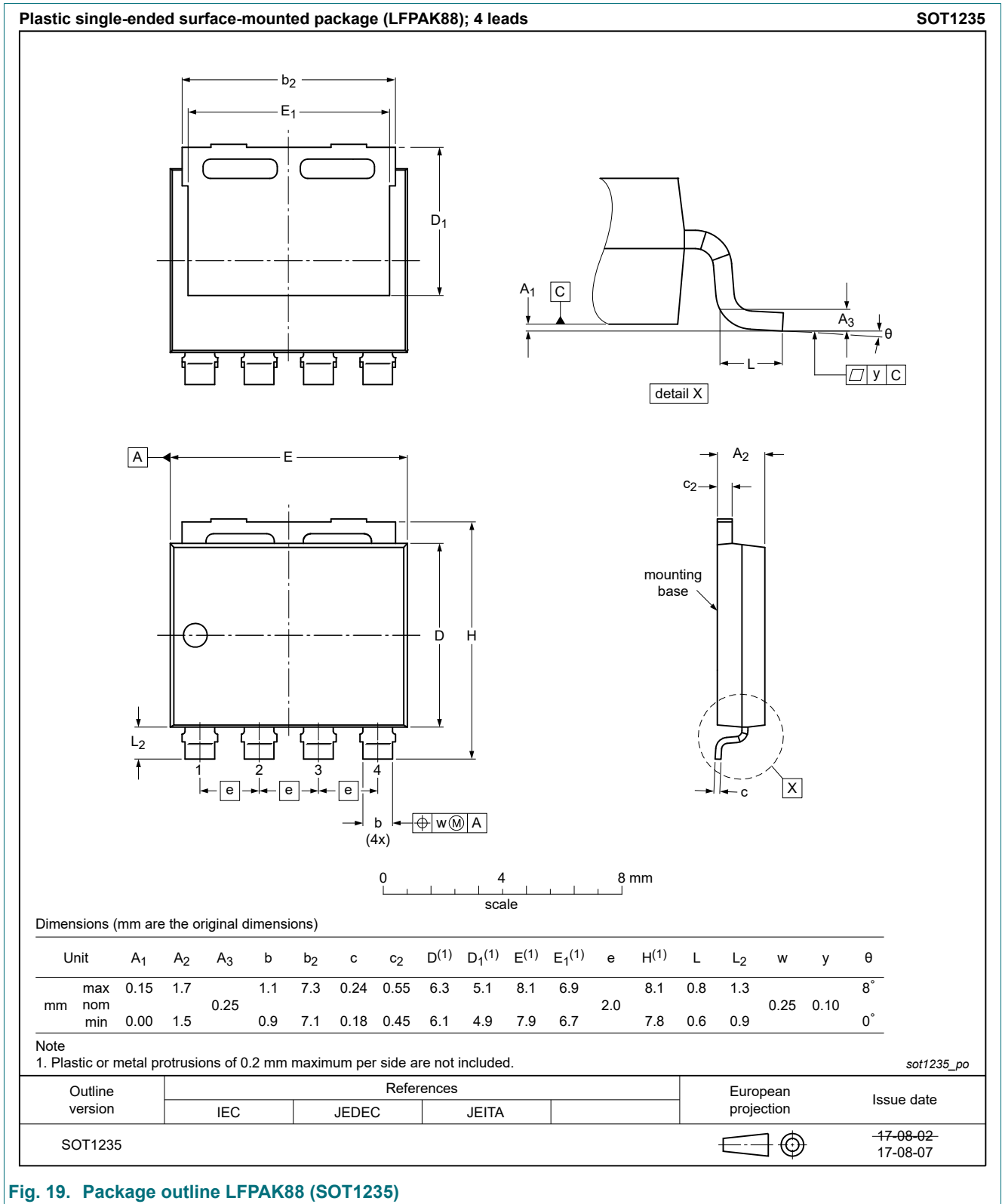


Fig. 19. Package outline LPAK88 (SOT1235)

12. Soldering

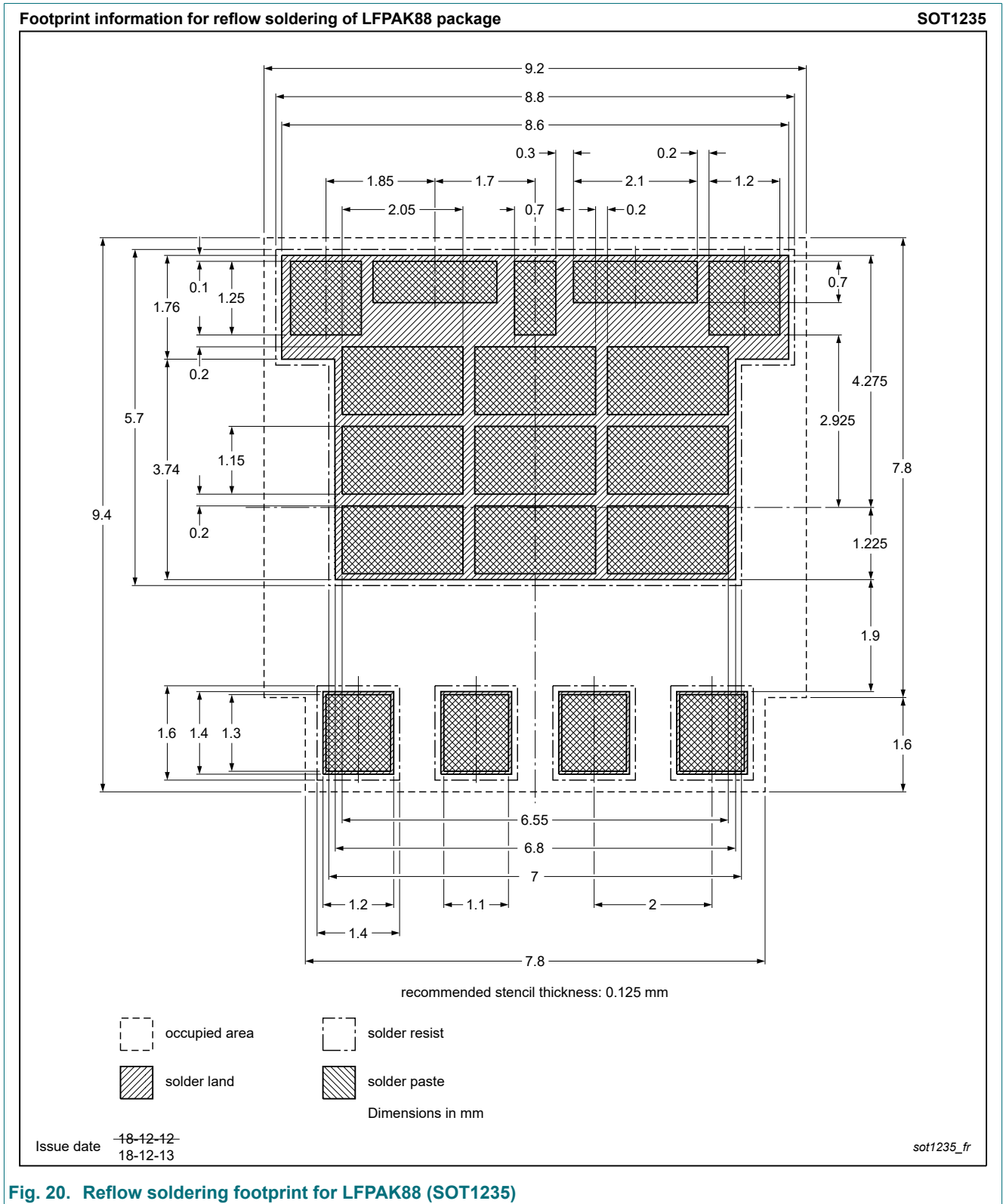


Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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