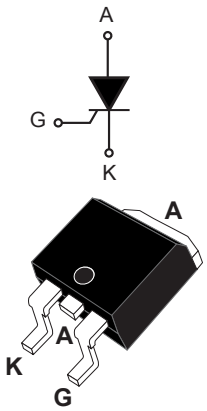
50 A 800 V high temperature SCR thyristors in D²PAK package



D²PAK

Features

- High junction temperature: T_j = 150 °C
- 800 V V_{DRM} / V_{RRM}
- 900 V V_{DSM} / V_{RSM}
- Low I_{GT}: 15 mA
- High static immunity dV/dt = 1000 V/µs at 150 °C
- High turn-on rise dI/dt at 200 A/µs
- Halogen-free molding, lead-free plating
- ECOPACK2 compliant

Application

- Inrush current limiting circuits in AC/DC converters
- General purpose AC line load switching
- Heating resistor control, solid state relays

Product status
TN5015H-8G

Product summary	
Order code	TN5015H-8G
Package	D²PAK
$I_{T(RMS)}$	50 A
V_{DRM}/V_{RRM}	800 V
T_J (max.)	150 °C

Description

Thanks to its junction temperature T_j up to 150 °C, the TN5015H-8G offers high thermal performance operation up to 50 A RMS in a compact D²PAK SMD package.

Its trade-off noise immunity (dV/dt = 1000 V/µs) versus its gate triggering current (I_{GT} = 15 mA) and its turn-on current rise (dI/dt = 200 A/µs) allow to design robust and compact control circuit in AC/DC converters for inrush current limiting circuits and industrial drives, such as overvoltage crowbar protection, motor control circuits and power tools.

1 Characteristics

Table 1. Absolute maximum ratings (limiting values), T_j = 25 °C unless otherwise specified

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180 ° conduction angle)		T_c = 122 °C	50	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)		T_c = 124 °C	30	A
			T_c = 130 °C	25	
			T_c = 135 °C	20	
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25 °C)		t_p = 8.3 ms	550	A
			t_p = 10 ms	500	
I^2t	I^2t value for fusing		t_p = 10 ms	1250	A^2s
dI/dt	I_G = 2 x I_{GT}, tr ≤ 100 ns Critical rate of rise of on-state current		f = 50 Hz	200	A/µs
V_{DRM}/V_{RRM}	Repetitive peak off-state voltage		T_j = 150 °C	800	V
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage		t_p = 10 ms	900	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 150 °C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 150 °C	1	W
V_{RGM}	Maximum peak reverse gate voltage			5	V
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Maximum operating junction temperature			-40 to +150	°C
T_l	Maximum lead temperature soldering during 10 s			260	°C

Table 2. Electrical characteristics (T_j = 25 °C unless otherwise specified)

Symbol	Test conditions			Value	Unit
I_{GT}	V_D = 12 V, R_L = 33 Ω		Min.	5	mA
			Max.	15	
V_{GT}			Max.	1.3	V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ	T_j = 150 °C	Min.	0.2	V
I_H	I_T = 500 mA, gate open		Max.	50	mA
I_L	I_G = 1.2 x I_{GT}		Max.	70	mA
dV/dt	V_D = 536 V, gate open	T_j = 150 °C	Min.	1000	V/µs
t_{gt}	I_{TM} = 100 A, V_D = 536 V, I_G = 30 mA, (dI_G/dt) max = 0.2 A/µs		Typ.	1.9	µs
t_q	I_T = 100 A, V_D = 536 V, V_R = 25 V, dV_D/dt = 40 V/µs	T_j = 125 °C	Typ.	70	µs
		T_j = 150 °C	Typ.	85	µs

Table 3. Static characteristics

Symbol	Test conditions			Value	Unit
V_{TM}	I_{TM} = 100 A, t_p = 380 µs	T_j = 25 °C	Max.	1.55	V
V_{TO}	Threshold voltage	T_j = 150 °C	Max.	0.85	
R_D	Dynamic resistance	T_j = 150 °C	Max.	8	mΩ
I_{DRM}, I_{RRM}	V_D = V_{DRM} = V_{RRM}	T_j = 25 °C	Max.	2.5	µA
		T_j = 150 °C		12	mA

Table 4. Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Max.	0.6	°C/W
$R_{th(j-a)}$	Junction to ambient, S = 2.5 cm²(1), E_{CU} = 70 µm	Typ.	45	

1. *Copper surface under tab, on PCB FR4.*

1.1 Characteristics curves

Figure 1. Maximum average power dissipation versus average on-state current

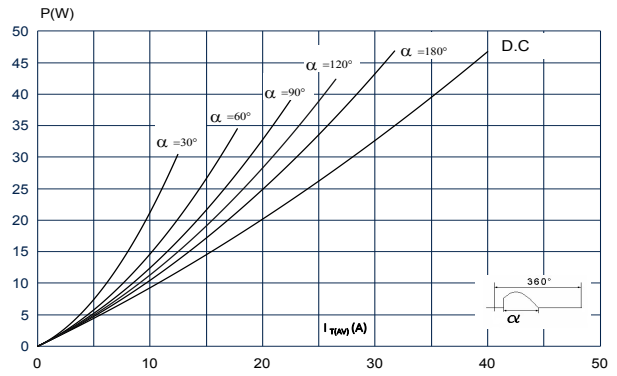


Figure 2. Average and DC on-state current versus case temperature

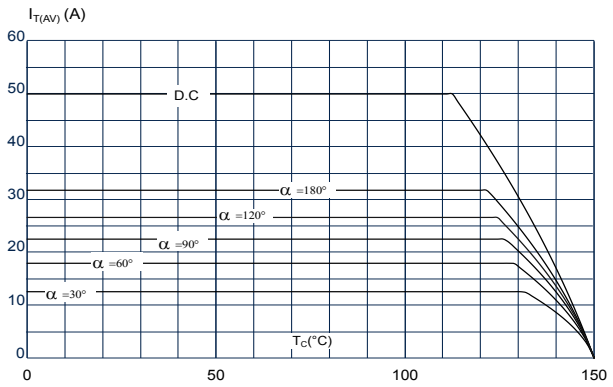


Figure 3. Average and D.C. on state current versus ambient temperature

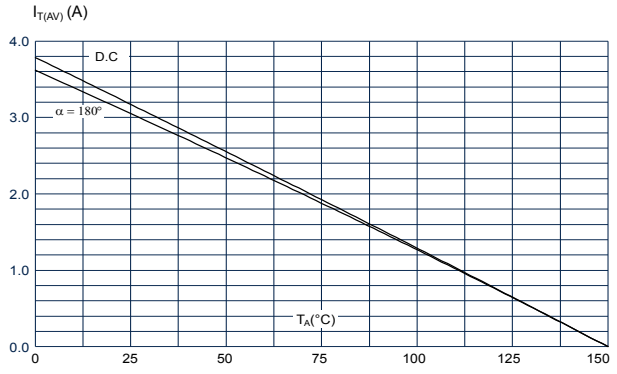


Figure 4. Relative variation of thermal impedance junction to case and junction to ambiant versus pulse duration

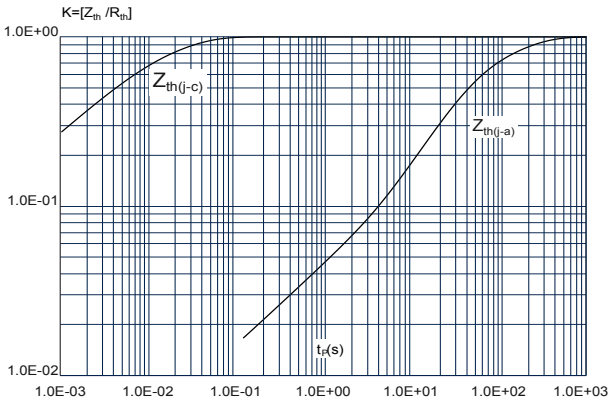


Figure 5. Relative variation of gate trigger current and gate voltage versus junction temperature

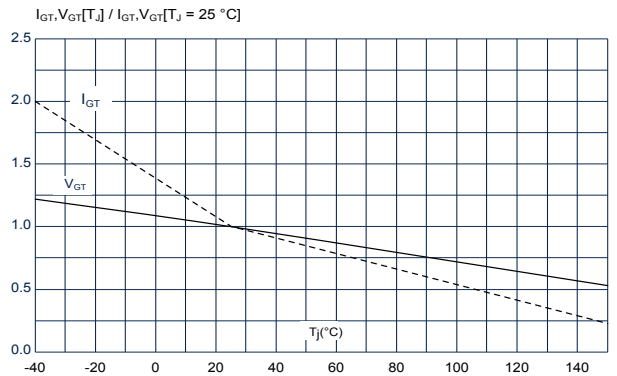


Figure 6. Relative variation of holding and latching current versus junction temperature

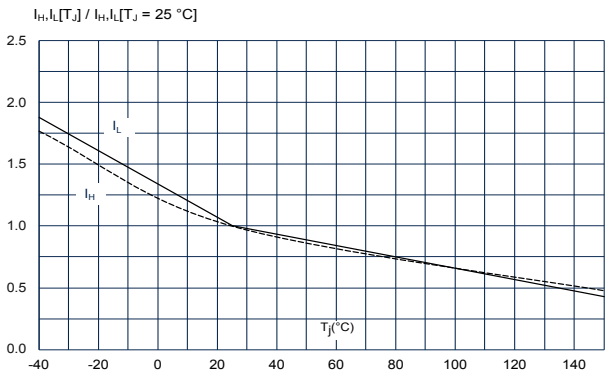


Figure 7. Relative variation of static dV/dt immunity versus junction temperature

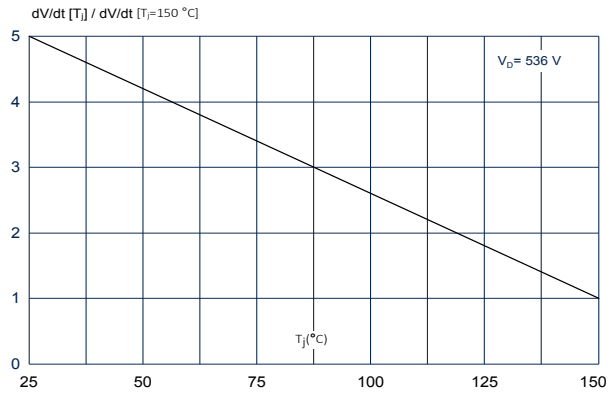


Figure 8. Surge peak on-state current versus number of cycles

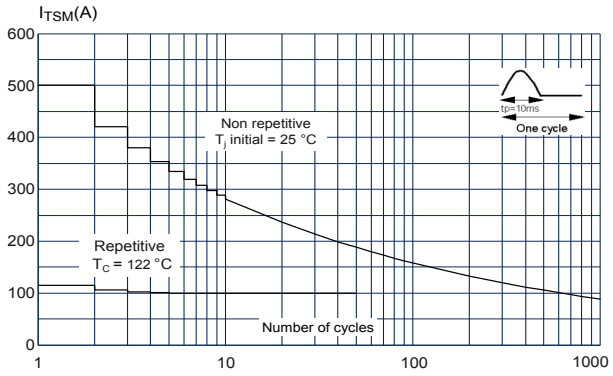


Figure 9. Non repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms

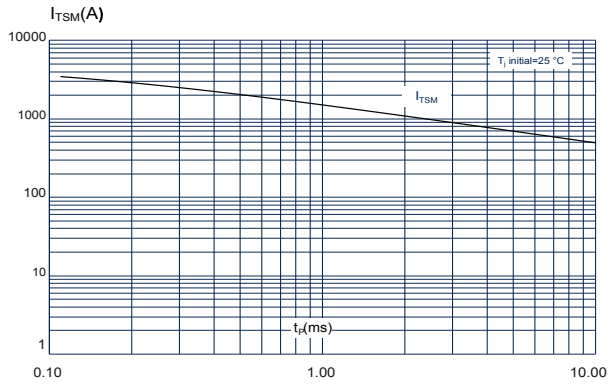


Figure 10. On-state characteristics (maximum values)

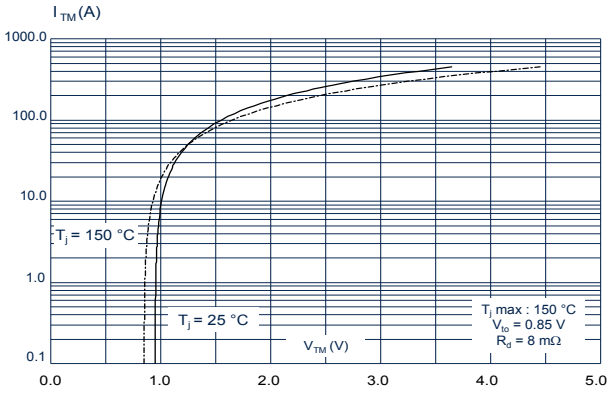


Figure 11. Relative variation of leakage current versus junction temperature

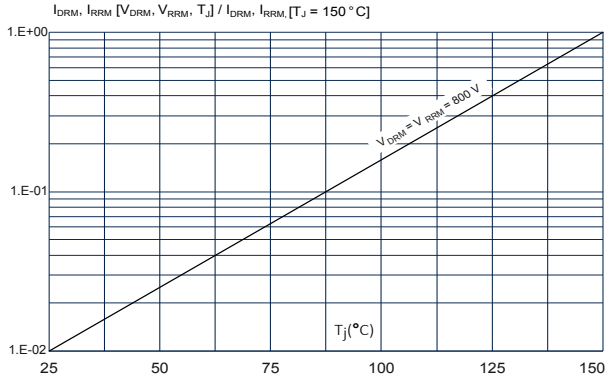


Figure 12. Thermal resistance junction to ambient versus copper surface under tab

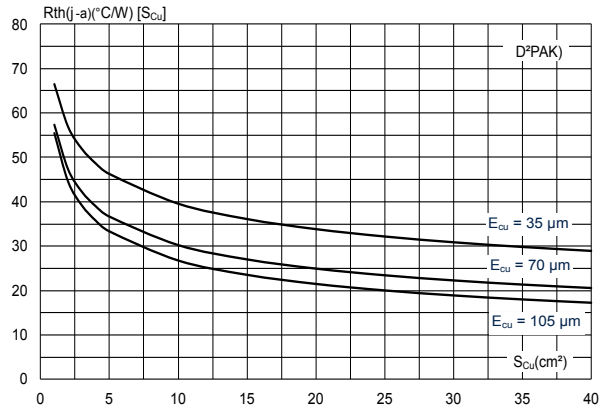
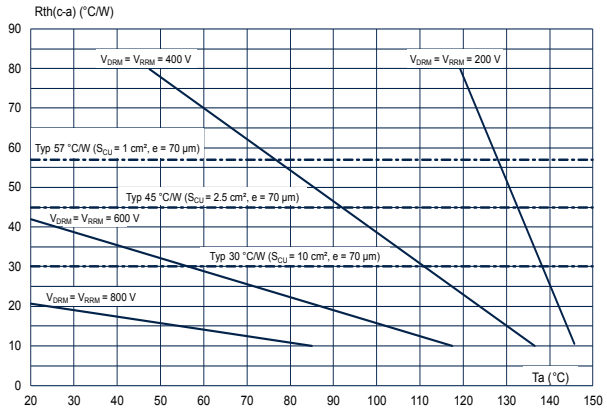


Figure 13. Recommended maximum case-to-ambient thermal resistance versus ambient temperature for different peak off-state voltages



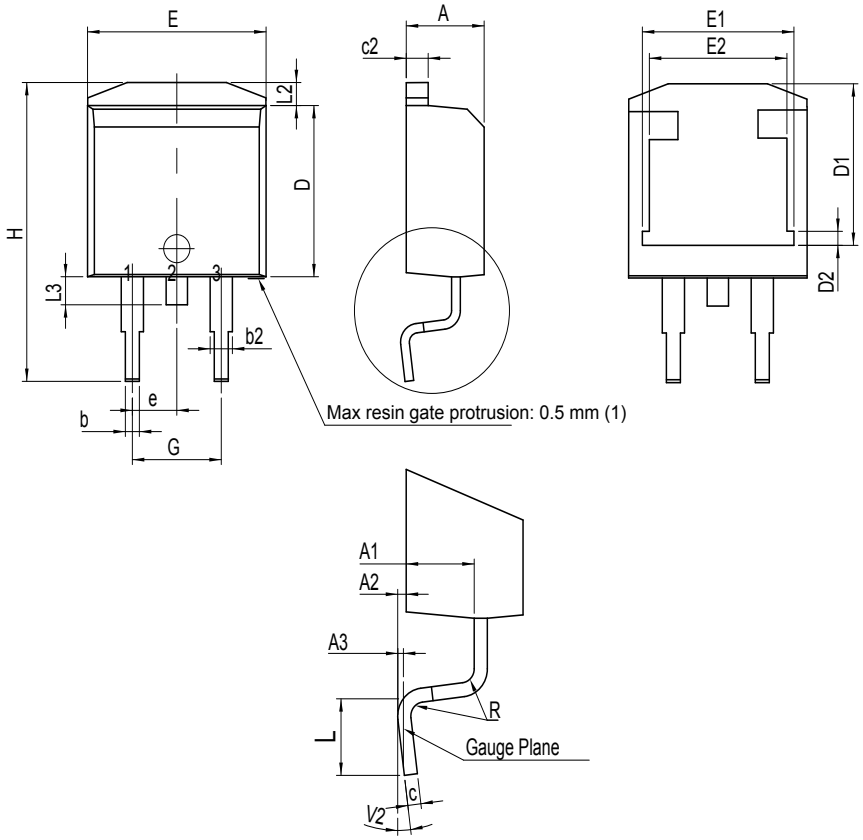
2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 D²PAK package information

- ECOPACK2 compliant
- Lead-free package leads finishing
- Molding compound resin is halogen-free and meets UL94 flammability standard level V0

Figure 14. D²PAK package outline



(1) Resin gate is accepted in each of position shown on the drawing, or their symmetrical.

Table 5. D²PAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.60	0.1693		0.1811
A1	2.49		2.69	0.0980		0.1059
A2	0.03		0.23	0.0012		0.0091
A3		0.25			0.0098	
b	0.70		0.93	0.0276		0.0366
b2	1.25		1.7	0.0492		0.0669
c	0.45		0.60	0.0177		0.0236
c2	1.21		1.36	0.0476		0.0535
D	8.95		9.35	0.3524		0.3681
D1	7.50		8.00	0.2953		0.3150
D2	1.30		1.70	0.0512		0.0669
e		2.54			0.1000	
E	10.00		10.28	0.3937		0.4047
E1	8.30		8.70	0.3268		0.3425
E2	6.85		7.25	0.2697		0.2854
G	4.88		5.28	0.1921		0.2079
H	15		15.85	0.5906		0.6240
L	1.78		2.28	0.0701		0.0898
L2	1.19		1.40	0.0468		0.0551
L3	1.40		1.75	0.0551		0.0689
R		0.40			0.0157	
V2[2]	0°		8°	0°		8°

1. *Dimensions in inches are given for reference only*
2. *Degrees*

Figure 15. D²PAK recommended footprint (dimensions are in mm)

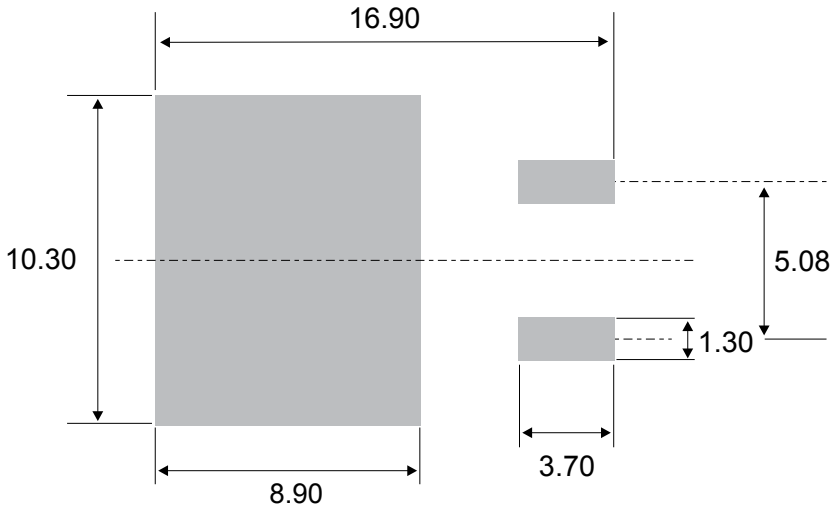
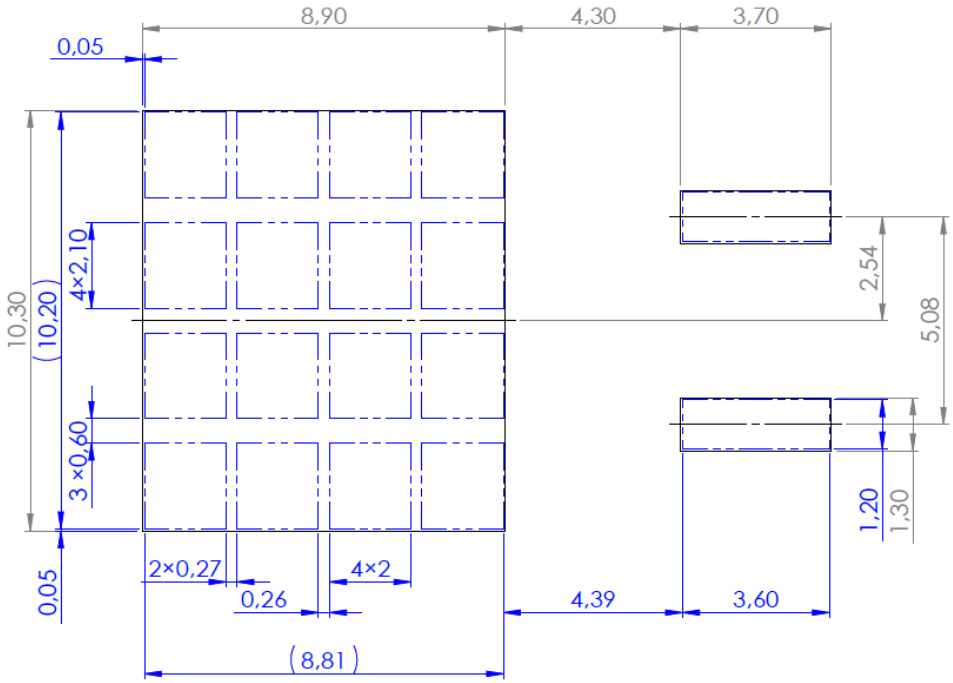


Figure 16. D²PAK stencil definitions (dimensions are in mm)



3 Ordering information

Figure 17. **Ordering information scheme**

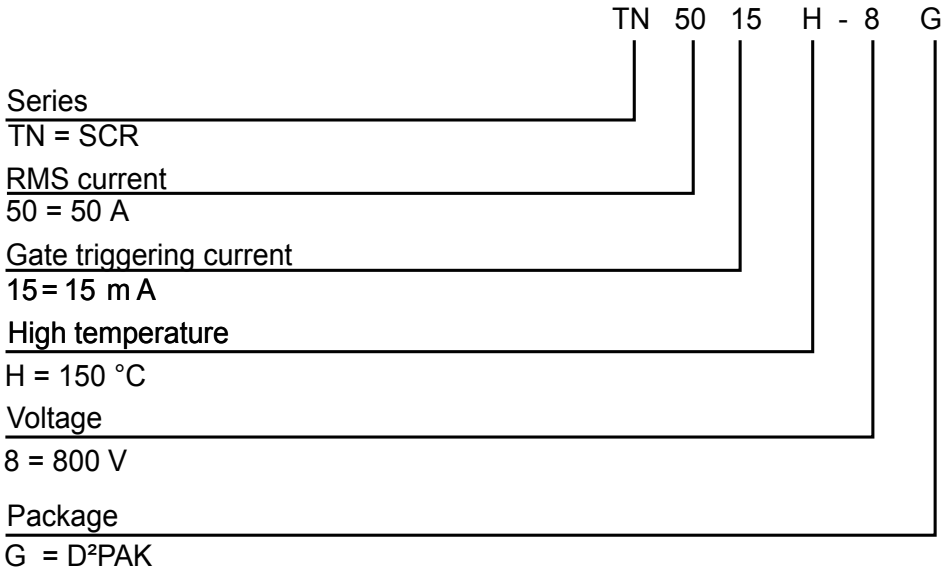


Table 6. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN5015H-8G	TN5015H8G	D²PAK	1.38 g	1000	Tape and reel

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
26-Oct-2023	1	Initial release.
30-Apr-2024	2	Updated Table 3, and Figure 13.

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