



Features

- $V_{DS(V)} = 60V$
- $I_{D\ MAX} = 80A$
- $R_{DS(on)} < 7.5m\Omega$ @ $V_{GS}=10V$
- $R_{DS(on)} < 9.5m\Omega$ @ $V_{GS}=4.5V$
- Packaging-PDFN5 × 6-8

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	+20	
Continuous Drain Current	$T_C = 25^\circ C$	I_D	80	A
	$T_C = 100^\circ C$		51	
	$T_A = 25^\circ C$		10	
	$T_A = 100^\circ C$		8	
Diode Continuous Forward Current	$T_C = 25^\circ C$	I_S	25	mJ
Avalanche Current, Single pulse (L=0.5mH) (Note 2)		I_{AS}	20	
Avalanche Energy, Single pulse (L=0.5mH) (Note 2)		E_{AS}	100	
Power Dissipation	$T_C = 25^\circ C$	P_D	52	W
	$T_C = 100^\circ C$		20.8	
	$T_A = 25^\circ C$		2	
	$T_A = 100^\circ C$		1.3	
Thermal Resistance. Junction- to-Case	Steady State	$R_{\theta JC}$	2.4	$^\circ C/W$
Thermal Resistance. Junction- to-Ambient (Note 3)	$t \leq 10s$	$R_{\theta JA}$	25	
Thermal Resistance. Junction- to-Case (Note 3)	Steady State		60	
Junction Temperature		T_J	1450	$^\circ C$
Storage Temperature Range		T_{stg}	-55 to 150	

Notes:

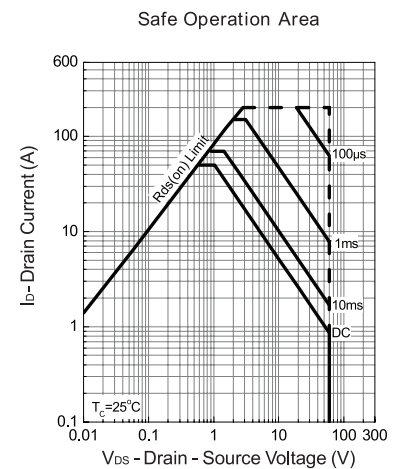
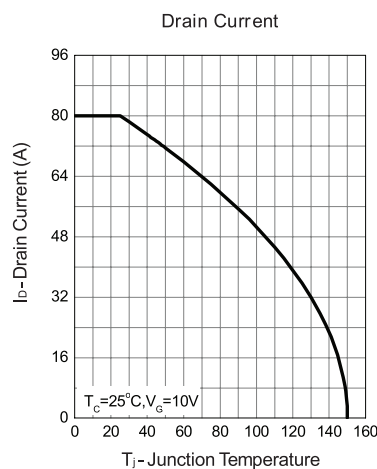
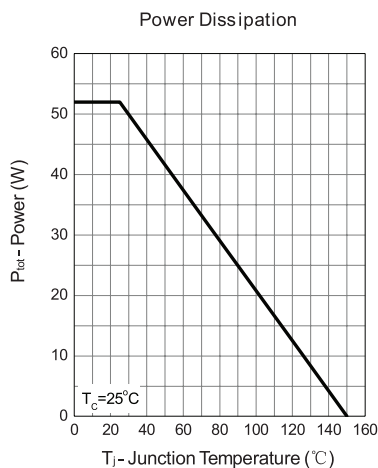
1. Pulse width limited by max. junction temperature.
2. UIS tested and pulse width limited by maximum junction temperature $150^\circ C$ (initial temperature $T_J=25^\circ C$).
3. Surface Mounted on $1in^2$ pad area.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

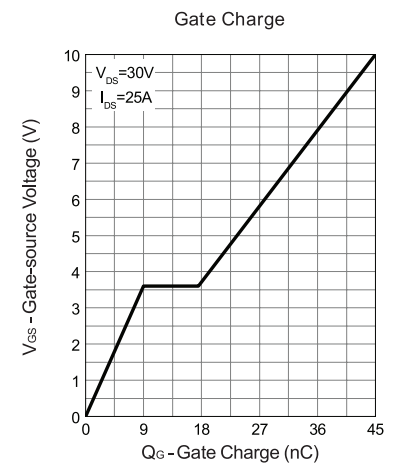
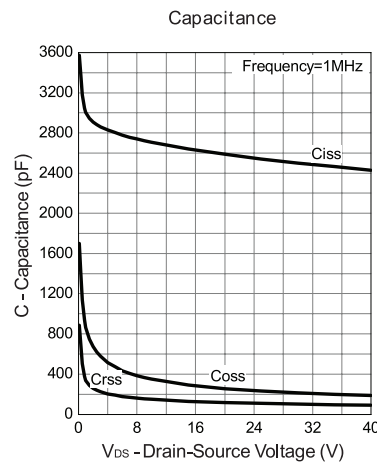
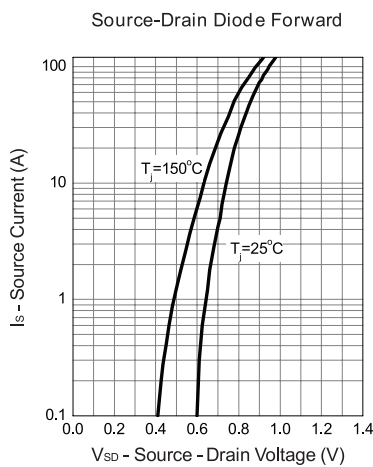
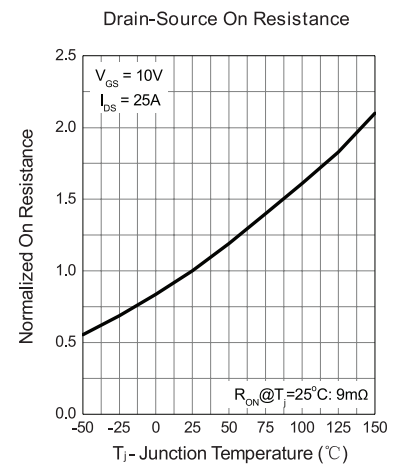
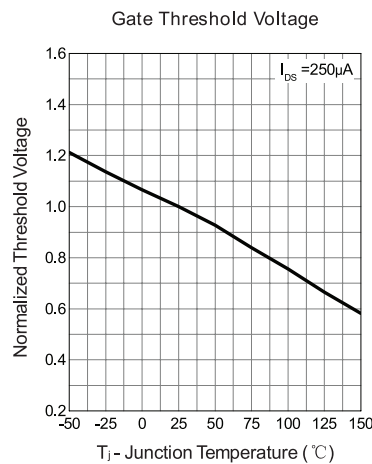
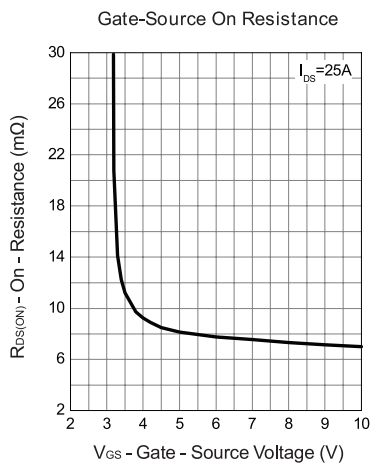
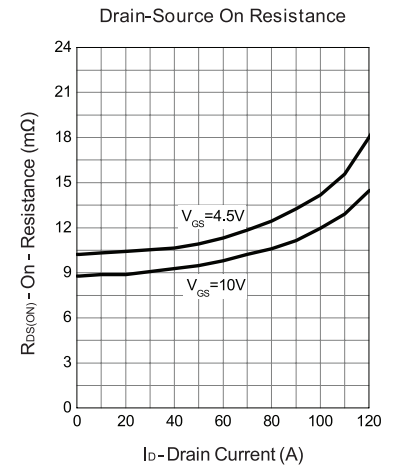
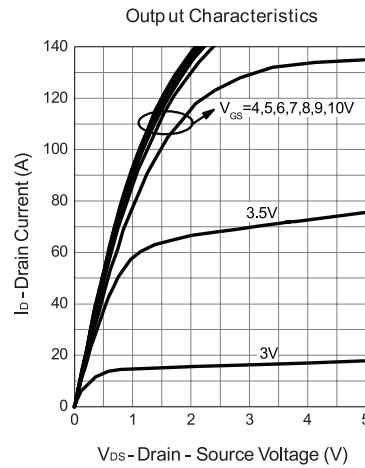
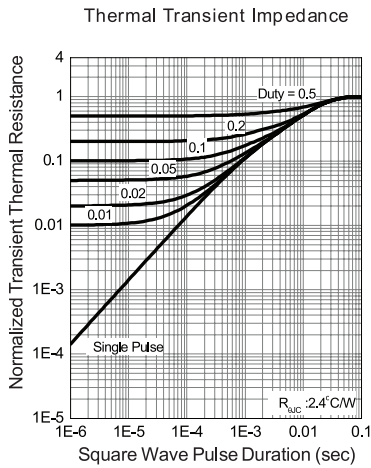
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-48V, V _{GS} =0V			1	μA
		V _{DS} =-48V, V _{GS} =0V, T _J = 85°C			30	
Gate to Source Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.1		2.1	V
Static Drain-Source On-Resistance (Note 4)	R _{DS(on)}	V _{GS} =10V, I _D =25A			7.5	mΩ
		V _{GS} =-4.5V, I _D =6A			9.5	
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =30V, f=1MHz		2500		pF
Output Capacitance	C _{oss}			215		
Reverse Transfer Capacitance	C _{rss}			1.5		
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		1		Ω
Total Gate Charge	Q _g	V _{GS} =10V, V _{DD} =30V, I _D =25A		45		nC
Gate Source Charge	Q _{gs}			9		
Gate Drain Charge	Q _{gd}			8.5		
Turn-On DelayTime	t _{d(on)}	V _{DD} = 30V, R _L = 30Ω, I _{DS} =1A I _{GEN} = 10A, R _G = 6Ω		20		nS
Turn-On Rise Time	t _r			9		
Turn-Off DelayTime	t _{d(off)}			55		
Turn-Off Fall Time	t _f			20		
Body Diode Reverse Recovery Time	t _{rr}	I _F = 25A, dI/dt = 100 A/μs		28		nS
Body Diode Reverse Recovery Charge	Q _{rr}			30		nC
Diode Forward Voltage	V _{SD}	V _{SD} = 25A, V _{GS} = 0V			13	V

Notes 4: Pulse test ; pulse width≤300μs, duty cycle≤2%.

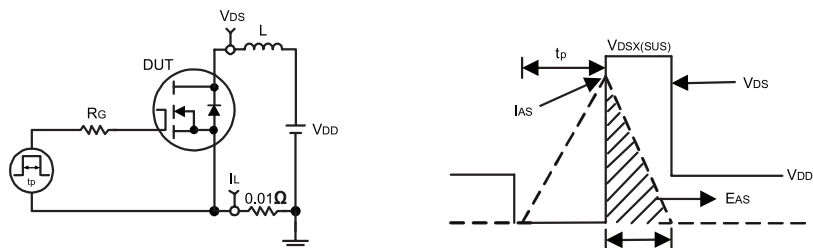
Typical Characteristics



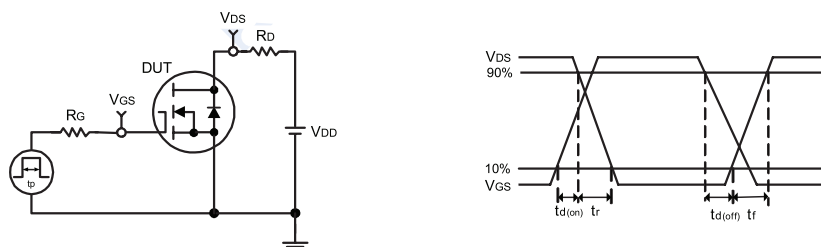
Typical Characteristics



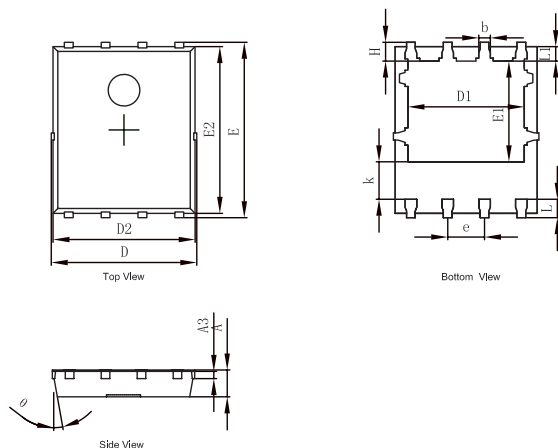
Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms

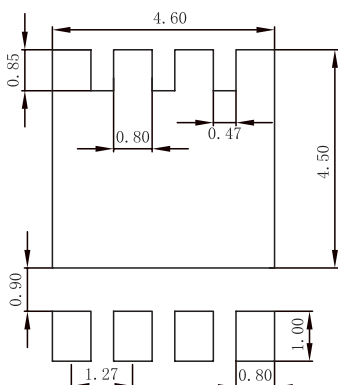


Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

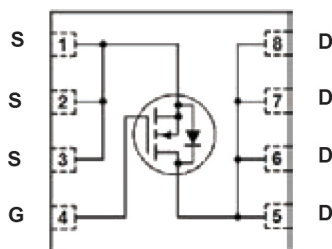
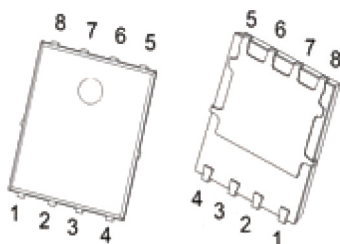
Suggested Pad Layout



Notes

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only.

Diagram



Part Number Table

Description	Part Number
N Channel MOSFET, 80A, 60V	2KK5115DFN

Dimensions : Millimetres

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