

N Channel MOSFET

multicomp^{PRO}

RoHS
Compliant



Features

- $V_{DS(V)} = 150V$
- $I_D = 65A$
- $R_{DS(on)}$ (at $V_{GS} = 10V$) $< 9.9m\Omega$
- SGT MOSFET
- Superior UIS performance
- 100% UIS tested
- Very low on-resistance

Absolute Maximum Ratings (TA = 25°C unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	+20	
Continuous Drain Current ^A	$T_C = 25^\circ C$	I_D	65	A
	$T_C = 100^\circ C$		41	
Pulsed Drain Current ^B		I_{DM}	260	
Single Pulse Avalanche Energy ^C		E_{AS}	324	mJ
Power Dissipation		P_D	104	W
Thermal Resistance, Junction- to-Ambient ^D		$R_{\theta JA}$	45	mJ
Thermal Resistance, Junction- to-Case		$R_{\theta JC}$	1.2	°C/W
Storage Temperature Range		T_{stg}	-55 to 150	°C

Notes:

A. The max drain current rating is silicon limited

B. Repetitive Rating: Pulse width limited by maximum junction temperature

C. L = 0.5 mH, $V_{DD} = 50V$, $I_{AS} = 36A$, $R_G = 25\Omega$, Starting $T_J = 25^\circ C$

D. Mount on minimum PCB layout

Electrical Characteristics (TJ = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -250\mu A$, $V_{GS} = 0V$	150			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -150V$, $V_{GS} = 0V$			1	μA
Gate to Source Leakage Current	I_{GSS}	$V_{DS} = 0V$, $V_{GS} = \pm 20V$			± 100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = 20A$		8	9.9	m Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 75V$, $F = 1MHz$		3690		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			15		
Gate Resistance	R_G	$F = 1MHz$		1.2		Ω

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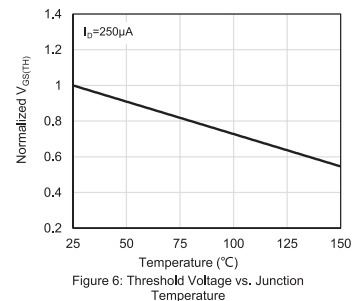
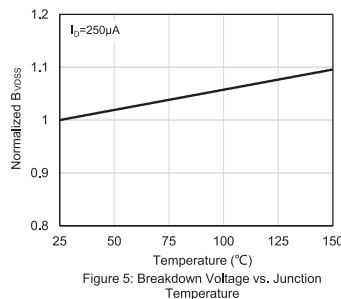
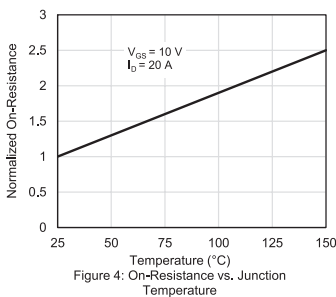
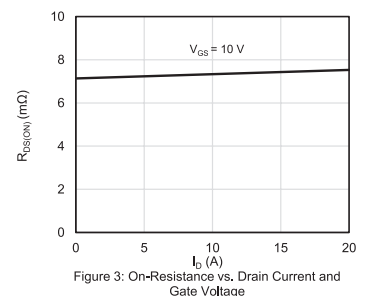
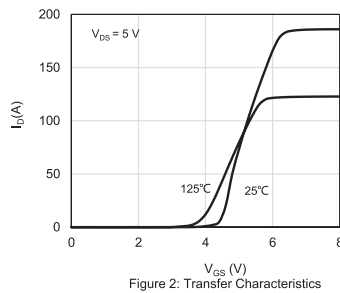
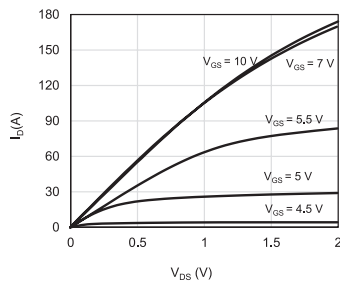
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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Characteristics						
Total Gate Charge	Q _g	V _{DD} =75V, I _D =20A V _{GS} =10V,		51		nC
Gate Source Charge	Q _{gs}			18		
Gate Drain Charge	Q _{gd}			10		
Turn-On DelayTime	t _{d(on)}	V _{DD} = 75V, R _L = 3.8Ω, V _{GS} = 10V, R _G = 6.8Ω		23		nS
Turn-On Rise Time	t _r			40		
Turn-Off DelayTime	t _{d(off)}			48		
Turn-Off Fall Time	t _f			22		
Drain-Source Diode Characteristics and Maximum Ratings						
Body Diode Reverse Recovery Time	t _{rr}	V _{DD} = 75V, I _F = 20A dI/dt = 100 A/μs,		86		nS
Body Diode Reverse Recovery Charge	Q _{rr}			265		nC
Peak Reverse Recovery Current	I _{RRM}			5		
Maximum Body-Diode Continuous Current	I _S				65	
Maximum Body-Diode Current (Pulsed)	I _{SM}				260	
Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1A		0.68		V

Notes:

1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Typical Characteristics



Typical Characteristics

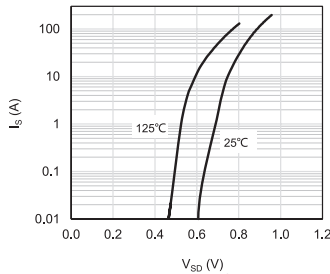


Figure 7: Body-Diode Characteristics

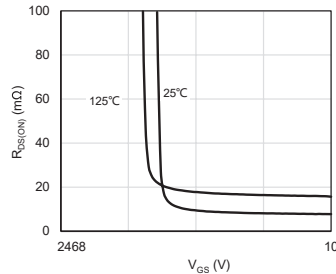


Figure 8: On-Resistance vs. Gate-Source Voltage

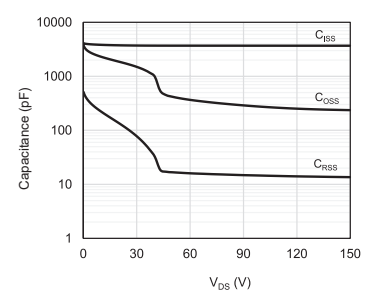


Figure 9: Capacitance Characteristics

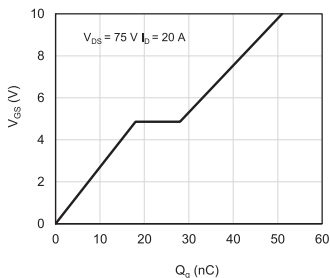


Figure 10: Gate-Charge Characteristics

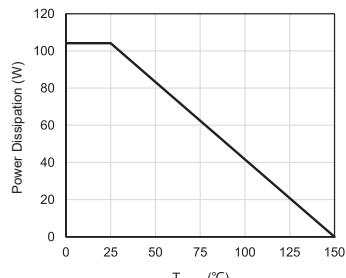


Figure 11: Power De-rating

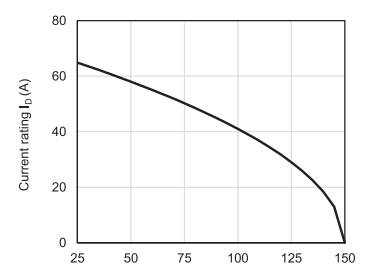


Figure 12: Current De-rating

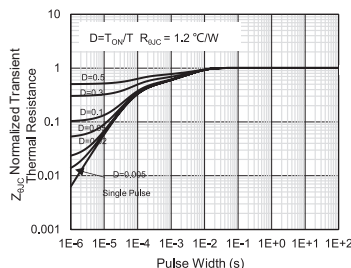


Figure 13: Normalized Maximum Transient Thermal Impedance

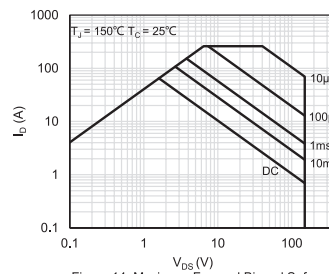
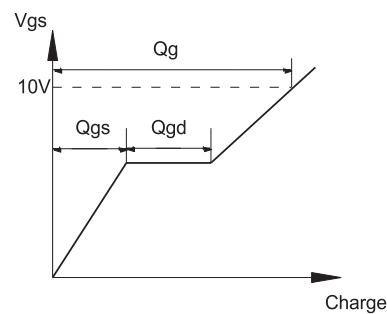
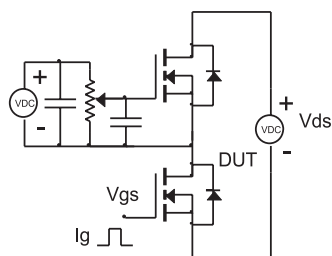


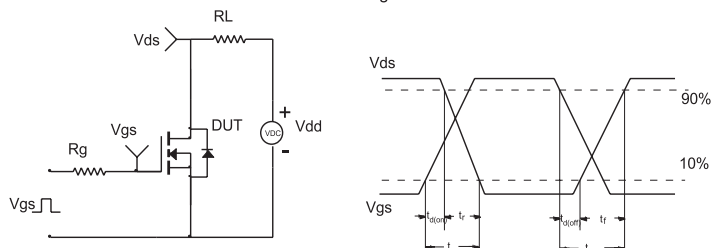
Figure 14: Maximum Forward Biased Safe Operating Area

Test Circuit and Waveform

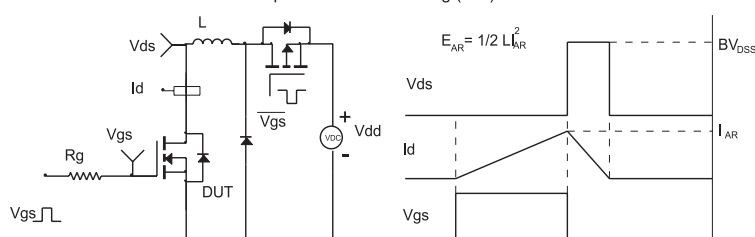
Gate Charge Test Circuit & Waveform



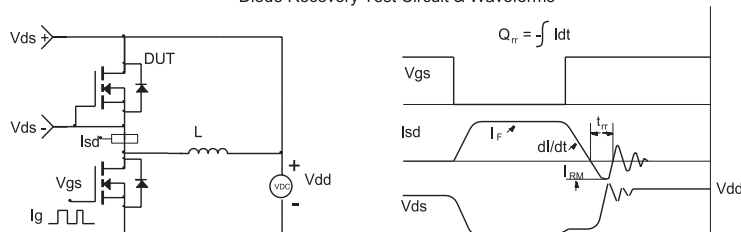
Resistive Switching Test Circuit & Waveforms



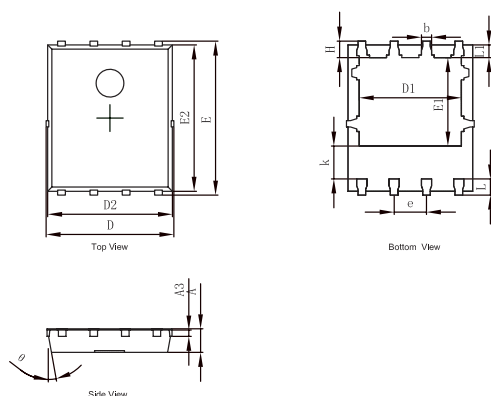
Undamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

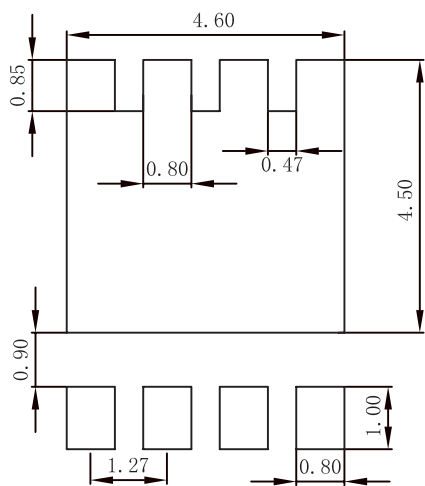


Package Outline Dimensions



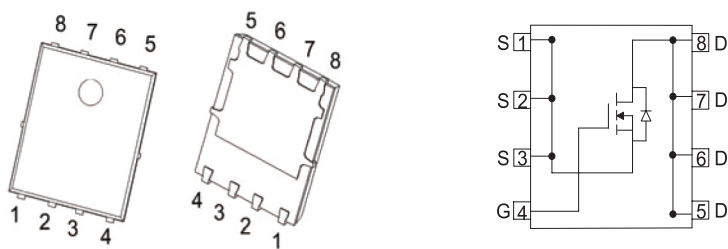
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

Suggested Pad Layout



- Notes**
- 1. Controlling dimension: in millimeters.
 - 2. General tolerance: $\pm 0.05\text{mm}$
 - 3. The pad layout is for reference purposes only.

Diagram



Dimensions : Millimetres

Part Number Table

Description	Part Number
N Channel MOSFET, 65A, 150V	2KK6040DFN

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