

MOSFETs Silicon N-Channel MOS

SSM3K56ACT

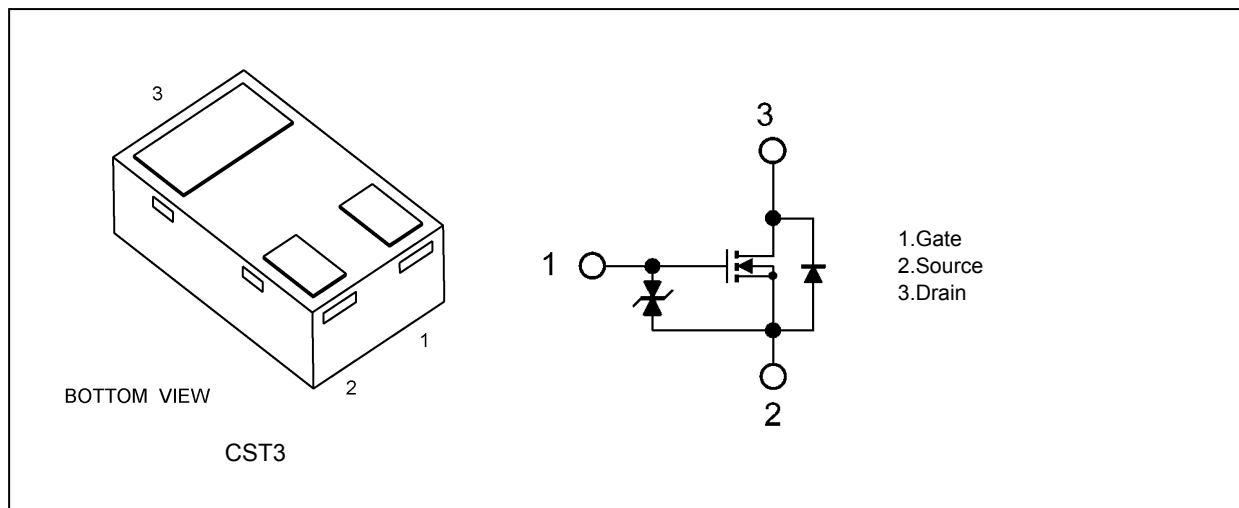
1. Applications

- High-Speed Switching

2. Features

- (1) 1.5-V gate drive voltage.
- (2) Low drain-source on-resistance
 - : $R_{DS(ON)} = 235 \text{ m}\Omega$ (max) (@ $V_{GS} = 4.5 \text{ V}$)
 - $R_{DS(ON)} = 300 \text{ m}\Omega$ (max) (@ $V_{GS} = 2.5 \text{ V}$)
 - $R_{DS(ON)} = 480 \text{ m}\Omega$ (max) (@ $V_{GS} = 1.8 \text{ V}$)
 - $R_{DS(ON)} = 840 \text{ m}\Omega$ (max) (@ $V_{GS} = 1.5 \text{ V}$)

3. Packaging and Pin Configuration



Start of commercial production
2015-11

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	20	V
Gate-source voltage	V_{GSS}	± 8	
Drain current (DC) (Note 1)	I_D	1400	mA
Drain current (pulsed) (Note 1),(Note 2)	I_{DP}	2800	
Power dissipation (Note 3)	P_D	500	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150°C .

Note 2: Pulse width (PW) ≤ 10 ms, duty $\leq 1\%$

Note 3: Mounted on an FR4 board.(25.4 mm $\times$ 25.4 mm $\times$ 1.6 mm, Cu Pad: 645 mm²)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the power dissipation, P_D , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 6\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	20	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = 1\text{ mA}, V_{GS} = -5\text{ V}$	15	—	—	
Gate threshold voltage (Note 2)	V_{th}	$V_{DS} = 3\text{ V}, I_D = 1\text{ mA}$	0.4	—	1.0	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = 800\text{ mA}, V_{GS} = 4.5\text{ V}$	—	186	235	$\text{m}\Omega$
		$I_D = 600\text{ mA}, V_{GS} = 2.5\text{ V}$	—	230	300	
		$I_D = 200\text{ mA}, V_{GS} = 1.8\text{ V}$	—	290	480	
		$I_D = 50\text{ mA}, V_{GS} = 1.5\text{ V}$	—	360	840	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 200\text{ mA}$	—	1.4	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th} , and $V_{GS(OFF)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.

Take this into consideration when using the device.

Note 3: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	55	—	pF
Reverse transfer capacitance	C_{rss}		—	6	—	
Output capacitance	C_{oss}		—	16	—	
Switching time (turn-on time)	t_{on}	$V_{DD} = 10\text{ V}, I_D = 200\text{ mA}$ $V_{GS} = 0\text{ to }2.5\text{ V}, R_G = 50\ \Omega,$ Duty $\leq 1\%$, Input: $t_r, t_f < 5\text{ ns}$ Common source, See Chapter 5.3	—	5.5	—	ns
Switching time (turn-off time)	t_{off}		—	8.5	—	

5.3. Switching Time Test Circuit

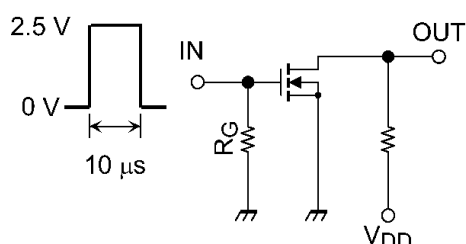


Fig. 5.3.1 Test Circuit of Switching Time

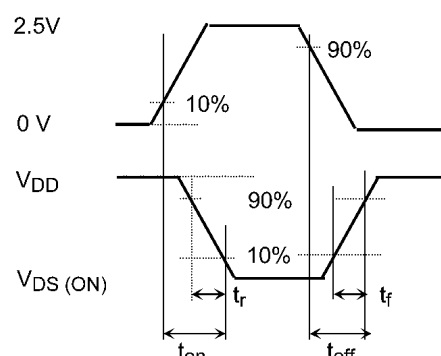


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} = 10\text{ V}, V_{GS} = 4.5\text{ V},$ $I_D = 800\text{ mA}$	—	1.0	—	nC
Gate-source charge 1	Q_{gs1}		—	0.12	—	
Gate-drain charge	Q_{gd}		—	0.4	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	V _{DSF}	I _D = -1.4 A, V _{GS} = 0 V	—	-0.82	-1.2	V

Note 1: Pulse measurement.

6. Marking

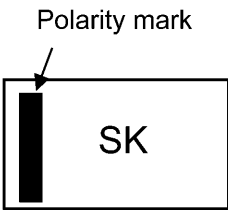


Fig. 6.1 Marking

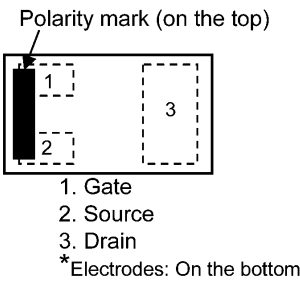
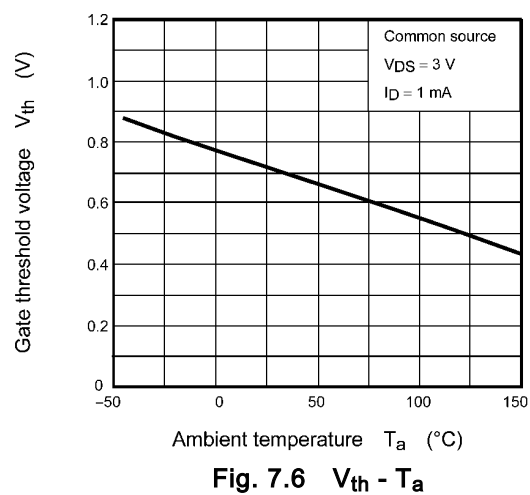
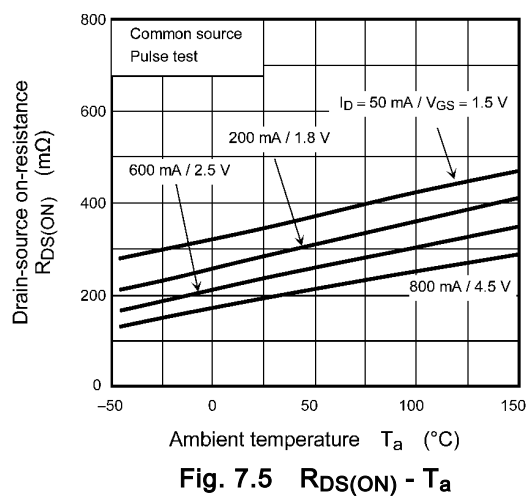
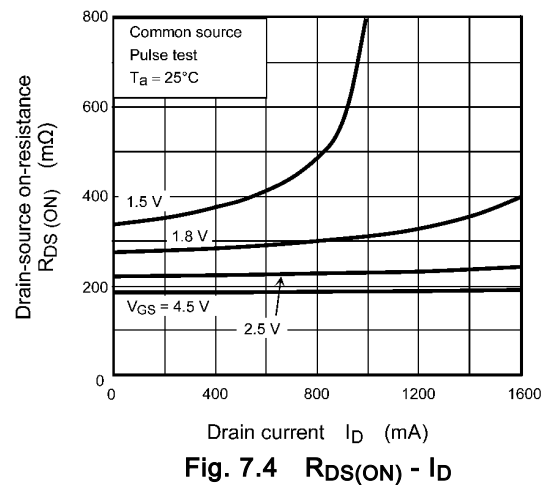
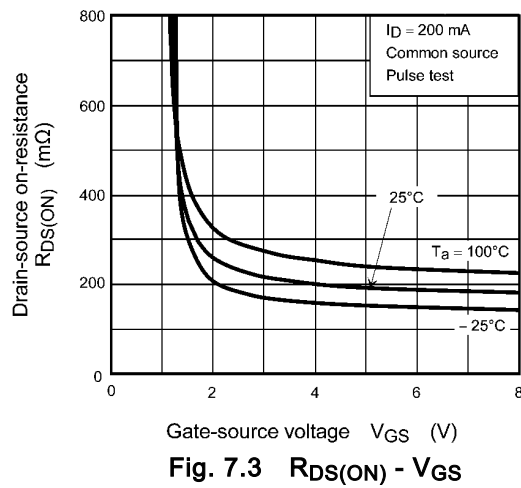
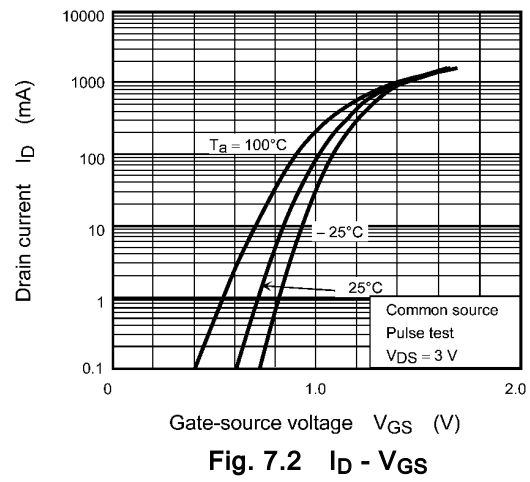
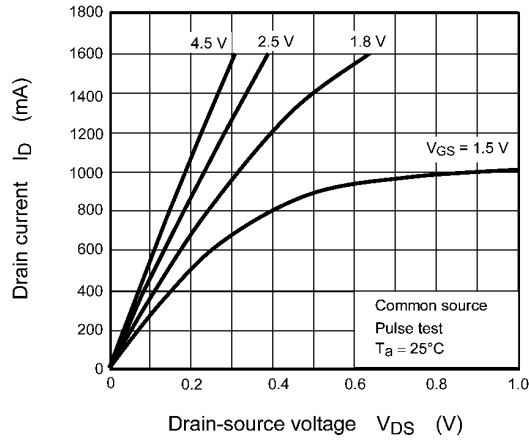


Fig. 6.2 Pin Condition(top view)

7. Characteristics Curves (Note)



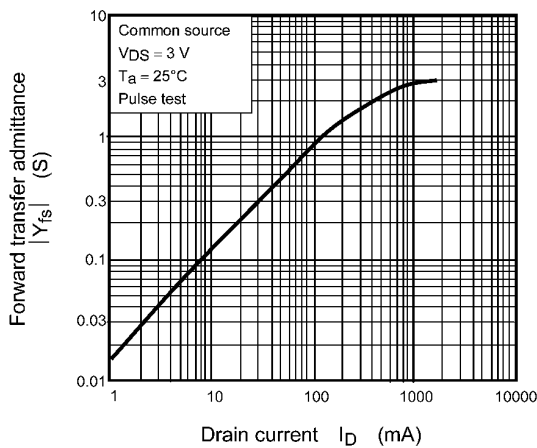


Fig. 7.7 $|Y_{fs}| - I_D$

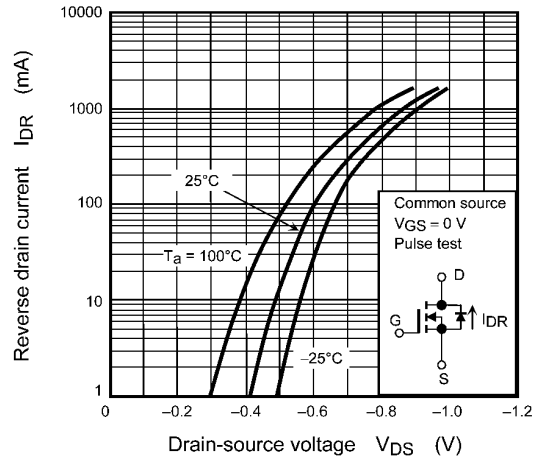


Fig. 7.8 $I_{DR} - V_{DS}$

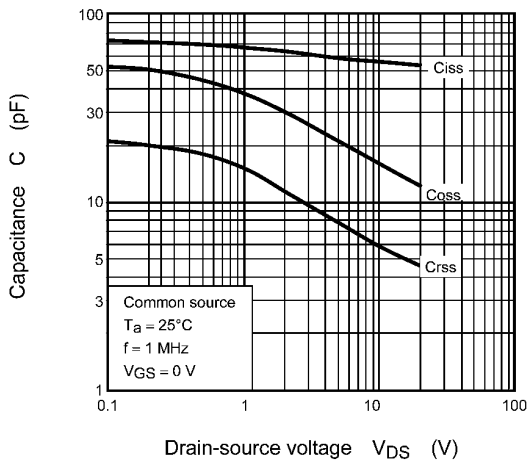


Fig. 7.9 $C - V_{DS}$

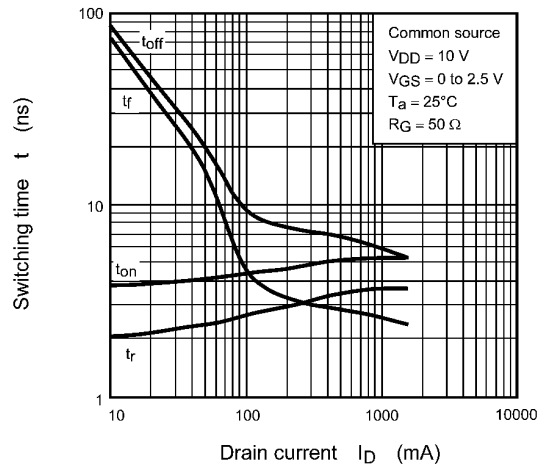


Fig. 7.10 $t - I_D$

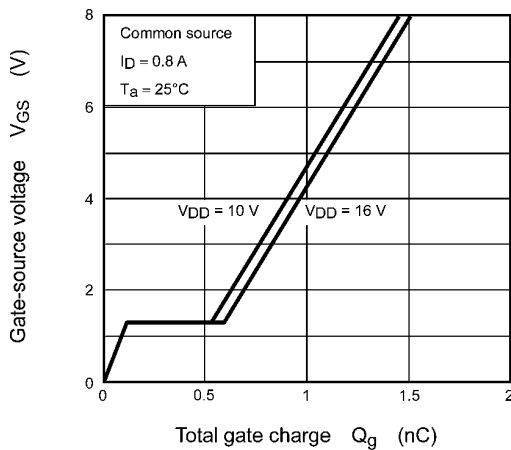


Fig. 7.11 Dynamic Input Characteristics

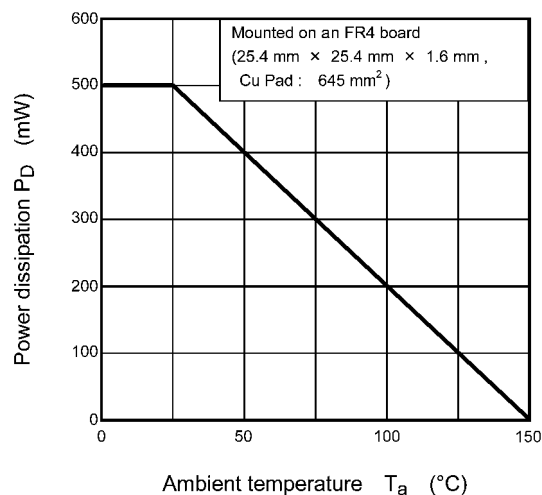


Fig. 7.12 $P_D - T_a$

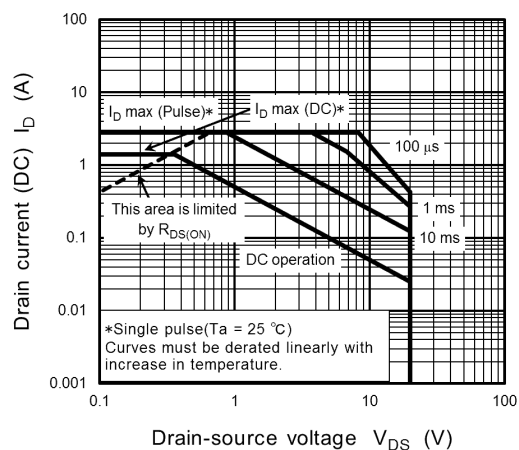
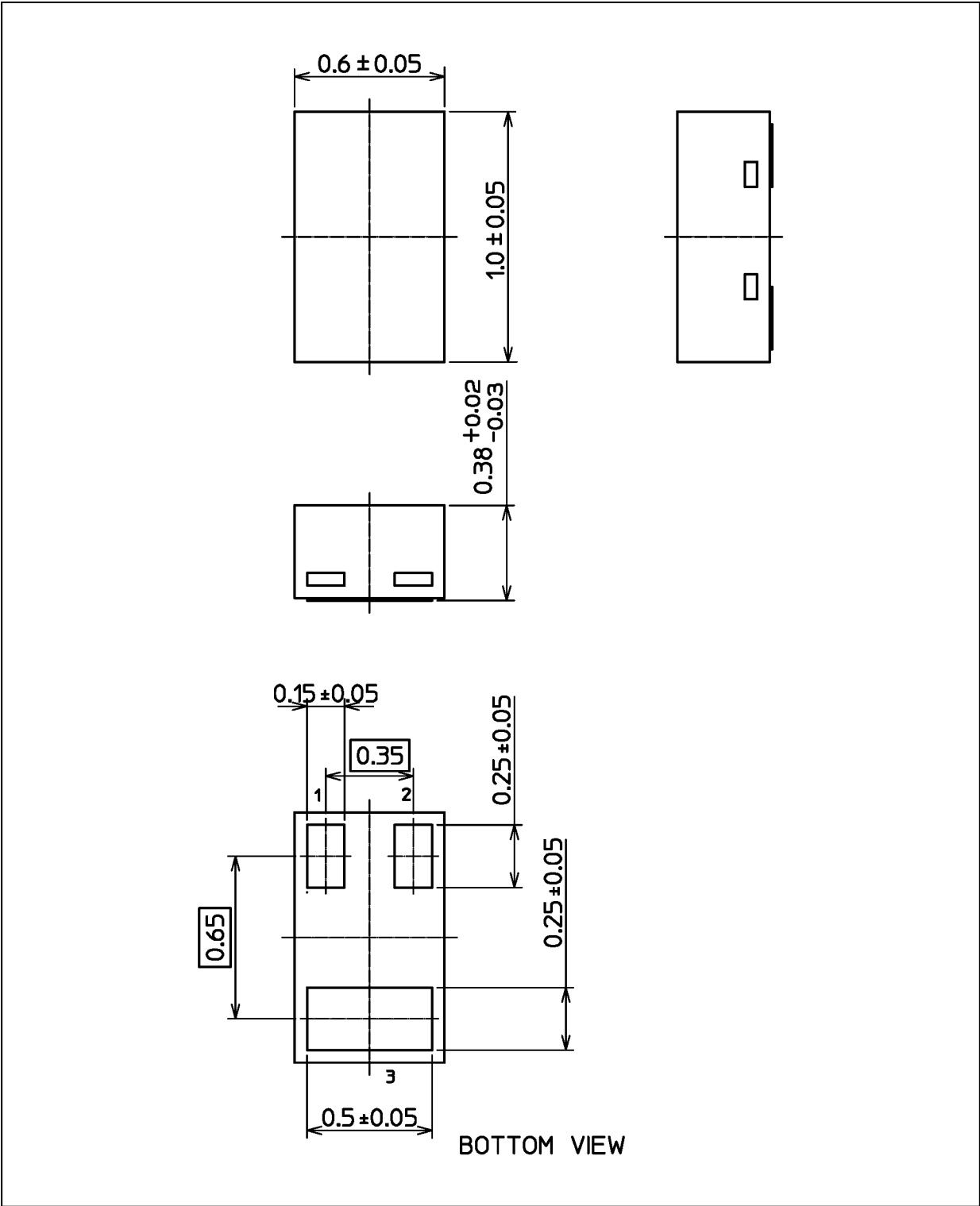


Fig. 7.13 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.75 mg (typ.)

Package Name(s)
Nickname: CST3

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