



PSMN2R6-80YSF

NextPower 80 V, 2.4 mOhm, 231 A, N-channel MOSFET in LFAK56E package

29 April 2024

Product data sheet

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 231 A $I_{D(max)}$ – demonstrated continuous current rating
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFAK56E package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- USB-PD adapters
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

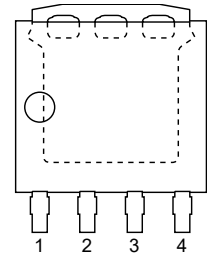
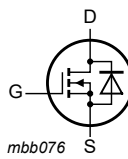
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	231	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	294	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	1.9	2.4	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 105\text{ °C}$; Fig. 13	-	3.1	4.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 14 ; Fig. 15	5.8	16.5	38	nC
$Q_{G(tot)}$	total gate charge		42.5	85	127	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 58\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 127\text{ μs}$; Fig. 4	[1]	-	383	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; Fig. 18	-	33	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R6-80YSF	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R6-80YSF	2F6S80Y

8. Limiting values

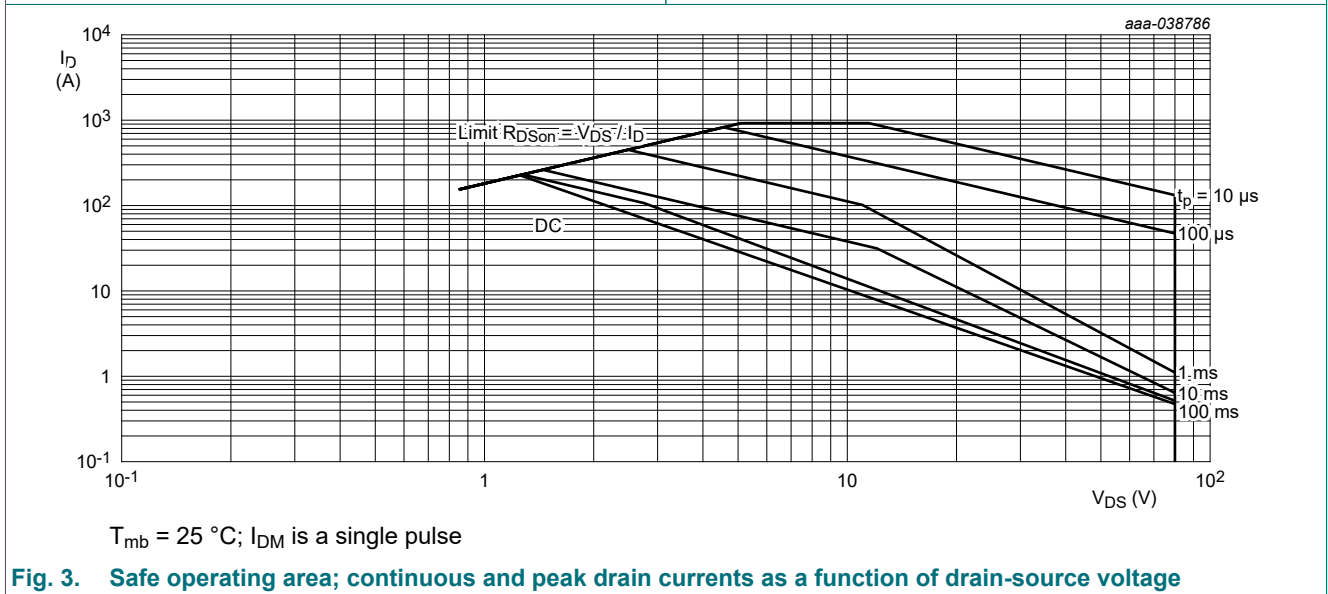
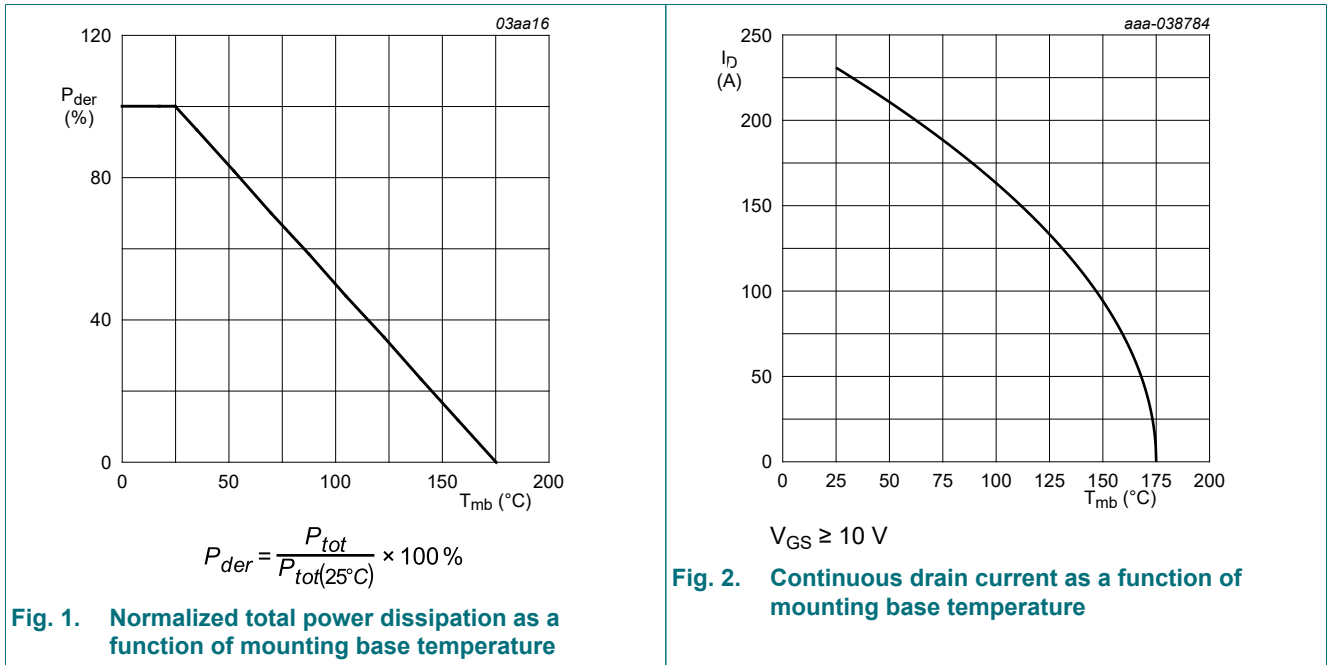
Table 5. Limiting values

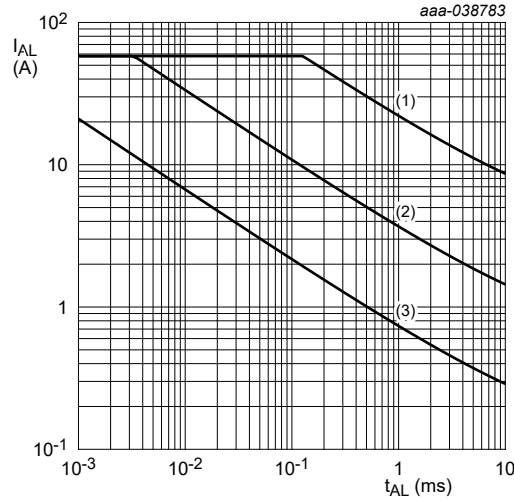
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	294	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	231	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	163	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	923	A
T_{stg}	storage temperature		-55	175	°C

Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature		-55	175	°C
$T_{slid(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	231	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	923	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 58\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 127\text{ }\mu\text{s}$; Fig. 4	[1]	-	383 mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[1]	-	58 A

[1] Protected by 100% test





(1) $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; (2) $T_{j(\text{init})} = 150\text{ }^{\circ}\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6 Fig. 7	-	42 85	-	K/W K/W

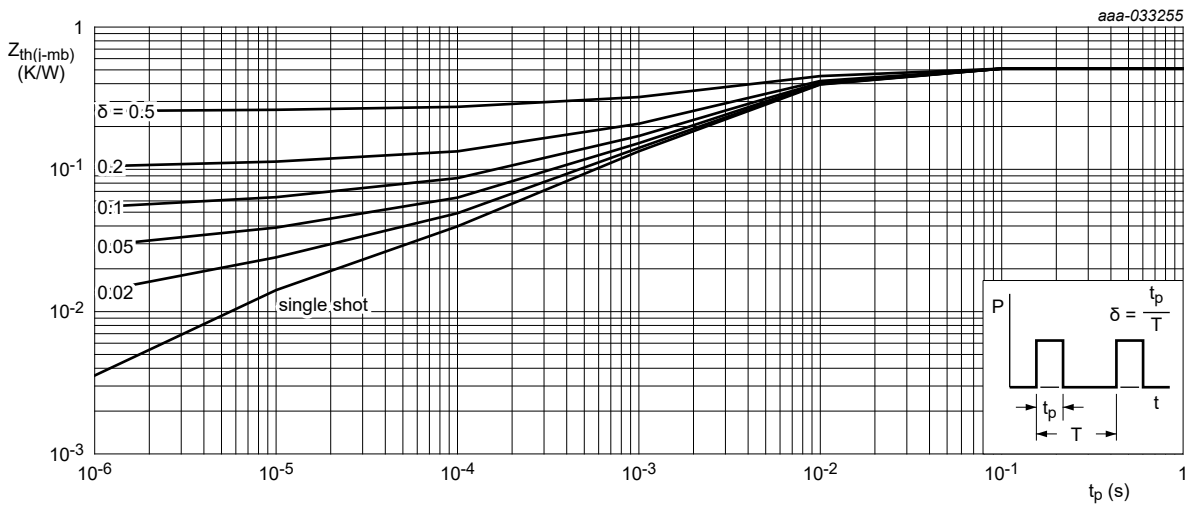
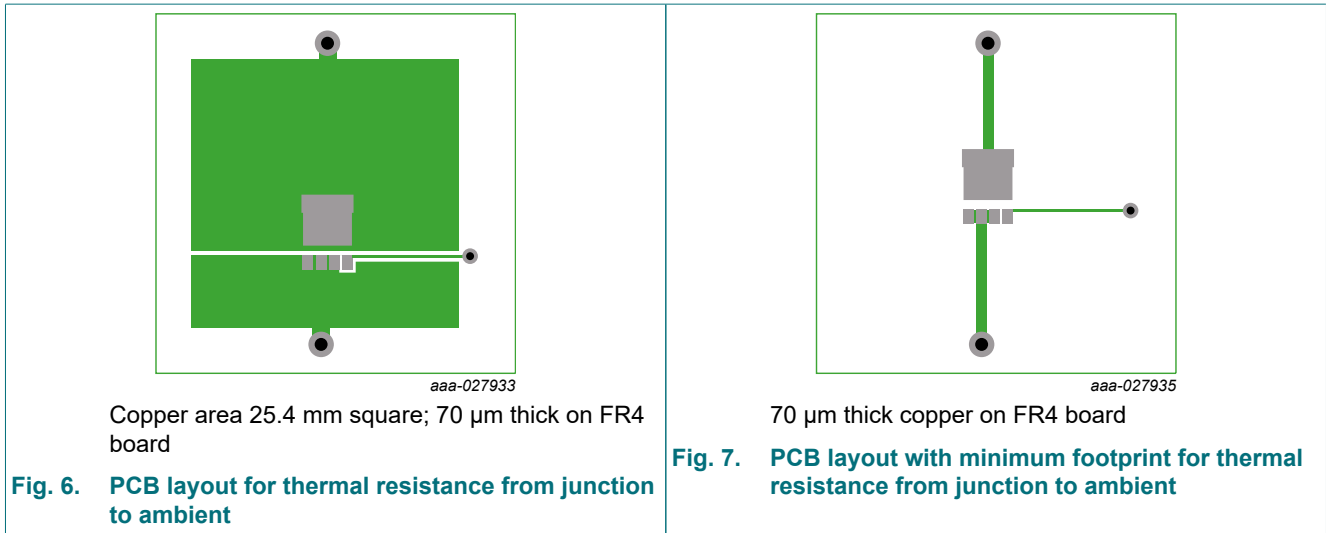


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



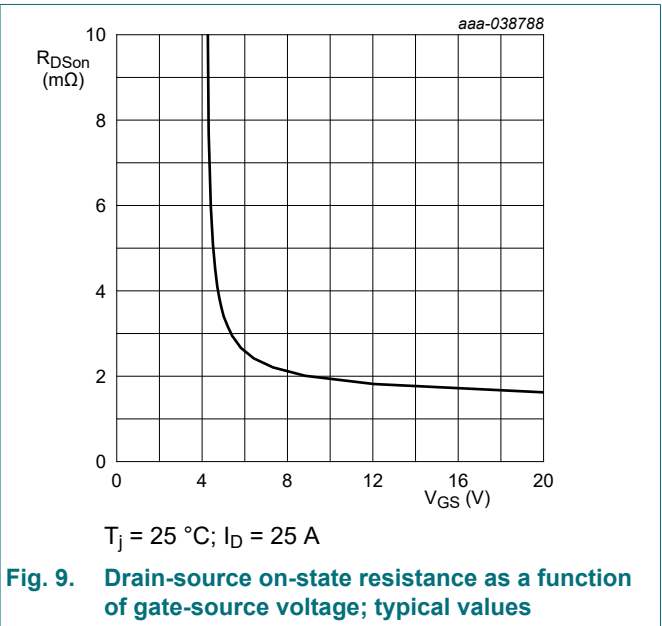
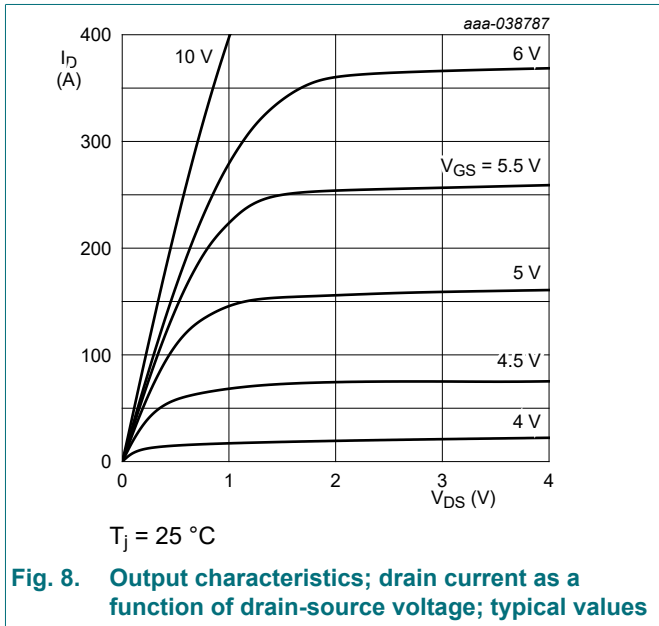
10. Characteristics

Table 7. Characteristics

T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	80	87	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	72	84	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 11	2	3	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C	-	1.9	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C	-	3.3	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C	-	-7	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C	-	0.003	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 125 °C	-	3	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	1.9	2.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 13	-	3.1	4.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 13	-	4.4	5.5	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	0.4	0.8	1.6	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	42.5	85	127	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	74	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V};$ Fig. 14 ; Fig. 15	8.8	22	35	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	16	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6	-	nC
Q_{GD}	gate-drain charge		5.8	16.5	38	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 40\text{ V};$ Fig. 14 ; Fig. 15	-	4	-	V
C_{iss}	input capacitance	$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ Fig. 16	3510	5850	8191	pF
C_{oss}	output capacitance		554	1385	2493	pF
C_{rss}	reverse transfer capacitance		4	44	102	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40\text{ V}; R_L = 1.6\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\ \Omega$	-	19	-	ns
t_r	rise time		-	18	-	ns
$t_{d(off)}$	turn-off delay time		-	53	-	ns
t_f	fall time		-	29	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.79	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 40\text{ V};$ Fig. 18	-	38	-	ns
Q_r	recovered charge		-	33	-	nC



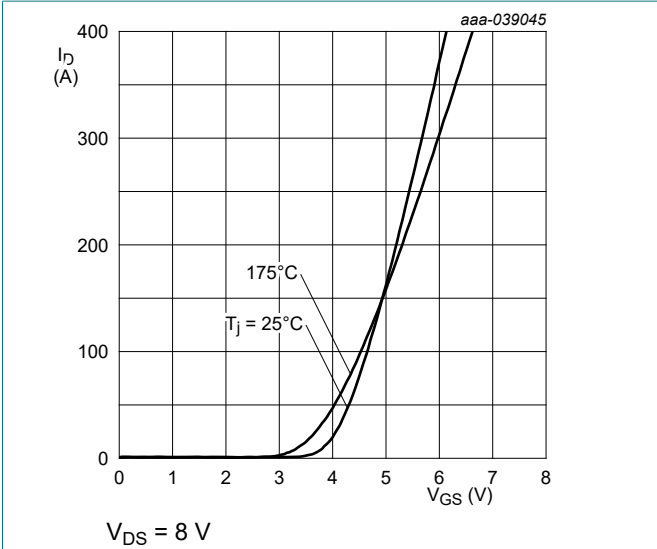


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

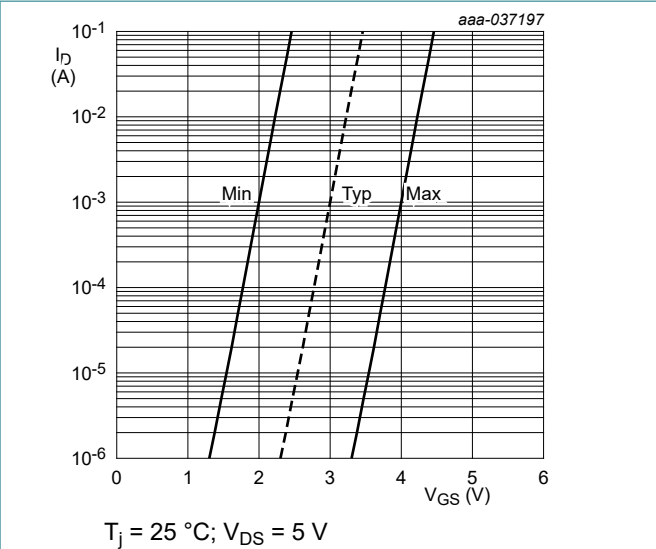


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

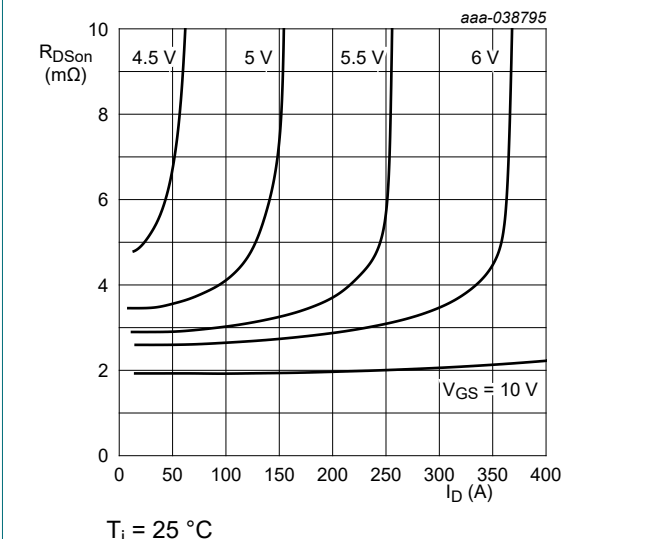


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

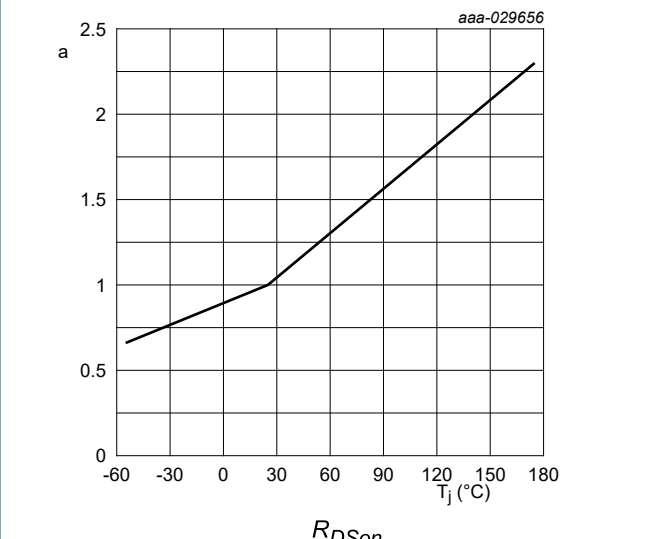


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

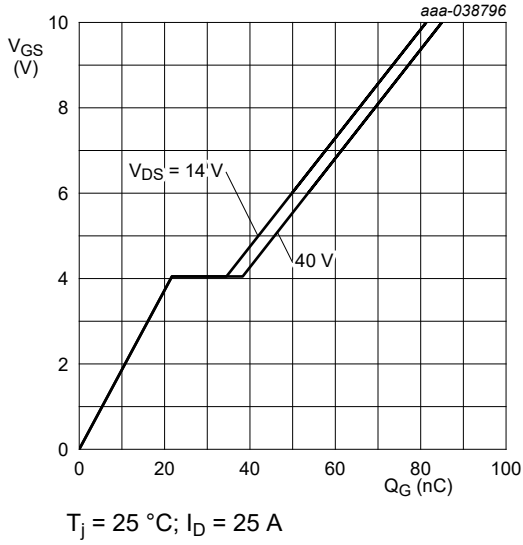


Fig. 14. Gate-source voltage as a function of gate charge; typical values

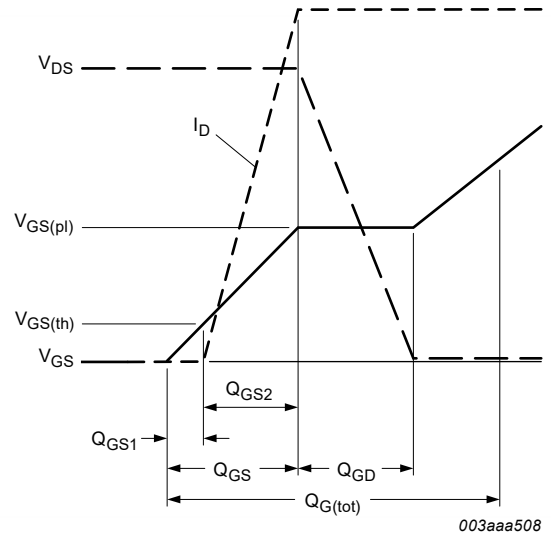


Fig. 15. Gate charge waveform definitions

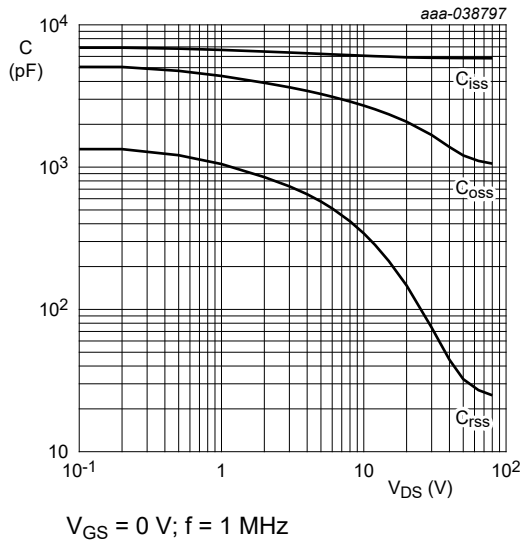


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

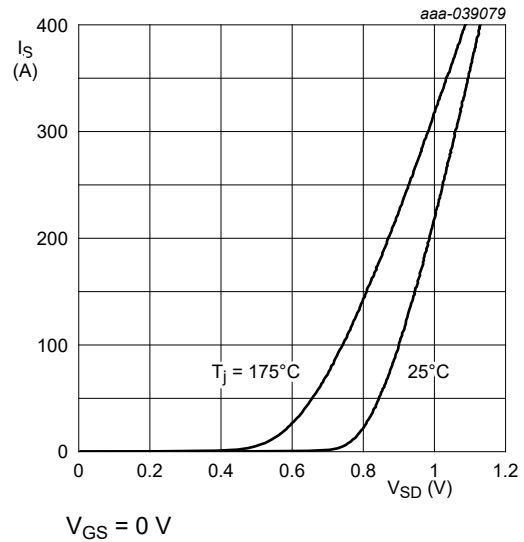


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

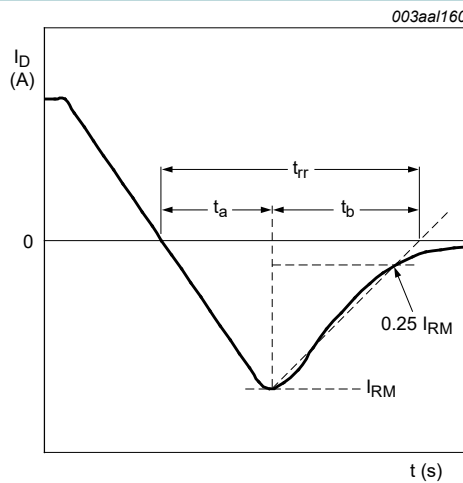


Fig. 18. Reverse recovery timing definition

11. Package outline

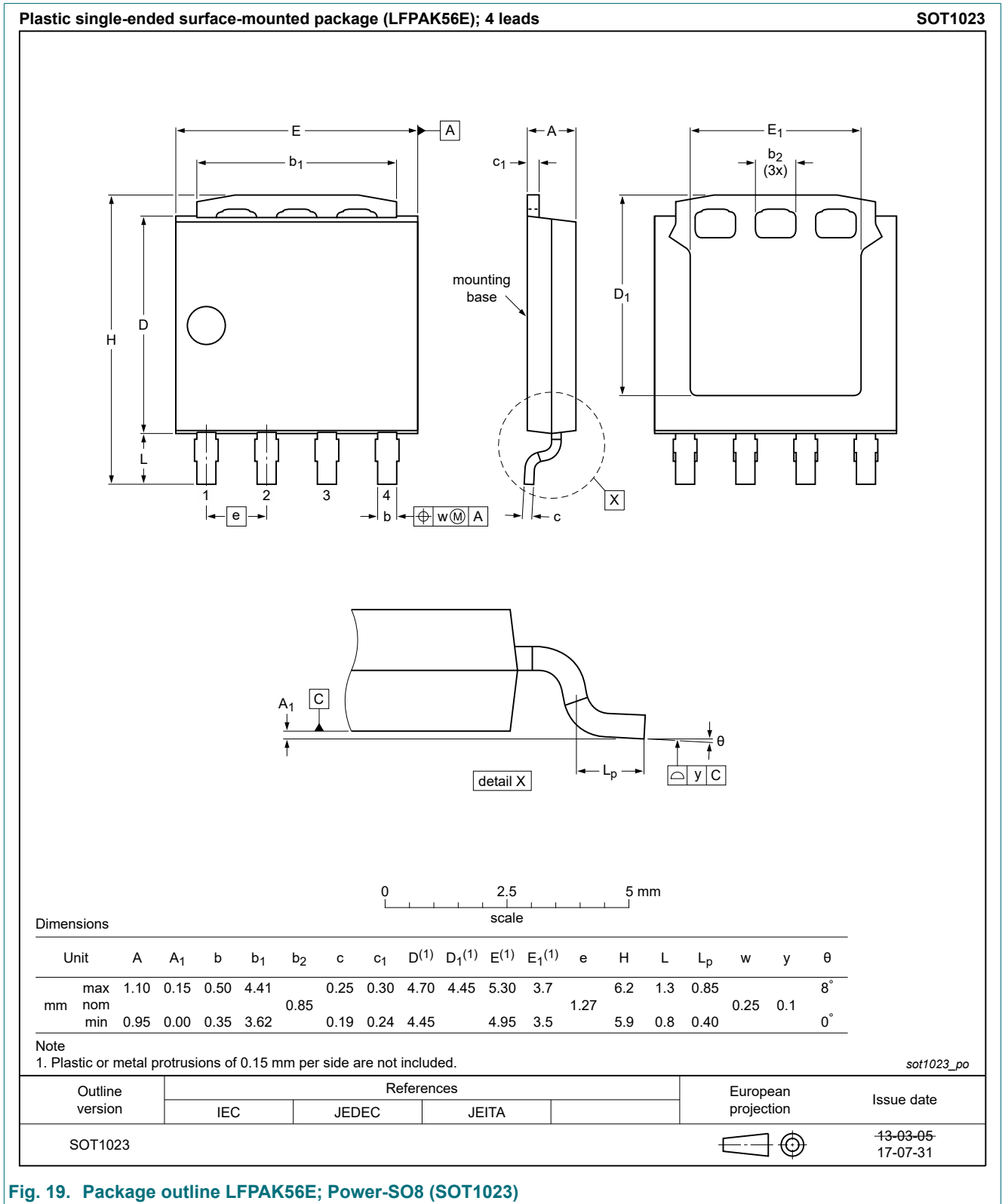


Fig. 19. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

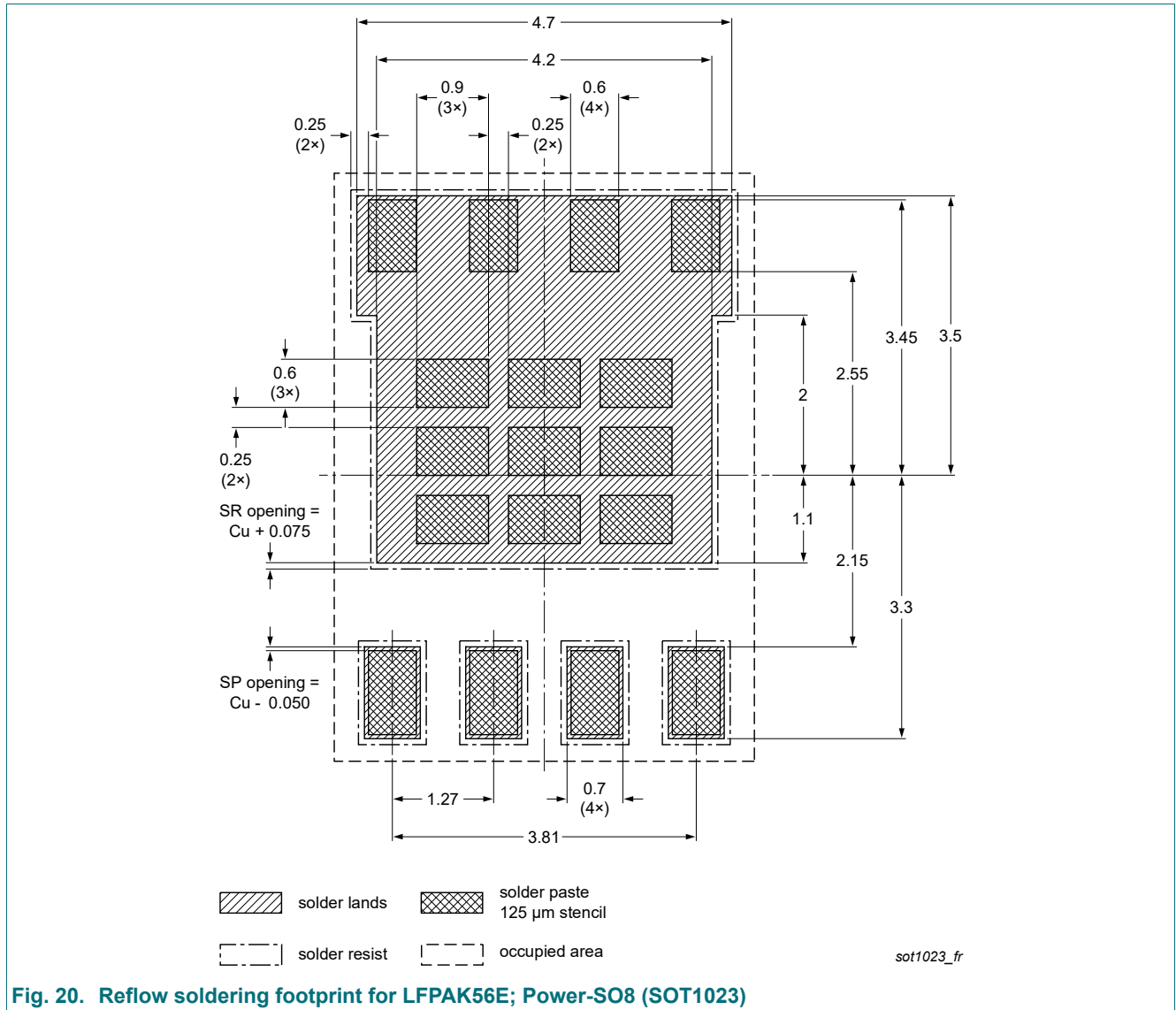


Fig. 20. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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