



BUK7Y1R0-40N

N-channel 40 V, 0.97 mOhm, Standard level MOSFET in LFPAK56

4 January 2024

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 15 low ohmic enhanced-Trench Bottom Oxide (e-TBO) technology, providing high ruggedness at low $R_{DS(on)}$, housed in an LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 15 e-TBO technology:
 - Merging benefits of Superjunction technology (high ruggedness) and Split-Gate technology (low $R_{DS(on)}$)
- Fast and efficient switching with high damping and low spiking
- Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joints
- LFPAK copper clip technology:
 - Improved reliability, with reduced R_{th} , $R_{DS(on)}$ and package inductance
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motor, lighting and solenoid control
- Reverse battery protection
- Ultra high-performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	320	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 25\text{ °C}$; Fig. 12		0.57	0.81	0.97	mΩ

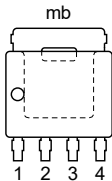
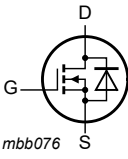
N-channel 40 V, 0.97 mOhm, Standard level MOSFET in LFPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14 ; Fig. 15	81	135	189	nC

[1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	 <i>mbb076</i>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y1R0-40N	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

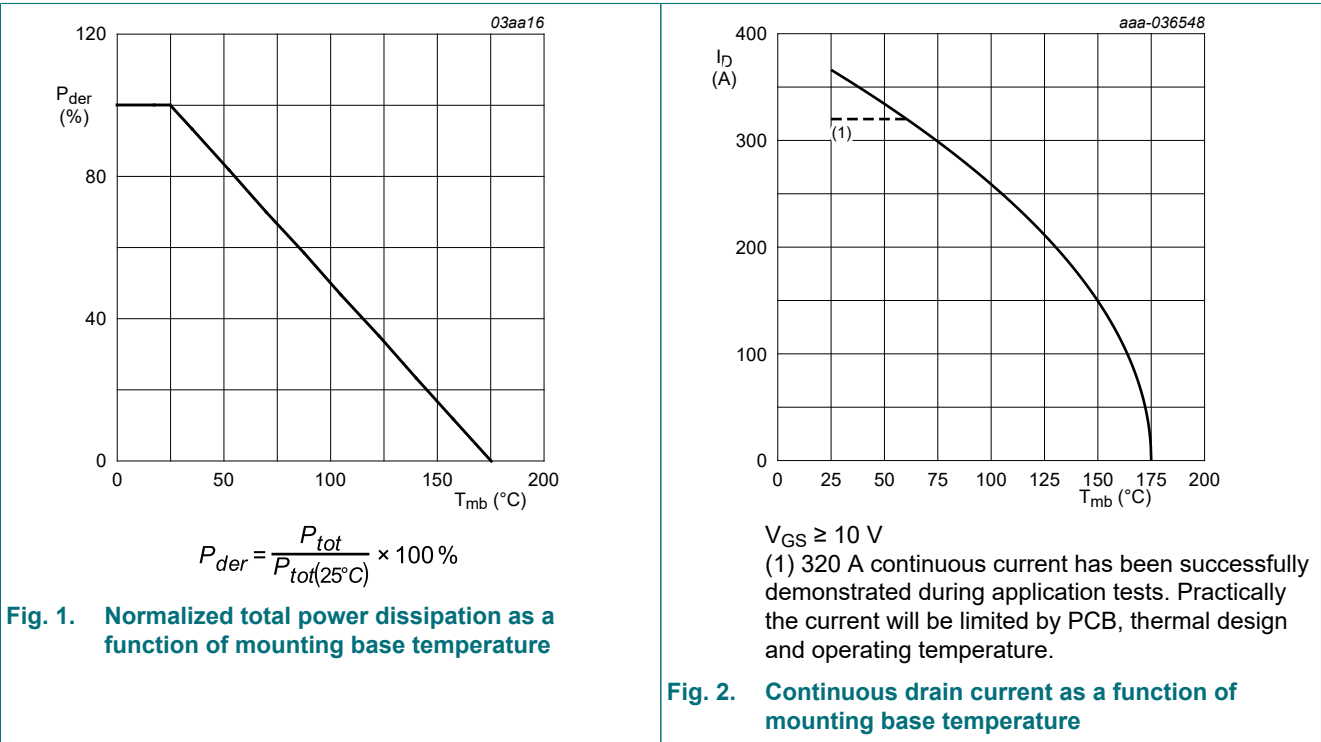
Type number	Marking code
BUK7Y1R0-40N	71N040Y

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	268	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	320	A
				-	262	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3 ; Fig. 4	[1]	-	1465	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	268	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1465	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 190 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 5	[2] [3]	-	145	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[4]	-	190	A

- [1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test.



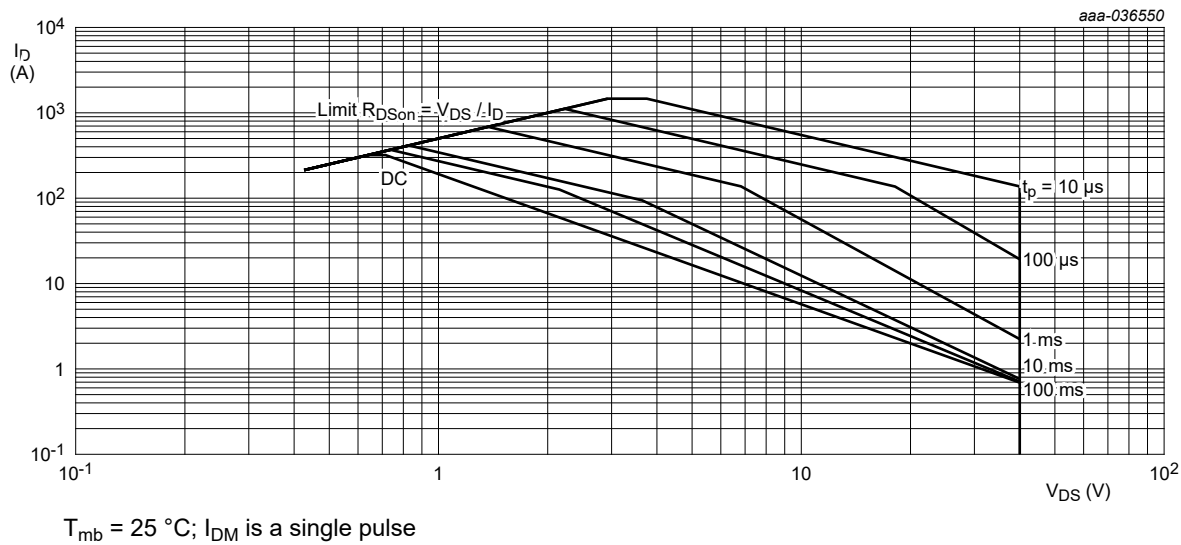


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

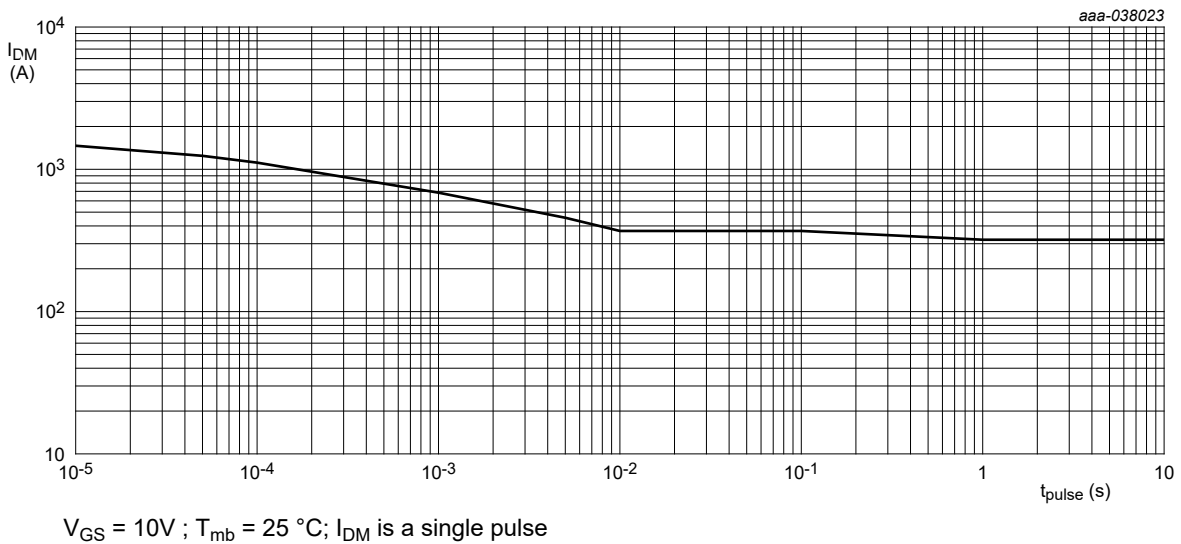
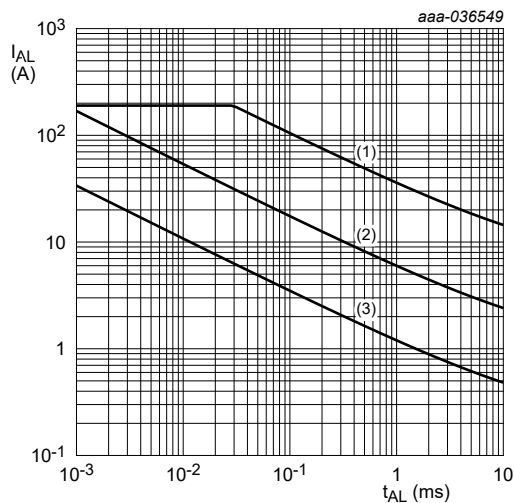


Fig. 4. Peak Current Capability



(1) $T_{j(init)} = 25\ ^\circ\text{C}$; (2) $T_{j(init)} = 150\ ^\circ\text{C}$; (3) Repetitive Avalanche

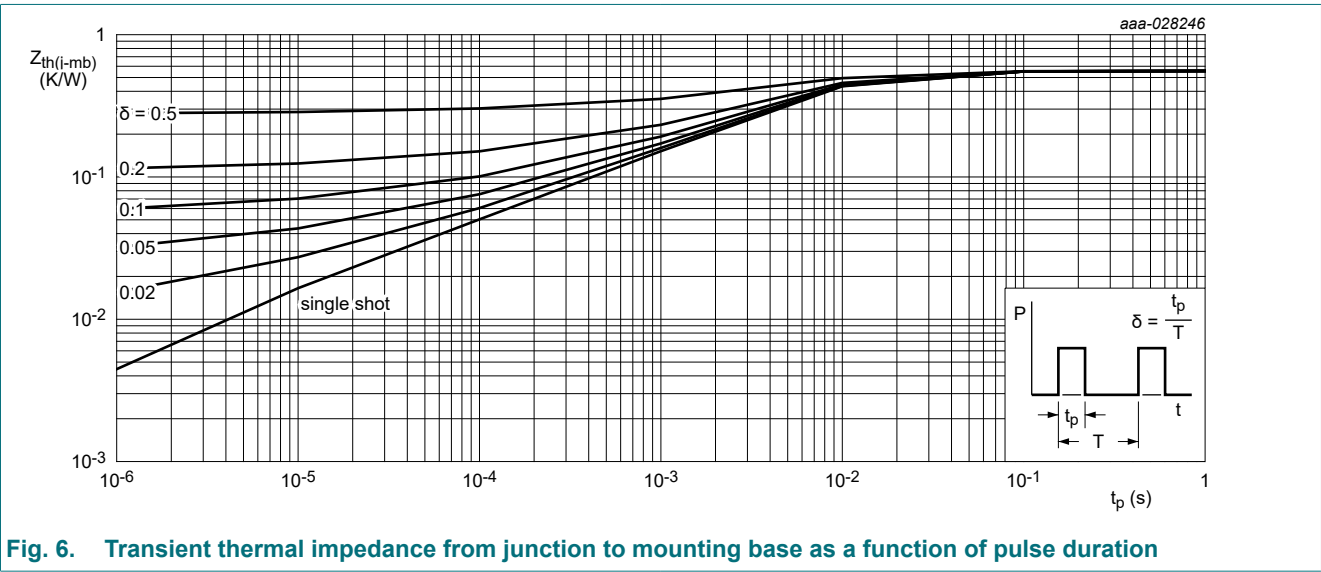
Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	0.48	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	24	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		40	43	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -40 °C		-	40.5	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		36	40	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 10		2.4	3	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C; Fig. 11		-	-	4.3	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C; Fig. 11		1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C		-	0.1	1	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _J = 125 °C		-	1.1	10	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _J = 175 °C		-	80	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12		0.57	0.81	0.97	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 105 °C; Fig. 13		0.77	1.15	1.46	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 125 °C; Fig. 13		0.84	1.25	1.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 13		1	1.52	2	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.2	0.63	1.6	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		81	135	189	nC
Q _{GS}	gate-source charge			14	26	38	nC
Q _{GD}	gate-drain charge			12	42	72	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 16		4552	7587	10622	pF
C _{oss}	output capacitance			1166	1666	2166	pF
C _{rss}	reverse transfer capacitance			252	631	1010	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	25	-	ns
t _r	rise time			-	49	-	ns
t _{d(off)}	turn-off delay time			-	79	-	ns
t _f	fall time			-	58	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17		-	0.79	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C; Fig. 18		-	34	-	ns
Q _r	recovered charge		[1]	-	24	-	nC

[1] includes capacitive recovery

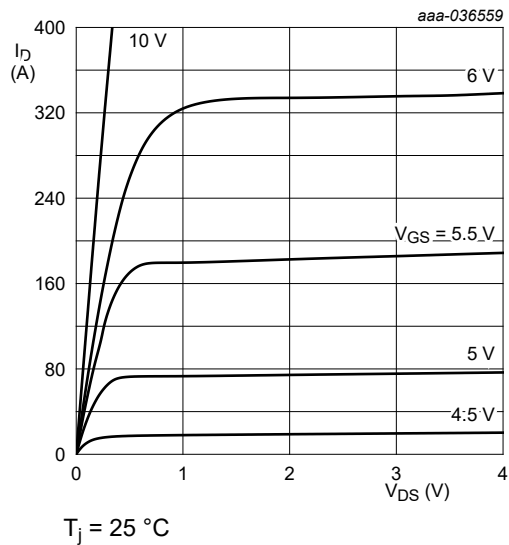


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

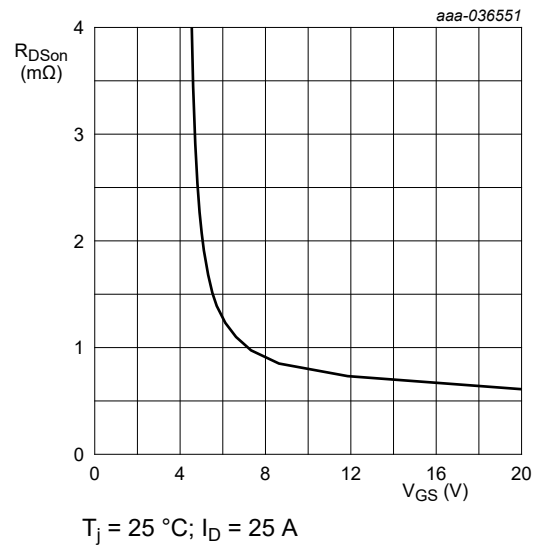


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

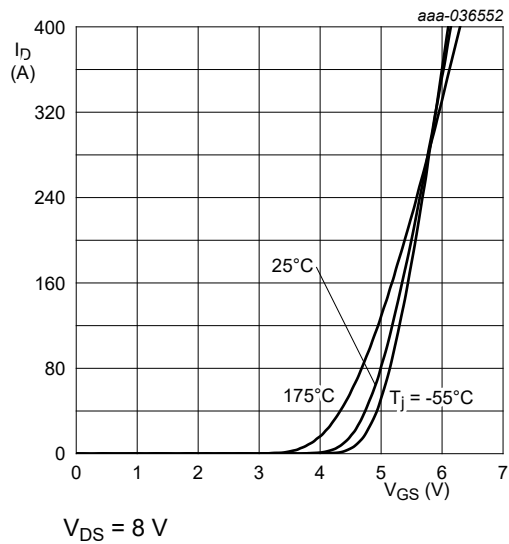


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

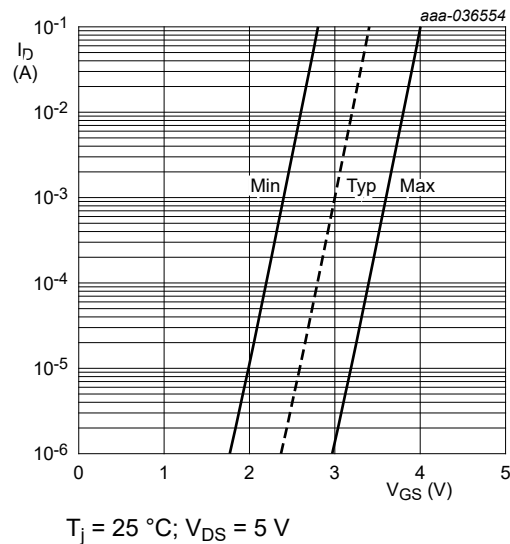


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

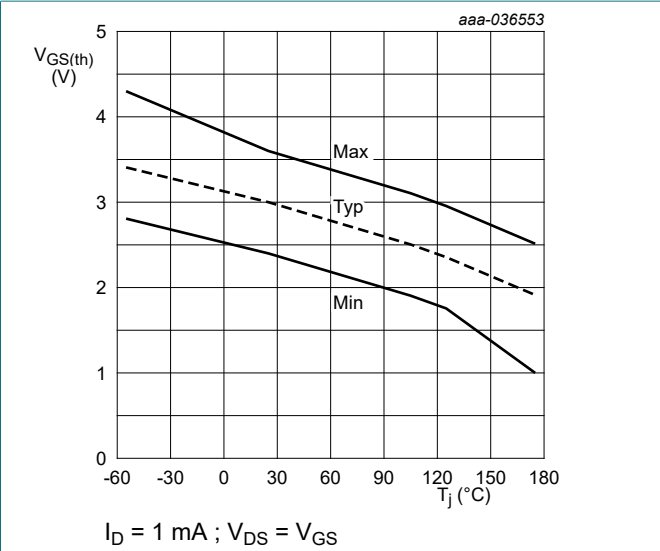


Fig. 11. Gate-source threshold voltage as a function of junction temperature

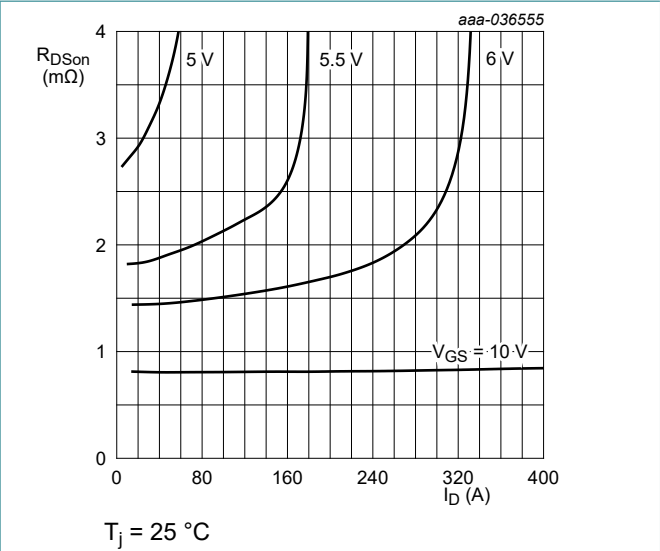


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

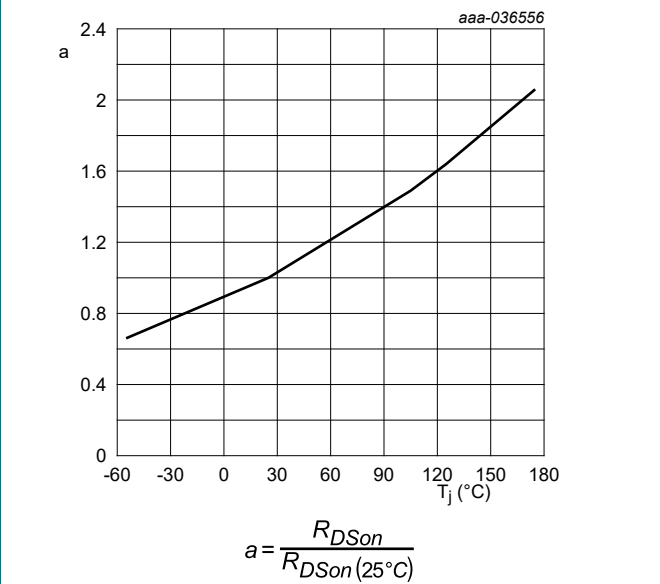


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

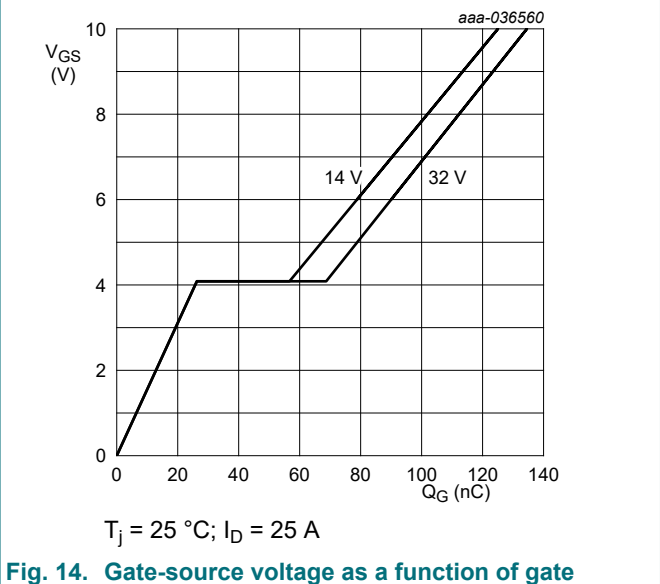


Fig. 14. Gate-source voltage as a function of gate charge; typical values

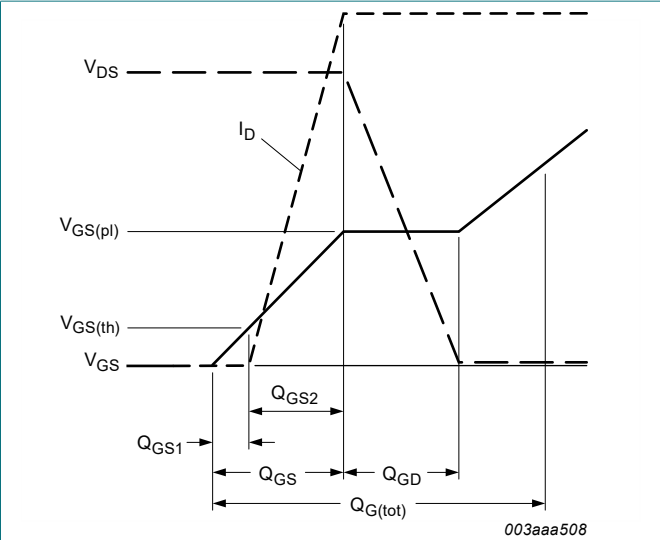


Fig. 15. Gate charge waveform definitions

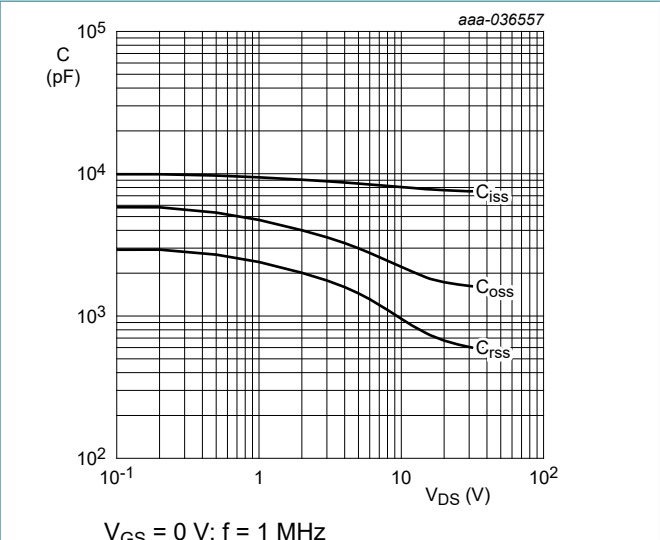


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

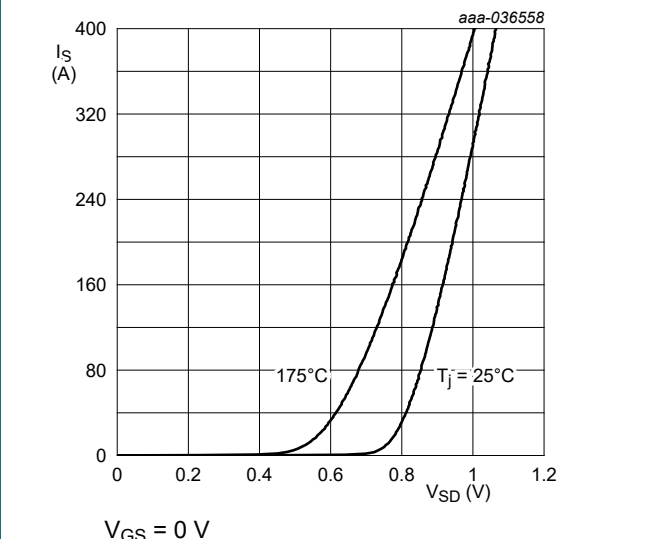


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

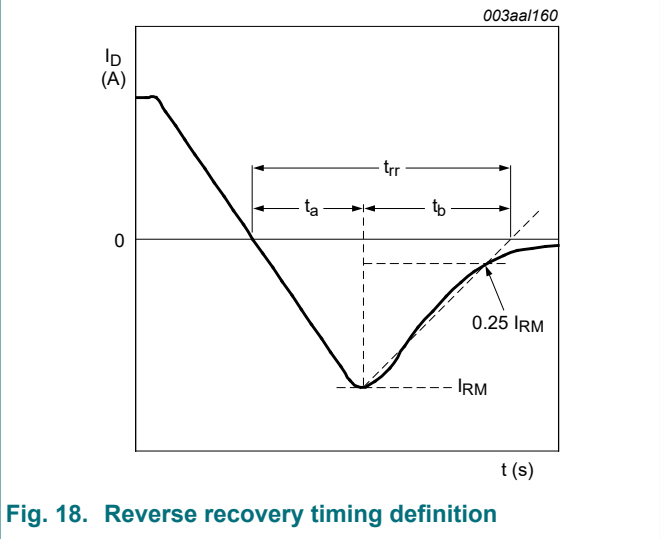


Fig. 18. Reverse recovery timing definition

11. Package outline

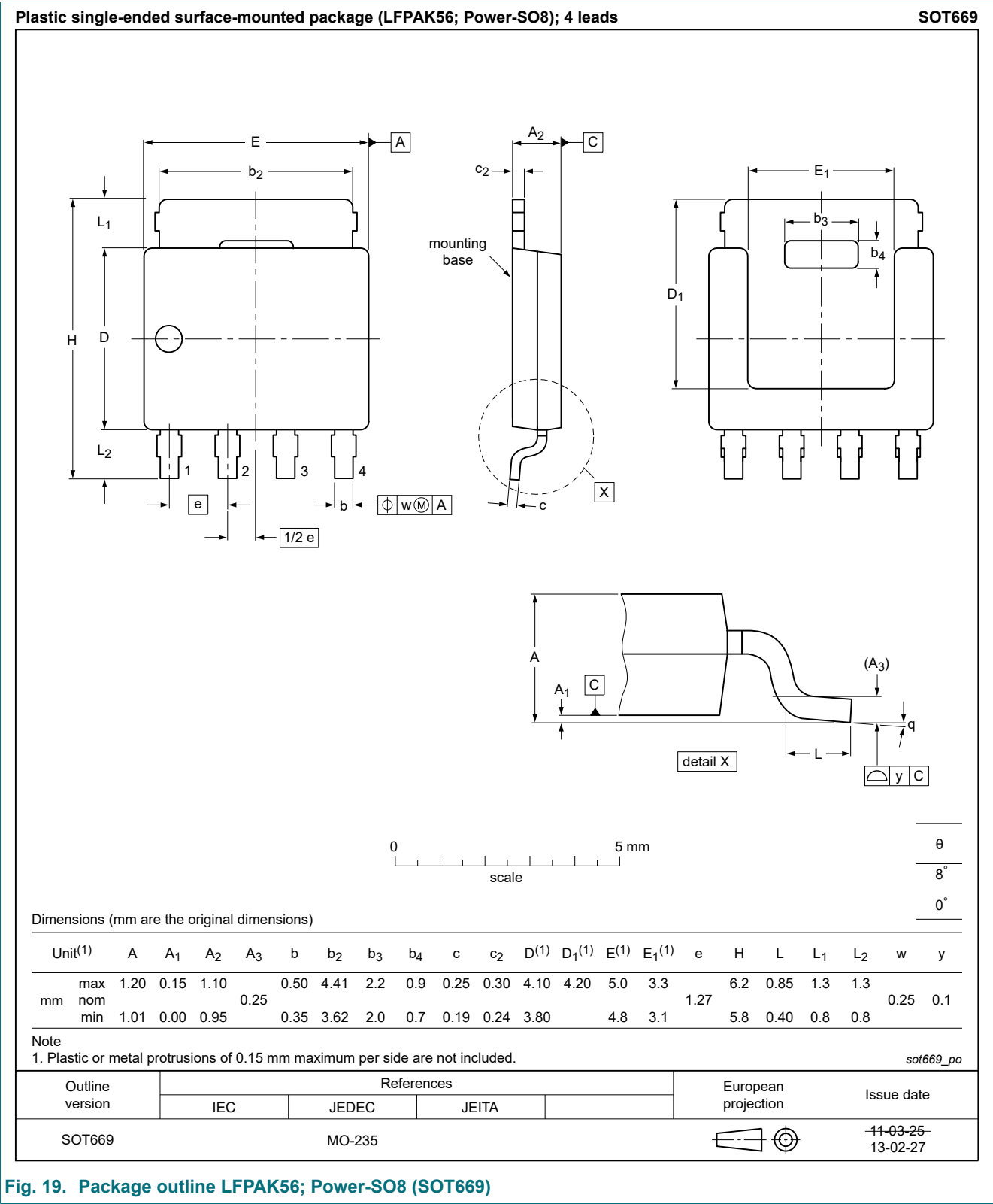


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

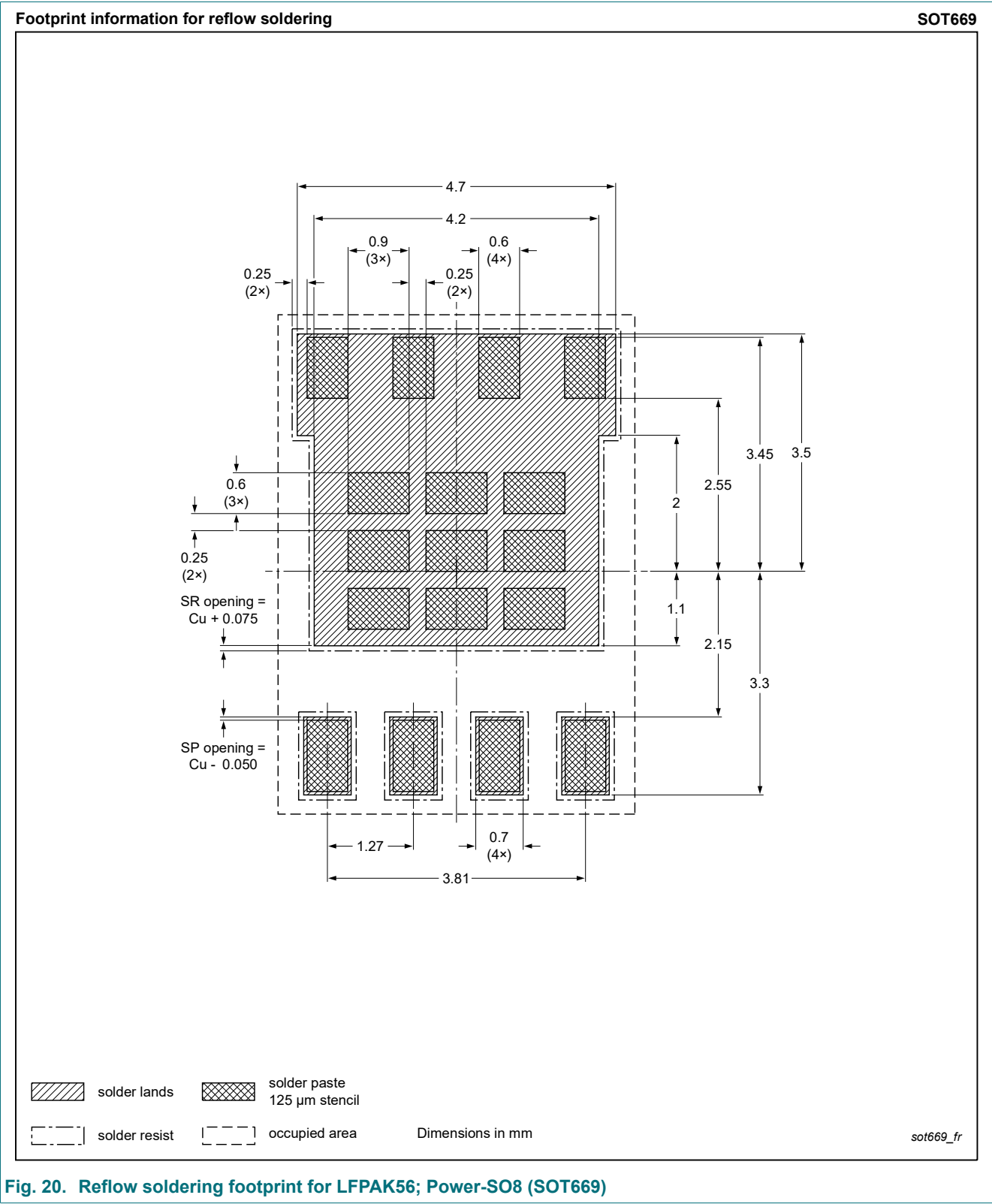


Fig. 20. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

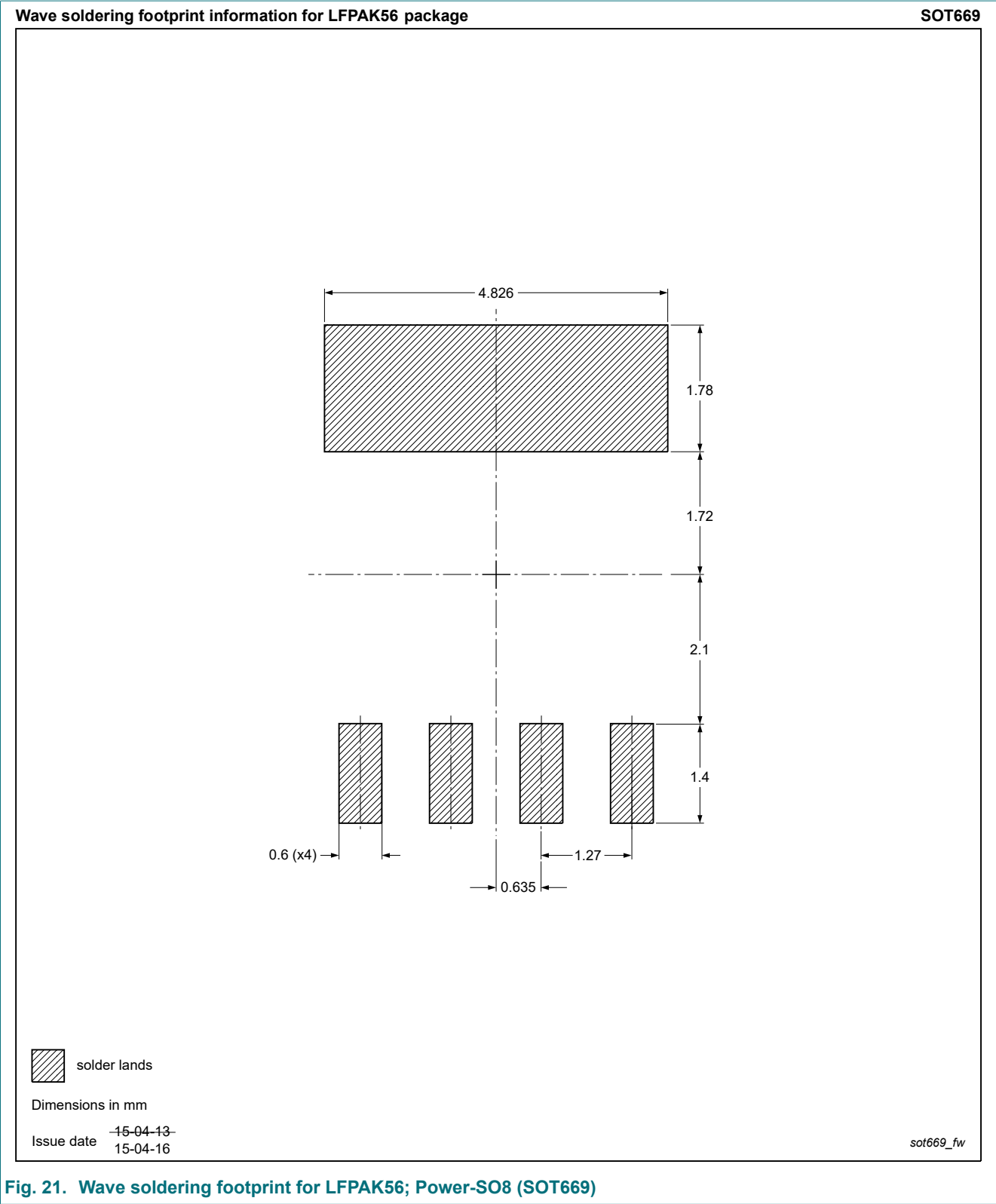


Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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