



PSMN3R2-40YLB

N-channel 40 V, 3.3 mOhm, 120 A logic level MOSFET in LPAK56 using optimized NextPowerS3 Schottky-Plus technology

13 February 2024

Product data sheet

1. General description

120 A, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56 package, using advanced TrenchMOS Superjunction technology with optimization to provide improved EMC performance (up to 6 dB). This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- Optimized for improved EMC Performance
- 120 A continuous $I_{D(max)}$ rating
- Avalanche rated, 100% tested at $I_{AS} = 120$ A
- Strong SOA (linear-mode) rating
- NextPowerS3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{rr} , Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low V_{SD} , low Q_{rr} , soft recovery and low I_{DSS} leakage
- Optimized for 4.5 V gate drive utilizing NextPowerS3 Superjunction technology
- High reliability LPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints providing excellent board level reliability
- Low parasitic inductance and resistance

3. Applications

- Automation, control and instrumentation
- Autonomous systems, Robotics and Cobots
- DC-to-DC converters
- Brushless DC motor control
- Brushed motors
- Battery isolation
- Industrial load-switch and eFuse
- Inrush management, hotswap

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	115	W
T_j	junction temperature			-55	-	175	°C

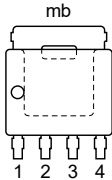
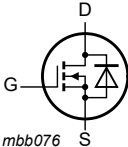
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	2.9	3.3	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	3.6	4.2	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; T _j = 25 °C; Fig. 12 ; Fig. 13		1.3	4.2	8.4	nC
Q _{G(tot)}	total gate charge			12	19	27	nC

[1] 120 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R2-40YLB	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R2-40YLB	3B2L40Y

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V
V _{DSM}	peak drain-source voltage	t _p ≤ 20 ns; f = 500 kHz; E _{DS(AL)} ≤ 200 nJ; pulsed	-	45	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	40	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	115	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	120	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	95	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	537	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C

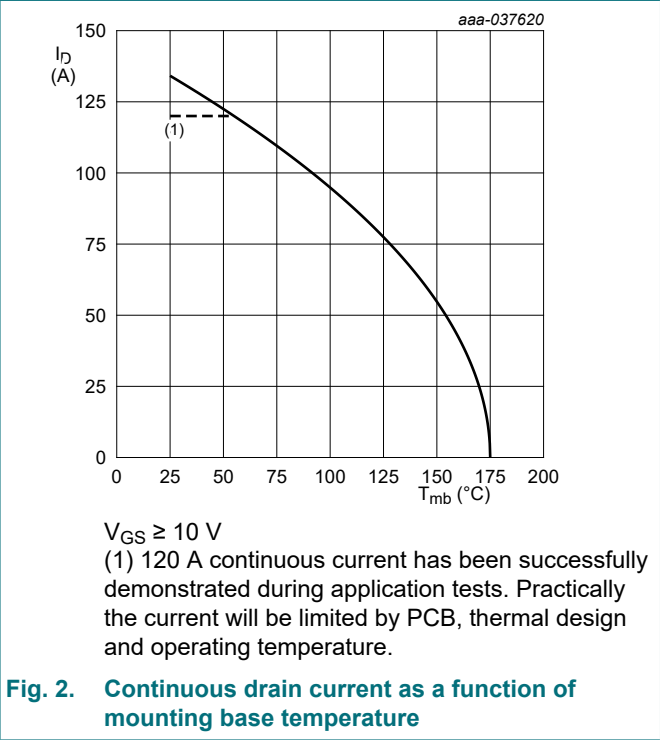
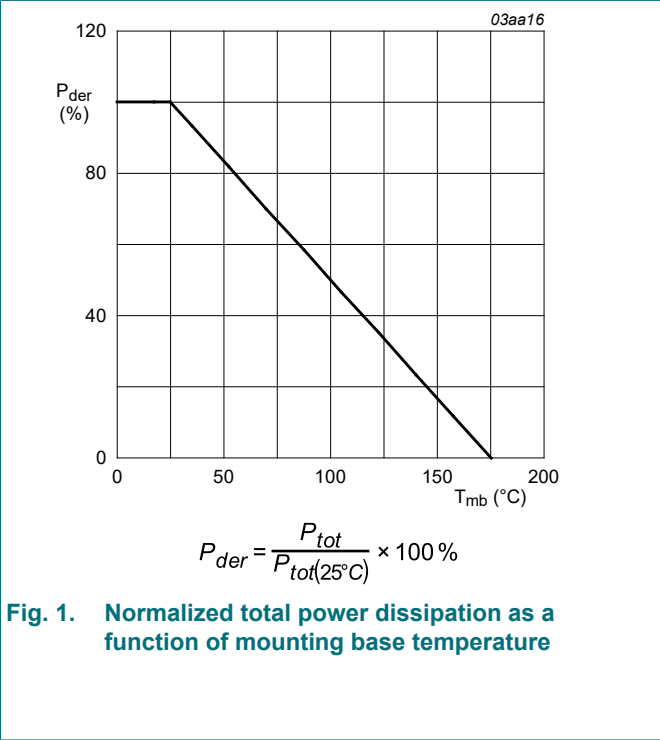
Source-drain diode

I _S	source current	T _{mb} = 25 °C		-	115	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	537	A

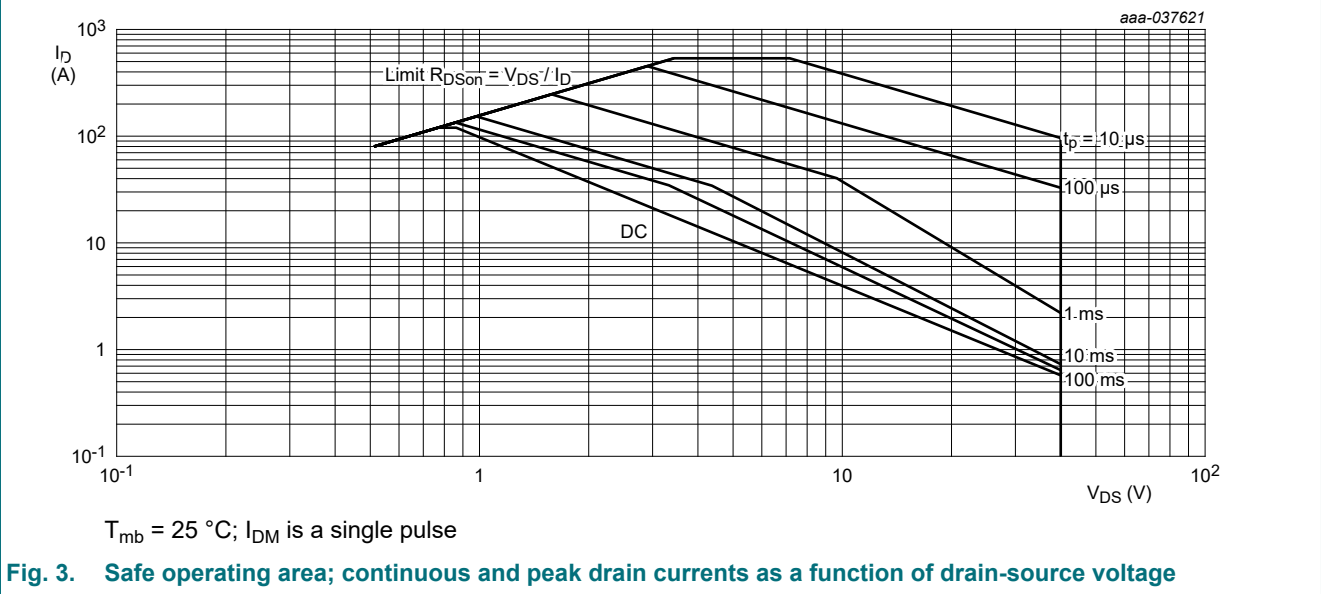
Avalanche ruggedness

E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 39 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 146 μs	[2]	-	148	mJ
		I _D = 25 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 374 μs	[2]	-	243	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	120	A

- [1] 120 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



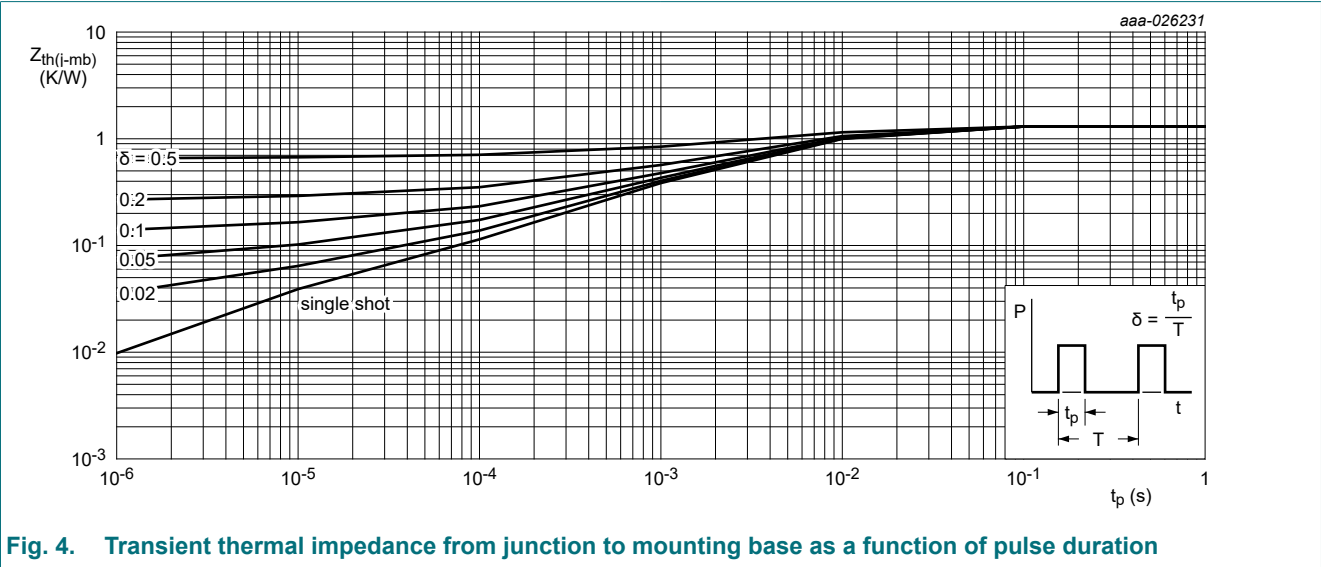
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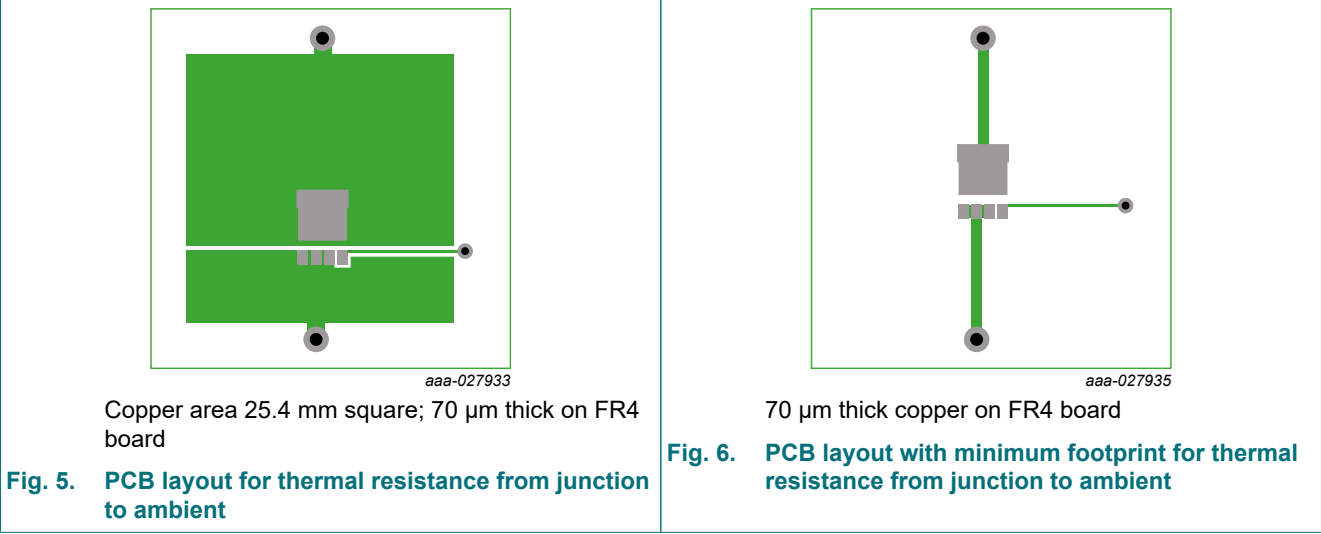
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.18	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W



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10. Characteristics

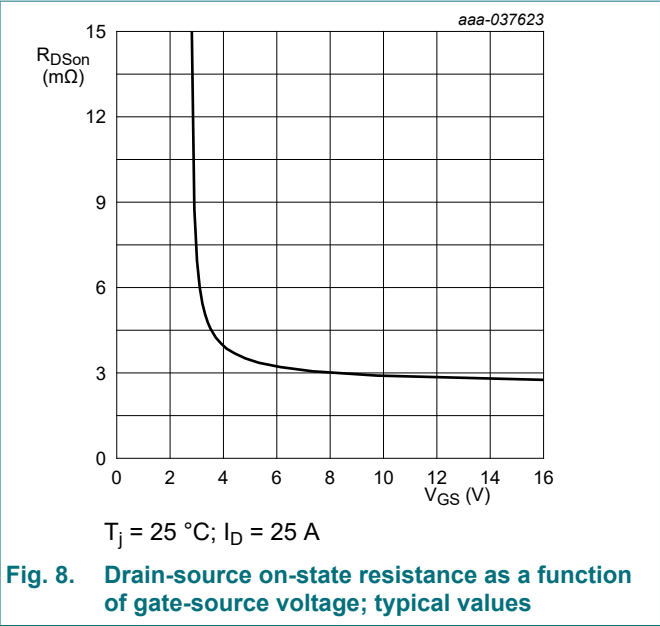
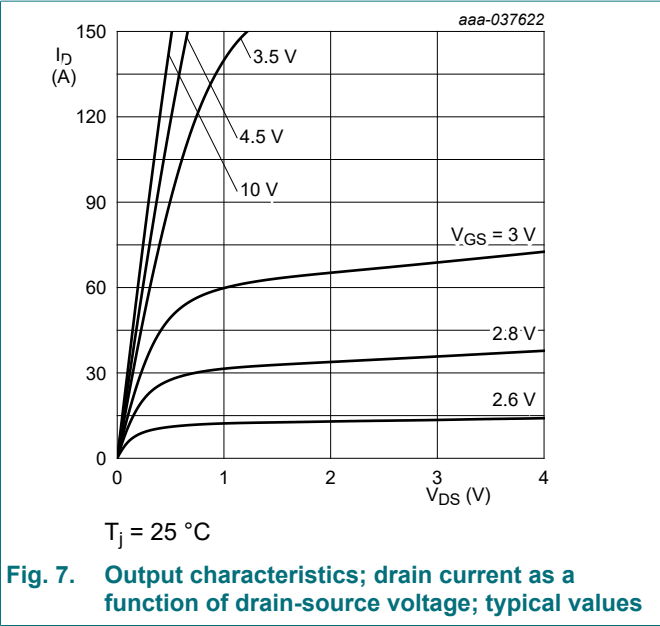
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	40	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C	1.35	1.8	2.05	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 150 °C	-	-4.7	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 32 V; V _{GS} = 0 V; T _J = 25 °C	-	0.01	1	μA
		V _{DS} = 32 V; V _{GS} = 0 V; T _J = 125 °C	-	1	-	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 10	-	2.9	3.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 11	-	-	6.4	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _J = 25 °C; Fig. 10	-	3.6	4.2	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _J = 175 °C; Fig. 11	-	-	8.1	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C	0.3	0.7	1.8	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; T _J = 25 °C; Fig. 12; Fig. 13	12	19	27	nC
		I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 12; Fig. 13	27	42	59	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C	-	40	-	nC

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 12 ; Fig. 13		4.6	7.7	12	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			2.7	4.5	6.8	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			1.8	3	4.5	nC
Q_{GD}	gate-drain charge			1.3	4.2	8.4	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 12 ; Fig. 13		-	2.8	-	V
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14		1955	3008	4211	pF
C_{oss}	output capacitance			644	991	1387	pF
C_{rss}	reverse transfer capacitance			30	99	218	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}$; $R_L = 0.8\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$; $T_j = 25\text{ }^{\circ}\text{C}$		-	17	-	ns
t_r	rise time			-	21	-	ns
$t_{d(off)}$	turn-off delay time			-	19	-	ns
t_f	fall time			-	12	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	29	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15		-	0.8	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 16		-	24	-	ns
Q_r	recovered charge		[1]	-	14	-	nC
t_a	reverse recovery rise time			-	12	-	ns
t_b	reverse recovery fall time			-	12	-	ns

[1] includes capacitive recovery



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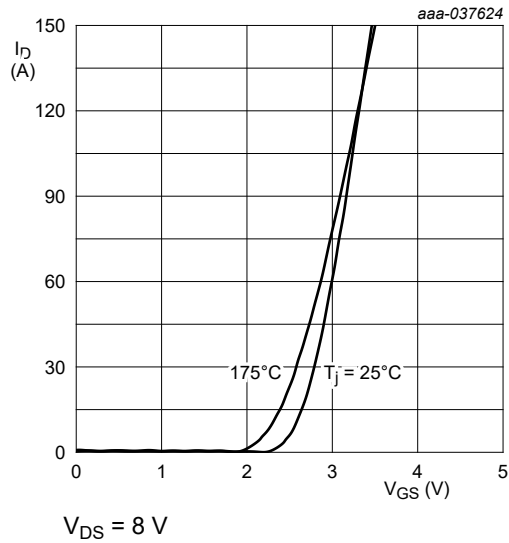


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

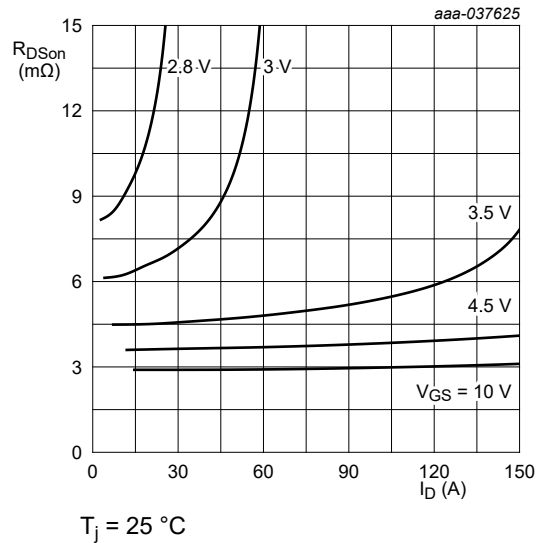


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

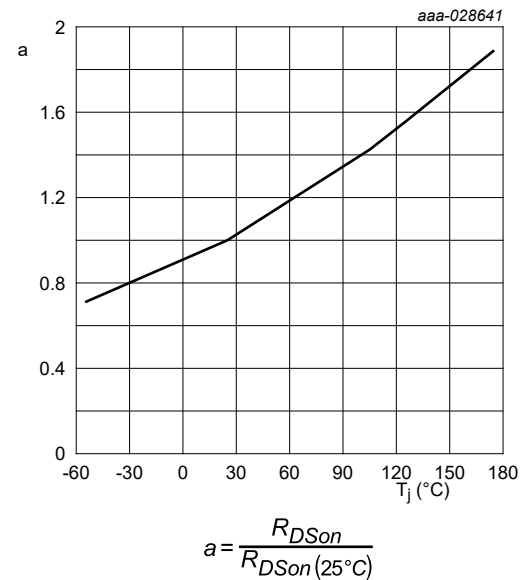


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

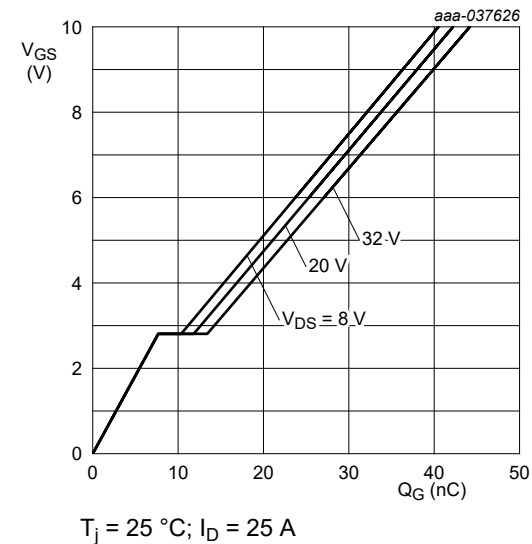


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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Fig. 13. Gate charge waveform definitions

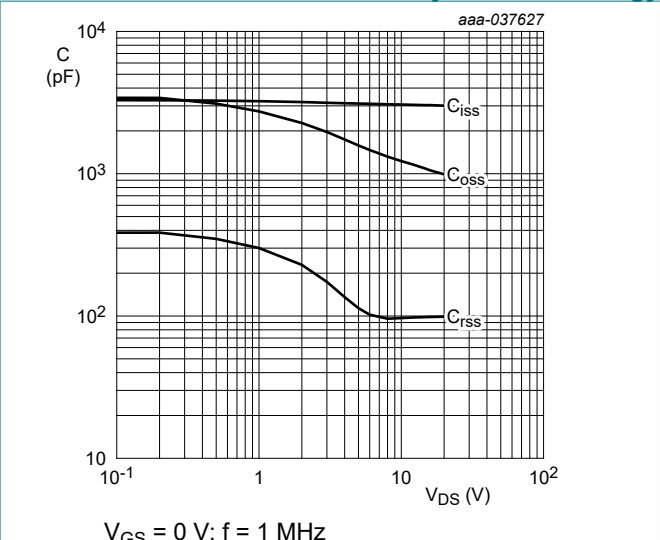


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

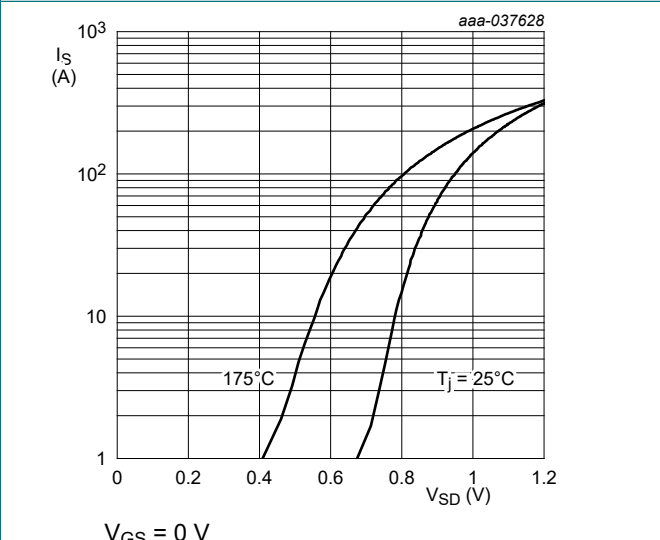


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

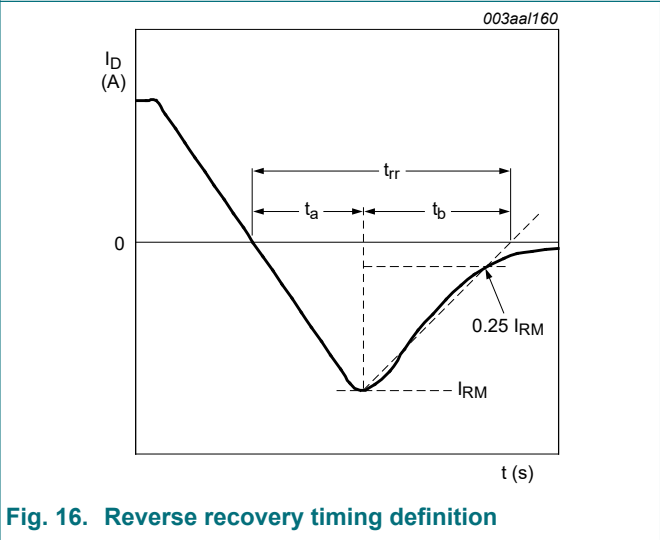


Fig. 16. Reverse recovery timing definition

11. Package outline

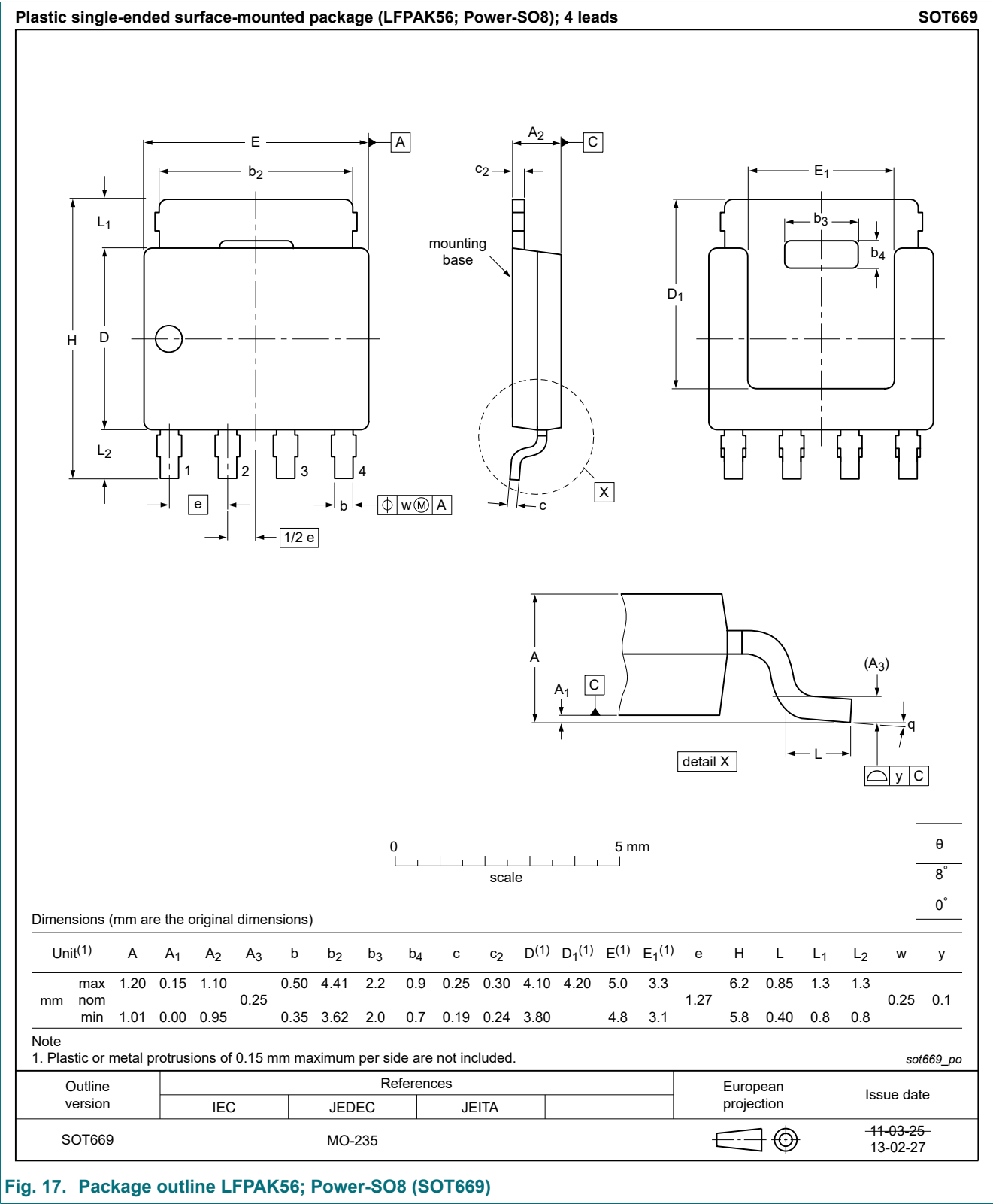


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

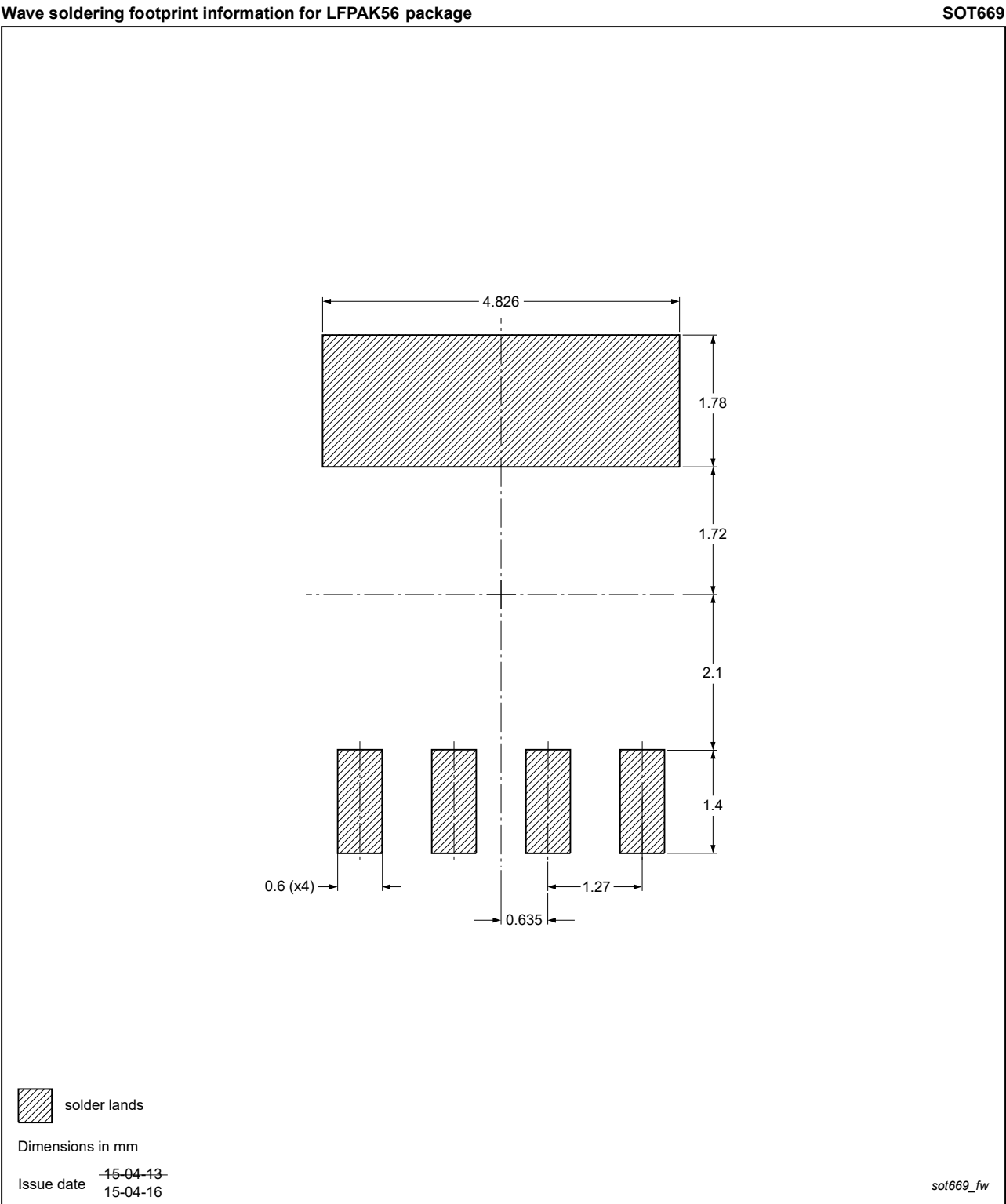


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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