

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J15FV

High-Speed Switching Applications

Analog Switch Applications

- Optimum for high-density mounting in small packages
- Low on-resistance : $R_{DS(ON)} = 12\ \Omega$ (max) (@ $V_{GS} = -4\text{ V}$)
: $R_{DS(ON)} = 32\ \Omega$ (max) (@ $V_{GS} = -2.5\text{ V}$)

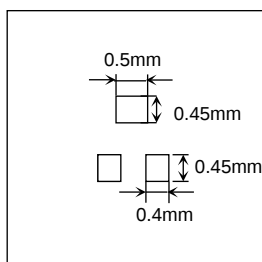
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V _{DSS}	−30	V
Gate-Source voltage		V _{GSS}	±20	V
Drain current	DC	I _D	−100	mA
	Pulse	I _{DP}	−200	
Power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW
Channel temperature		T _{ch}	150	°C
Storage temperature range		T _{stg}	−55 to 150	°C

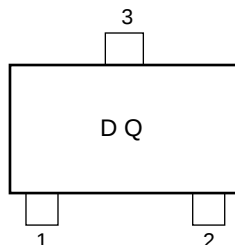
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

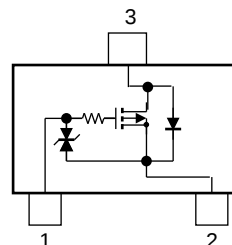
Note 1: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.585 mm²)



Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2003-04

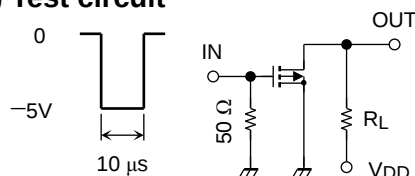
Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	MIN	TYP.	MAX	UNIT
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Drain-Source breakdown voltage	$V_{(BR) DSS}$	$I_D = -0.1 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-1.1	—	-1.7	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA}$ (Note 2)	20	—	—	mS
Drain-Source on-resistance	$R_{DS(ON)}$	$I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V}$ (Note 2)	—	8	12	Ω
		$I_D = -1 \text{ mA}, V_{GS} = -2.5 \text{ V}$ (Note 2)	—	14	32	
Input capacitance	C_{iss}	$V_{DS} = -3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	9.1	—	pF
Reverse transfer capacitance	C_{rss}		—	3.5	—	pF
Output capacitance	C_{oss}		—	8.6	—	pF
Switching time	Turn-on time	$V_{DD} = -5 \text{ V}, I_D = -10 \text{ mA},$ $V_{GS} = 0 \text{ to } -5 \text{ V}$	—	65	—	ns
	Turn-off time		—	175	—	

Note 2: Pulse Test

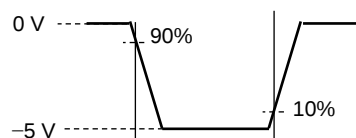
Switching Time Test Circuit

(a) Test circuit

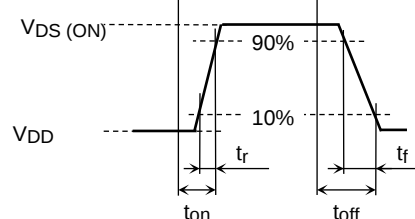


$V_{DD} = -5 \text{ V}$
Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
($Z_{out} = 50 \Omega$)
Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}



(c) V_{OUT}

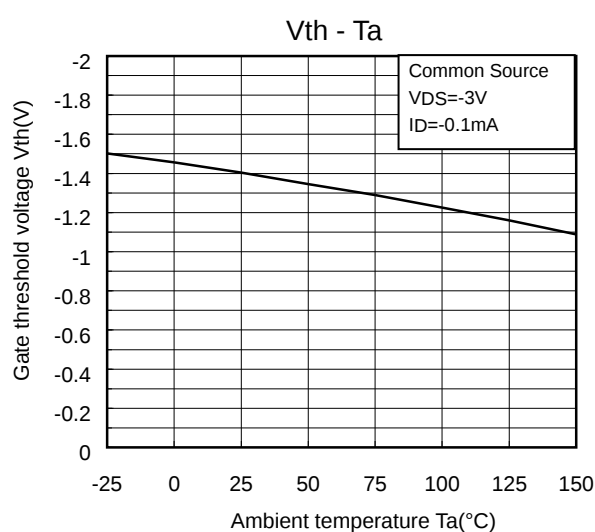
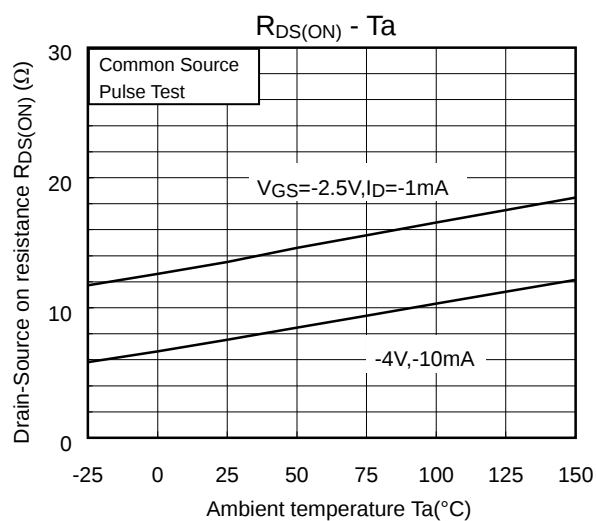
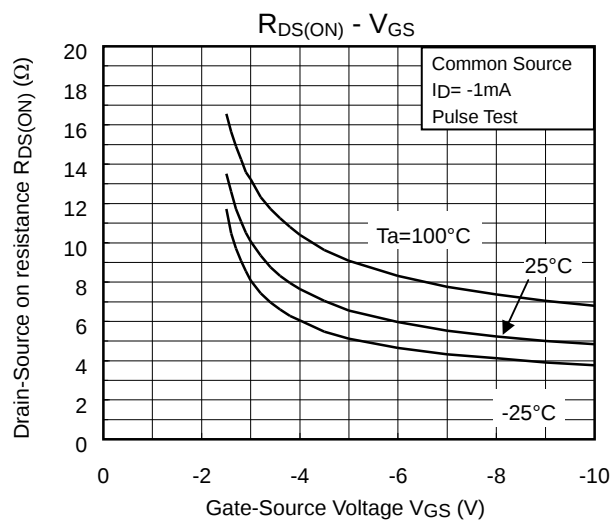
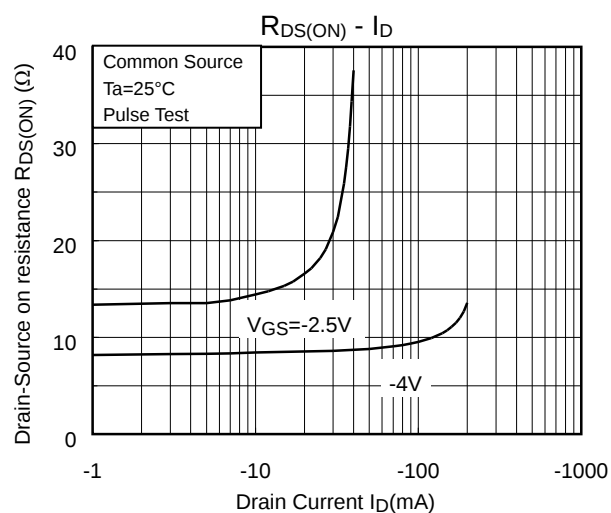
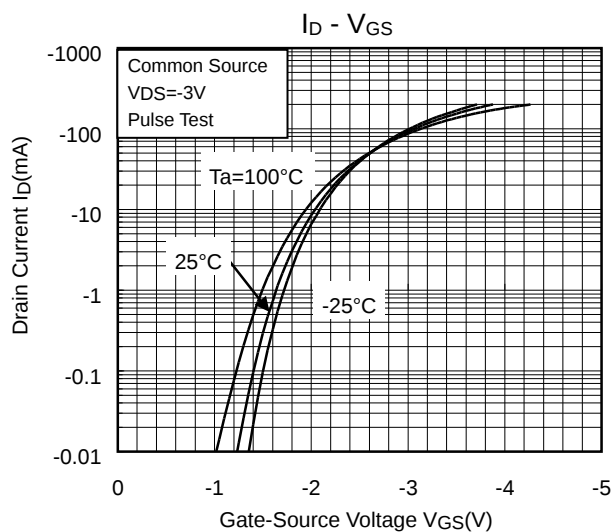
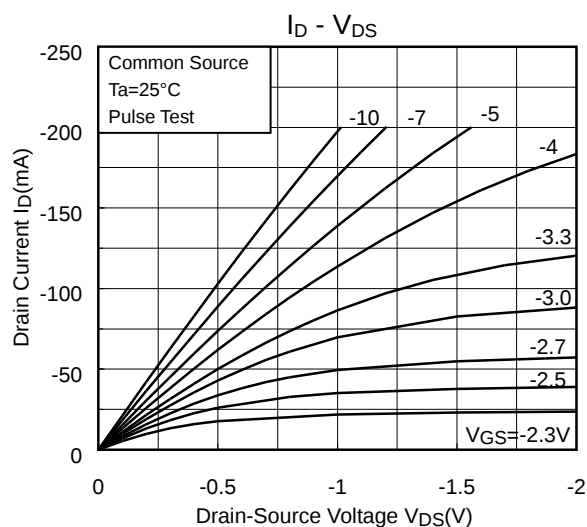


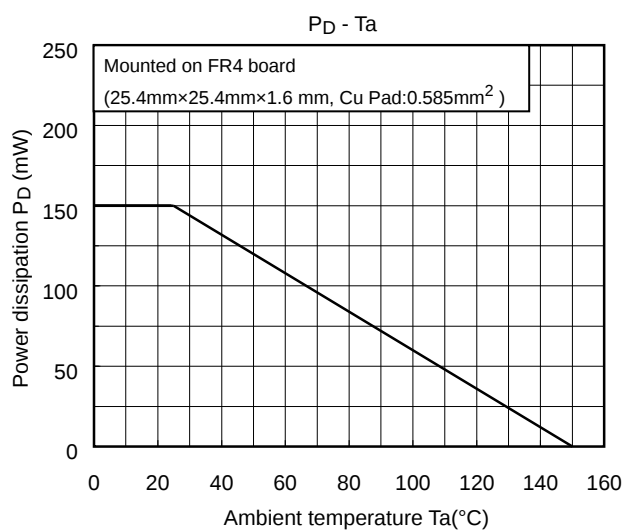
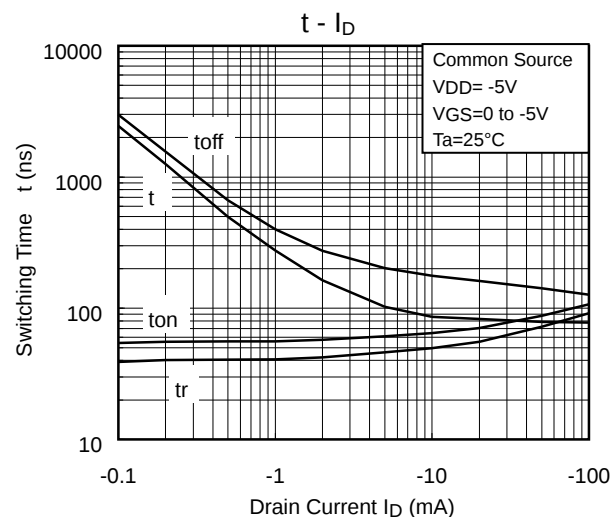
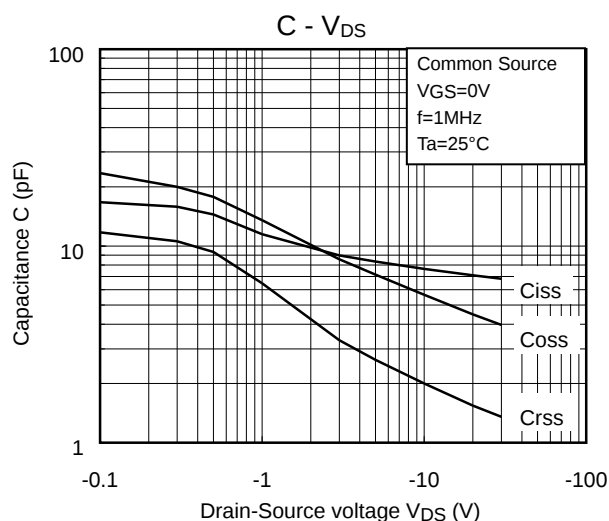
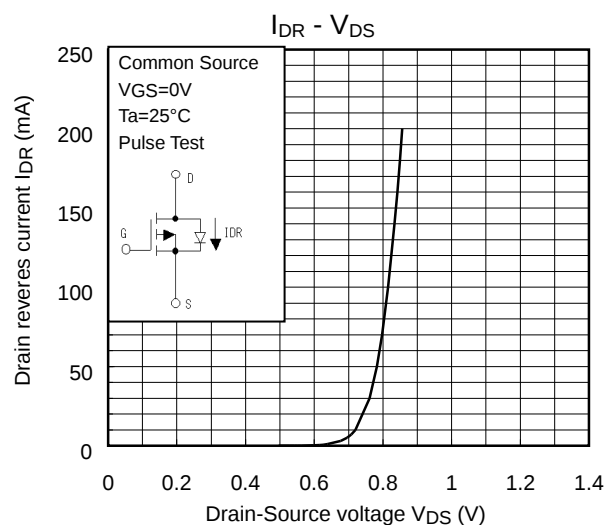
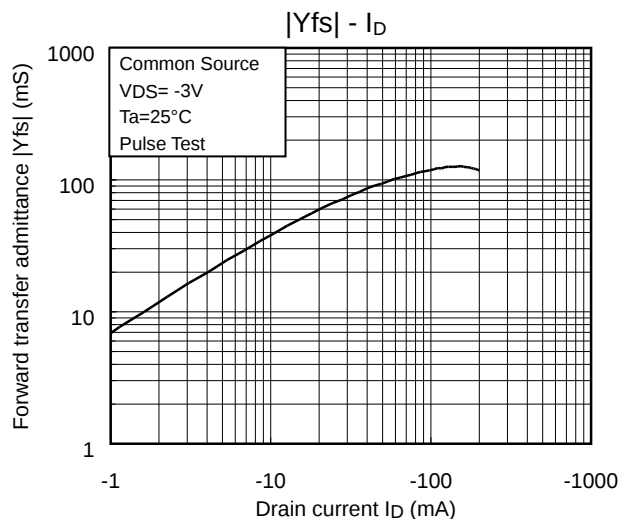
Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = -100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} and $V_{GS(OFF)}$ requires a lower voltage than V_{th} .

(The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration when using the device.





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