



# PSMN1R4-40YLD

N-channel 40 V, 1.4 m $\Omega$ , 240 A logic level MOSFET in LFPAK56 using NextPower-S3 technology

30 November 2017

Product data sheet

## 1. General description

240 Amp, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- 240 A capability
- Avalanche rated, 100% tested at  $I_{AS} = 190$  A
- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low  $Q_{RR}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high  $I_{DSS}$  leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power SO8) package, copper-clip, solder die attach and qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power OR-ing

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	238	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.38	1.85	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.12	1.4	m $\Omega$

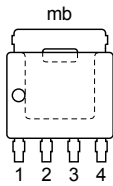
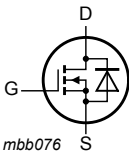
N-channel 40 V, 1.4 mΩ, 240 A logic level MOSFET in LFAK56 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	13	-	nC
$Q_{G(\text{tot})}$	total gate charge		-	45	-	nC

[1] 240A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LFAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R4-40YLD	LFAK56; Power-SO8	Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R4-40YLD	1D440L

## 8. Limiting values

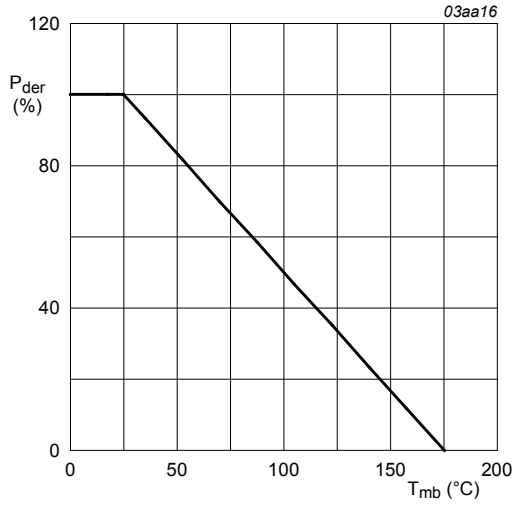
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20\text{ ns}$ ; $f \leq 500\text{ kHz}$ ; $E_{DS(AL)} \leq 200\text{ nJ}$ ; pulsed		-	45	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	238	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	<a href="#">[1]</a>	-	240	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>		-	214	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>		-	1201	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
$V_{ESD}$	electrostatic discharge voltage	HBM		2	-	kV
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	198.6	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	1201	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 74\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 0.23\text{ ms}$	<a href="#">[2]</a>	-	446	mJ
		$I_D = 25\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 2.52\text{ ms}$	<a href="#">[2]</a>	-	1641	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $R_{GS} = 50\text{ }\Omega$	<a href="#">[2]</a>	-	190	A

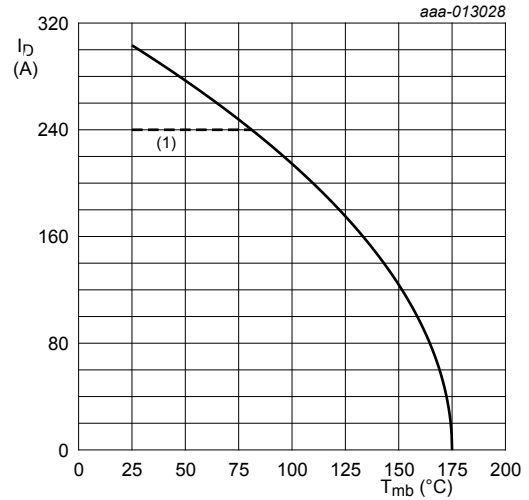
[1] 240A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.

[2] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



(1) 240A Continuous current has been successfully demonstrate during application tests. Practically the current will be limited by PCB, thermal design and operation temperature.  
 $V_{GS} \geq 10\text{ V}$

Fig. 2. Continuous drain current as a function of mounting base temperature

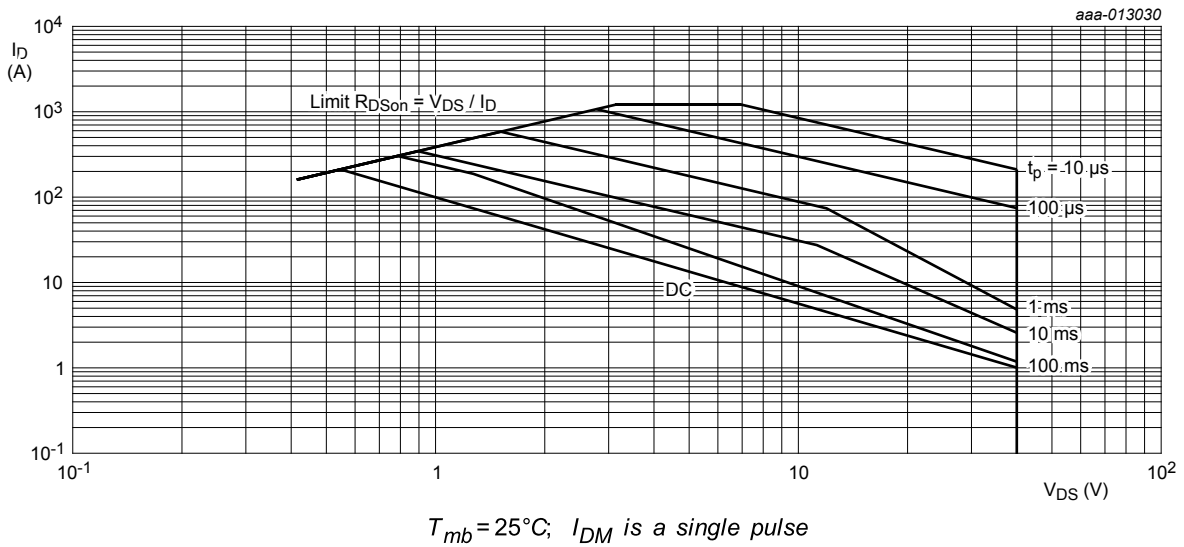


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>	-	50	-	K/W
		<a href="#">Fig. 6</a>	-	125	-	K/W

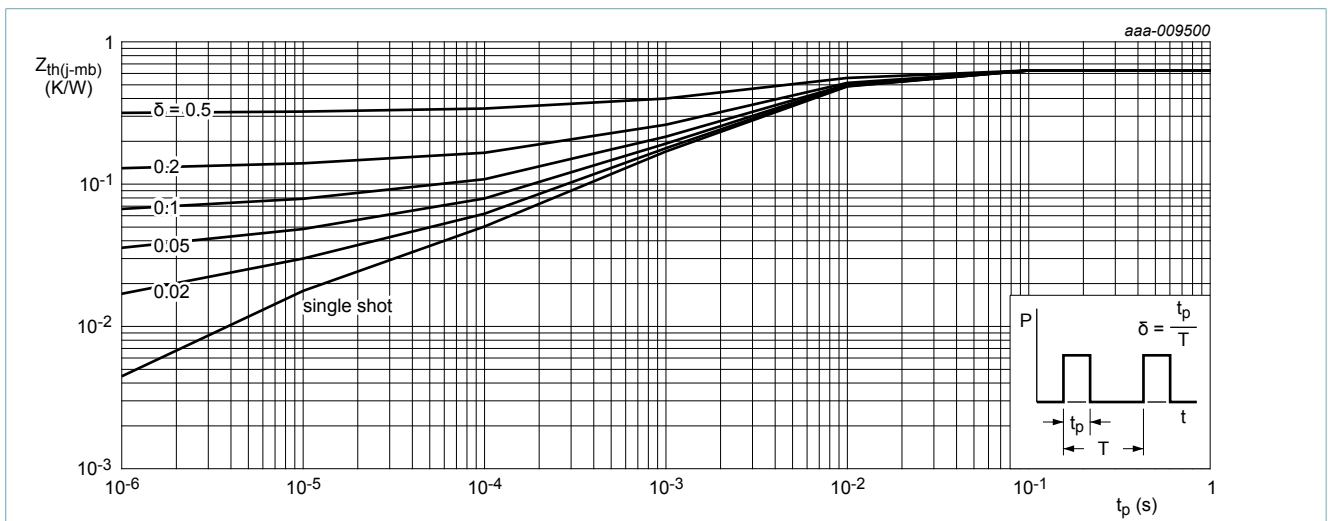


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-005750

aaa-005751

**Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper**

**Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint;FR4 board; 2oz copper**

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.05	1.7	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.8	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	12	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	-	1.12	1.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	2.65	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	-	1.38	1.85	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	3.4	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.1	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	96	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	45	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	85	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	15	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6	-	nC
$Q_{GD}$	gate-drain charge		-	13	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	-	6661	-	pF
$C_{oss}$	output capacitance		-	1543	-	pF
$C_{rss}$	reverse transfer capacitance		-	299	-	pF

N-channel 40 V, 1.4 mΩ, 240 A logic level MOSFET in LPAK56 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 0.8\ \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\ \Omega$	-	39	-	ns
$t_r$	rise time		-	49	-	ns
$t_{d(off)}$	turn-off delay time		-	47	-	ns
$t_f$	fall time		-	30	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	50	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; \text{Fig. 16}$	-	47	-	ns
$Q_r$	recovered charge		[1]	61	-	nC
$t_a$	reverse recovery rise time		-	25.4	-	ns
$t_b$	reverse recovery fall time		-	21.7	-	ns

[1] includes capacitive recovery

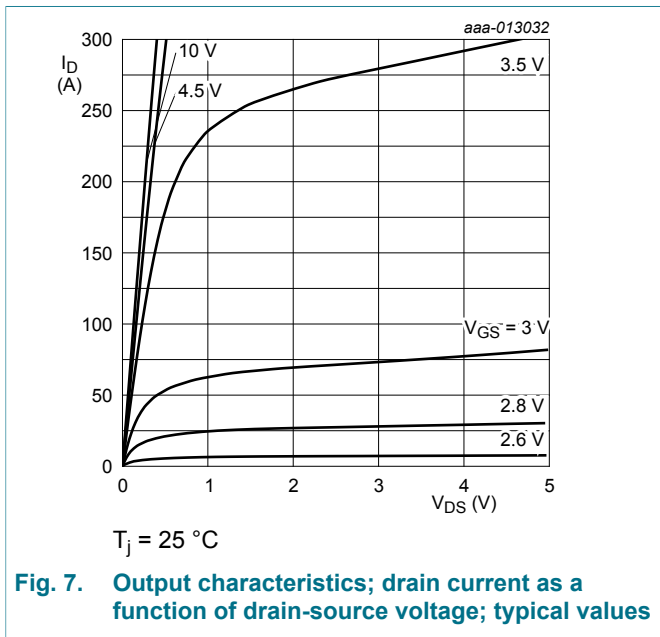


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

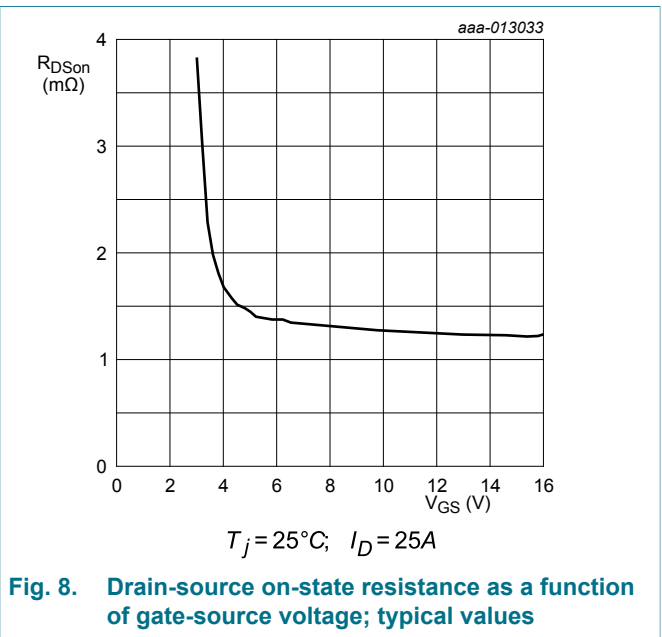


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

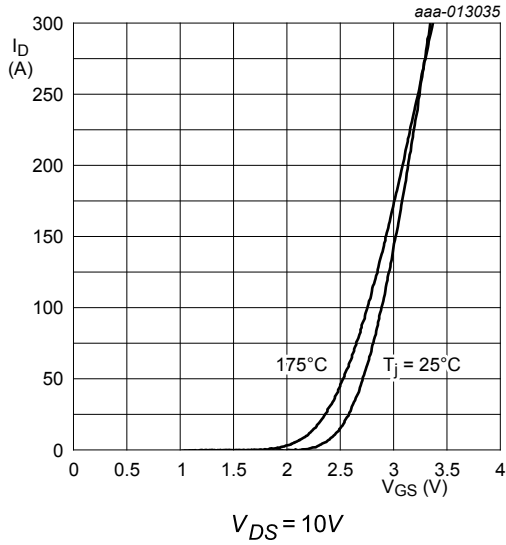


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

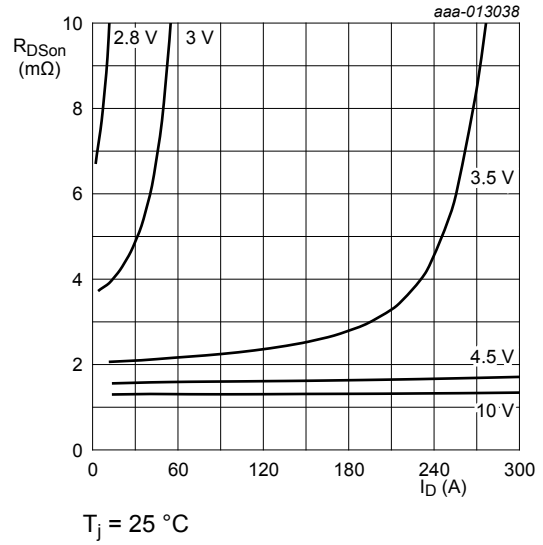
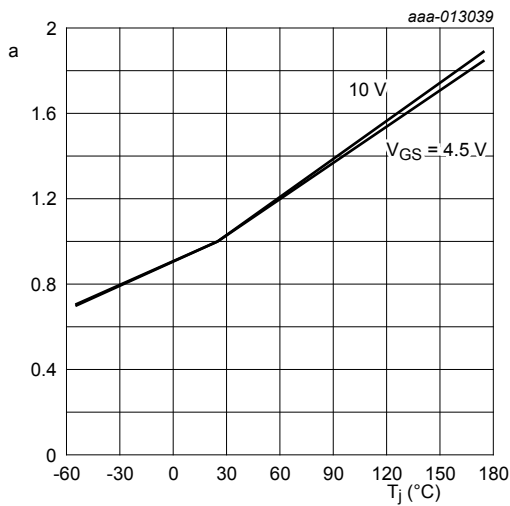


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon} (25^\circ C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

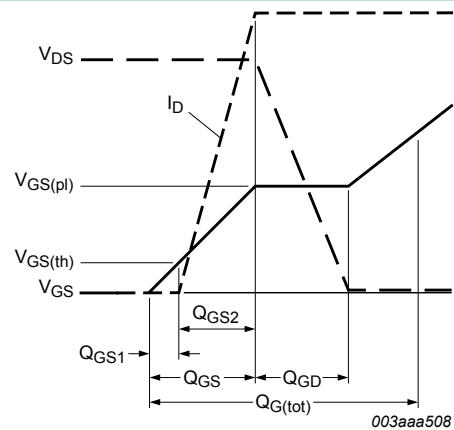


Fig. 12. Gate charge waveform definitions

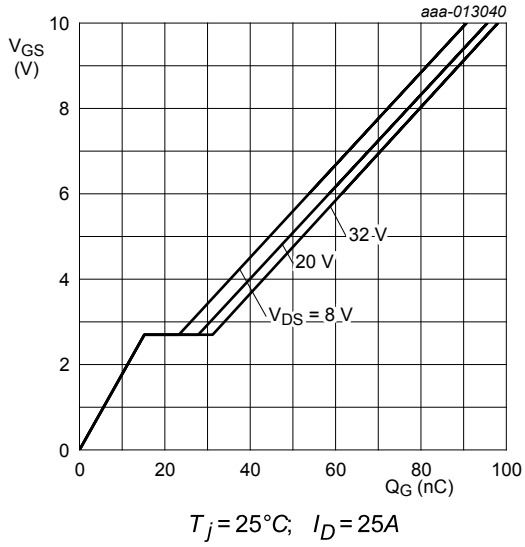


Fig. 13. Gate-source voltage as a function of gate charge; typical values

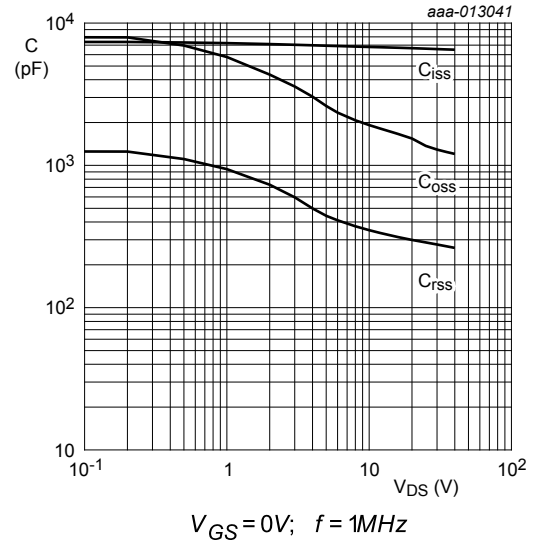


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

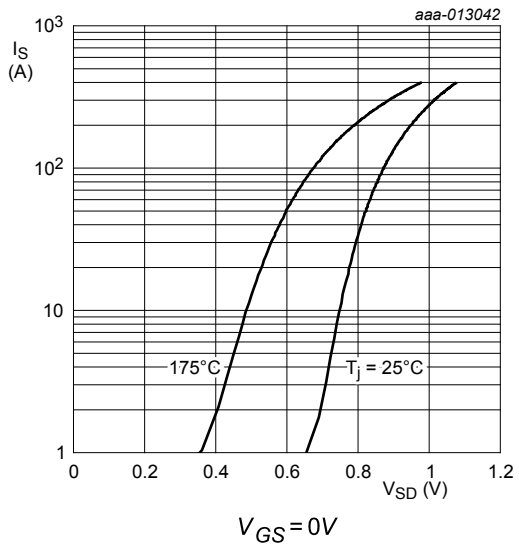


Fig. 15. Source current as a function of source-drain voltage; typical values

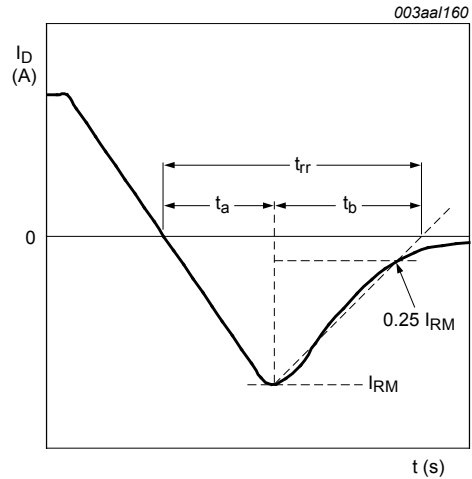
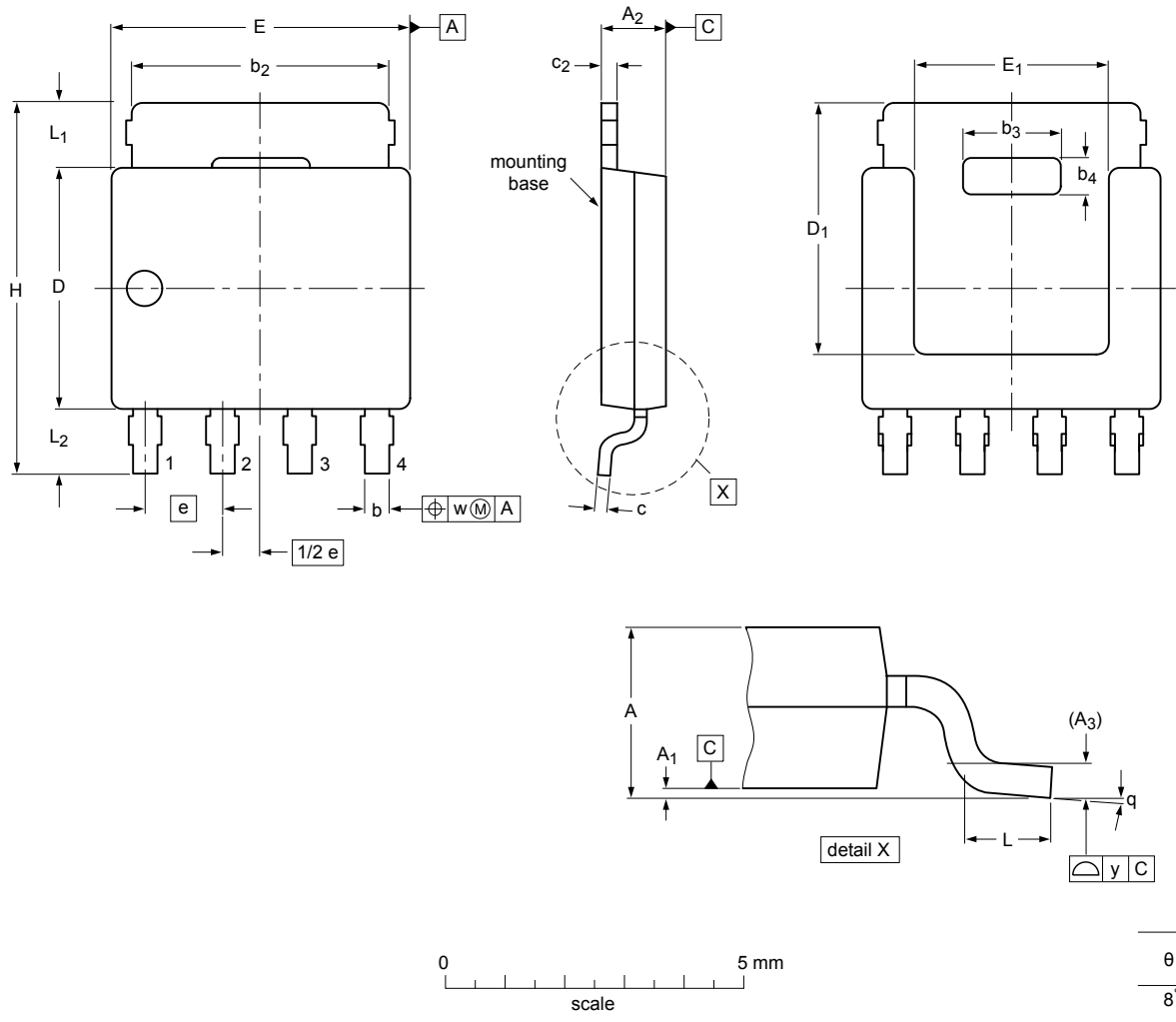


Fig. 16. Reverse recovery timing definition

### 11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3	1.27	6.2	0.85	1.3	1.3		
nom				0.25																0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT669		MO-235			-11-03-25- 13-02-27

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)



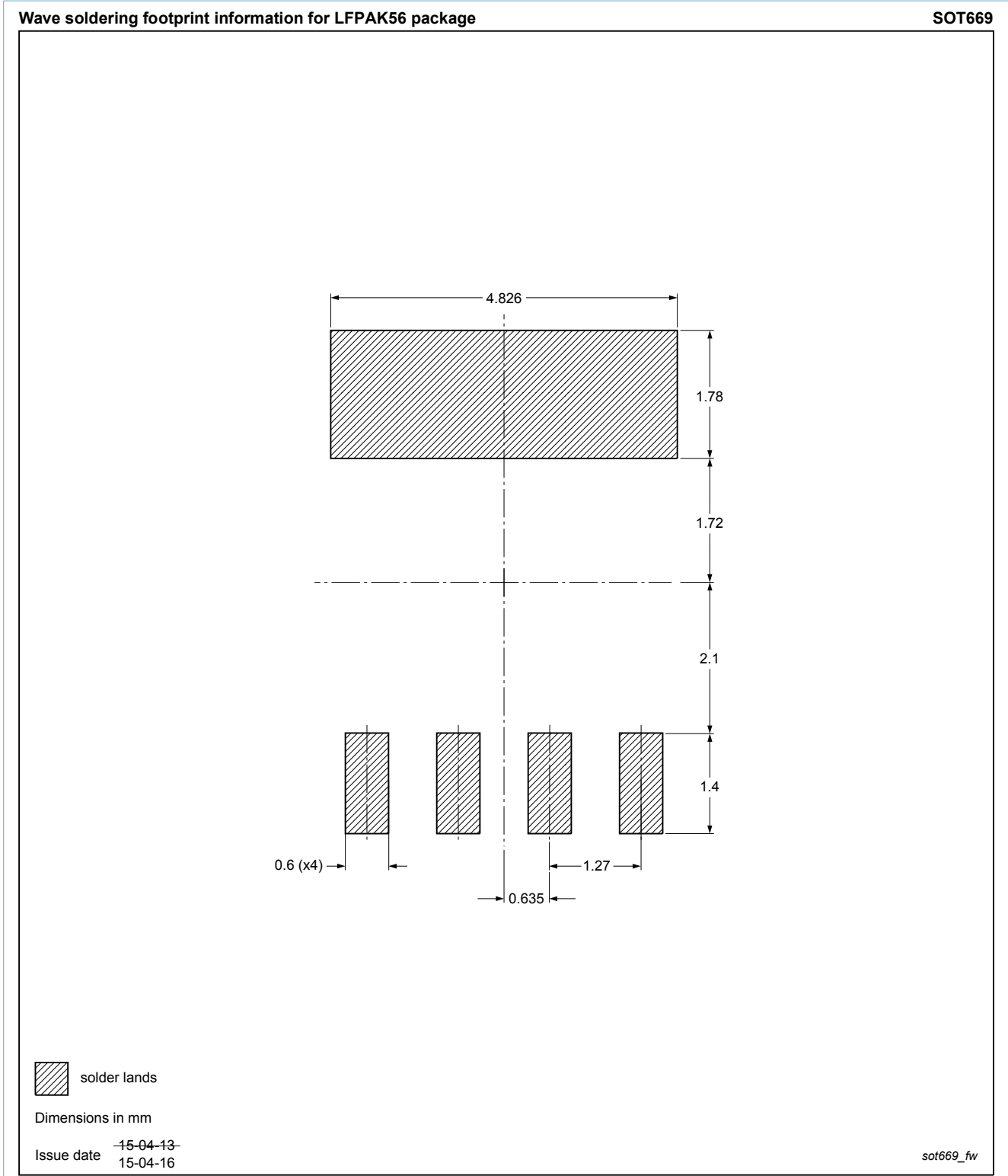


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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**N-channel 40 V, 1.4 mΩ, 240 A logic level MOSFET in LPAK56 using NextPower-S3 technology**

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## 14. Contents

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1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	5
10. Characteristics.....	6
11. Package outline.....	10
12. Soldering.....	11
13. Legal information.....	13

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For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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