



# PSMN1R9-40YSB

N-channel 40 V, 1.9 mOhm, 200 A standard level MOSFET in LPAK56 using optimized NextPowerS3 Schottky-Plus technology

13 February 2024

Product data sheet

## 1. General description

200 A, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56 package, using advanced TrenchMOS Superjunction technology with optimization to provide improved EMC performance (up to 6 dB). This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- Optimized for improved EMC Performance
- 200 A continuous  $I_{D(max)}$  rating
- Avalanche rated, 100% tested at  $I_{AS} = 180$  A
- Strong SOA (linear-mode) rating
- NextPowerS3 technology delivers 'superfast switching with soft body-diode recovery'
- Low  $Q_{rr}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low  $V_{SD}$ , low  $Q_{rr}$ , soft recovery and low  $I_{DSS}$  leakage
- High reliability LPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints providing excellent board level reliability
- Low parasitic inductance and resistance

## 3. Applications

- Automation, control and instrumentation
- Autonomous systems, Robotics and Cobots
- DC-to-DC converters
- Brushless DC motor control
- Brushed motors
- Battery isolation
- Industrial load-switch and eFuse
- Inrush management, hotswap

## 4. Quick reference data

Table 1. Quick reference data

| Symbol                        | Parameter                        | Conditions                                                                                    |     | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|-----------------------------------------------------------------------------------------------|-----|-----|-----|-----|------|
| $V_{DS}$                      | drain-source voltage             | $25\text{ °C} \leq T_j \leq 175\text{ °C}$                                                    |     | -   | -   | 40  | V    |
| $I_D$                         | drain current                    | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>                     | [1] | -   | -   | 200 | A    |
| $P_{tot}$                     | total power dissipation          | $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>                                              |     | -   | -   | 194 | W    |
| $T_j$                         | junction temperature             |                                                                                               |     | -55 | -   | 175 | °C   |
| <b>Static characteristics</b> |                                  |                                                                                               |     |     |     |     |      |
| $R_{DS(on)}$                  | drain-source on-state resistance | $V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a> |     | -   | 1.6 | 1.9 | mΩ   |

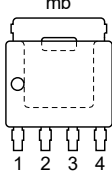
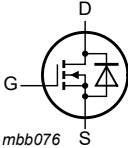
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| Symbol                  | Parameter         | Conditions                                                             | Min | Typ | Max | Unit |
|-------------------------|-------------------|------------------------------------------------------------------------|-----|-----|-----|------|
| Dynamic characteristics |                   |                                                                        |     |     |     |      |
| Q <sub>GD</sub>         | gate-drain charge | I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; | 2   | 7.6 | 15  | nC   |
| Q <sub>G(tot)</sub>     | total gate charge | T <sub>j</sub> = 25 °C; Fig. 12; Fig. 13                               | 36  | 56  | 78  | nC   |

[1] 200 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline                                                                                              | Graphic symbol                                                                                |
|-----|--------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| 1   | S      | source                            | <br>LPAK56; Power-SO8 (SOT669) | <br>mbb076 |
| 2   | S      | source                            |                                                                                                                 |                                                                                               |
| 3   | S      | source                            |                                                                                                                 |                                                                                               |
| 4   | G      | gate                              |                                                                                                                 |                                                                                               |
| mb  | D      | mounting base; connected to drain |                                                                                                                 |                                                                                               |

6. Ordering information

Table 3. Ordering information

| Type number   | Package           |                                                            |         |
|---------------|-------------------|------------------------------------------------------------|---------|
|               | Name              | Description                                                | Version |
| PSMN1R9-40YSB | LPAK56; Power-SO8 | plastic, single-ended surface-mounted package; 4 terminals | SOT669  |

7. Marking

Table 4. Marking codes

| Type number   | Marking code |
|---------------|--------------|
| PSMN1R9-40YSB | 1B9S40Y      |

8. Limiting values

Table 5. Limiting values

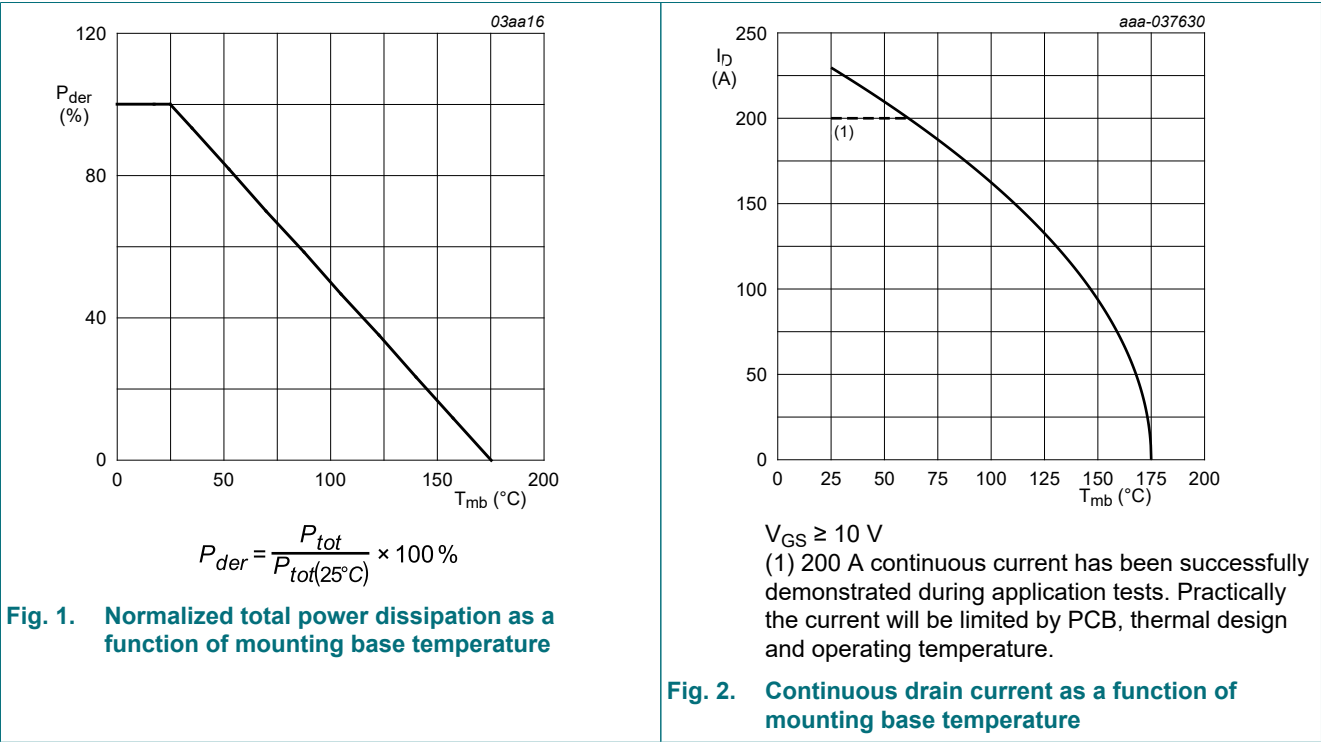
In accordance with the Absolute Maximum Rating System (IEC 60134). T<sub>j</sub> = 25 °C unless otherwise stated.

| Symbol           | Parameter                 | Conditions                                                                | Min | Max | Unit |
|------------------|---------------------------|---------------------------------------------------------------------------|-----|-----|------|
| V <sub>DS</sub>  | drain-source voltage      | 25 °C ≤ T <sub>j</sub> ≤ 175 °C                                           | -   | 40  | V    |
| V <sub>DSM</sub> | peak drain-source voltage | t <sub>p</sub> ≤ 20 ns; f = 500 kHz; E <sub>DS(AL)</sub> ≤ 200 nJ; pulsed | -   | 45  | V    |
| V <sub>DGR</sub> | drain-gate voltage        | 25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ                  | -   | 40  | V    |
| V <sub>GS</sub>  | gate-source voltage       |                                                                           | -20 | 20  | V    |
| P <sub>tot</sub> | total power dissipation   | T <sub>mb</sub> = 25 °C; Fig. 1                                           | -   | 194 | W    |
| I <sub>D</sub>   | drain current             | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2                   | [1] | 200 | A    |
|                  |                           | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2                  | -   | 162 | A    |
| I <sub>DM</sub>  | peak drain current        | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3           | -   | 919 | A    |

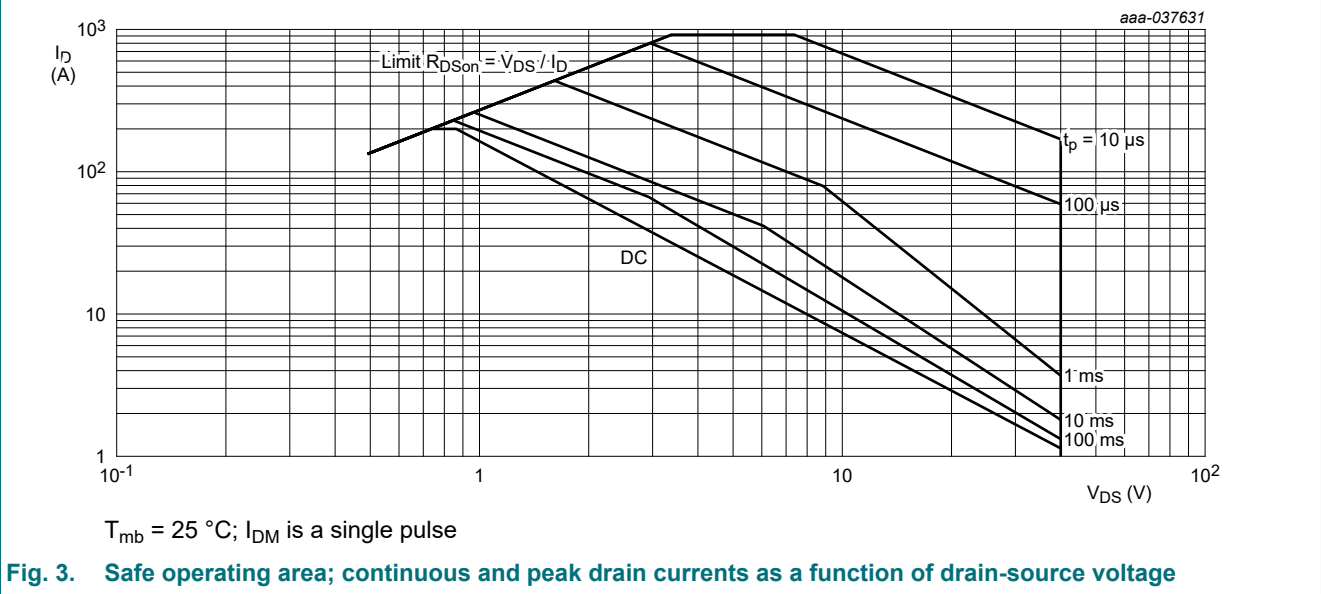
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| Symbol               | Parameter                                    | Conditions                                                                                                                                                         |     | Min | Max | Unit |
|----------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| T <sub>stg</sub>     | storage temperature                          |                                                                                                                                                                    |     | -55 | 175 | °C   |
| T <sub>j</sub>       | junction temperature                         |                                                                                                                                                                    |     | -55 | 175 | °C   |
| T <sub>slid(M)</sub> | peak soldering temperature                   |                                                                                                                                                                    |     | -   | 260 | °C   |
| Source-drain diode   |                                              |                                                                                                                                                                    |     |     |     |      |
| I <sub>S</sub>       | source current                               | T <sub>mb</sub> = 25 °C                                                                                                                                            |     | -   | 194 | A    |
| I <sub>SM</sub>      | peak source current                          | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C                                                                                                            |     | -   | 919 | A    |
| Avalanche ruggedness |                                              |                                                                                                                                                                    |     |     |     |      |
| E <sub>DS(AL)S</sub> | non-repetitive drain-source avalanche energy | I <sub>D</sub> = 60.8 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 202 μs | [2] | -   | 319 | mJ   |
|                      |                                              | I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 1.4 ms   | [2] | -   | 905 | mJ   |
| I <sub>AS</sub>      | non-repetitive avalanche current             | V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω                                                              | [2] | -   | 180 | A    |

- [1] 200 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



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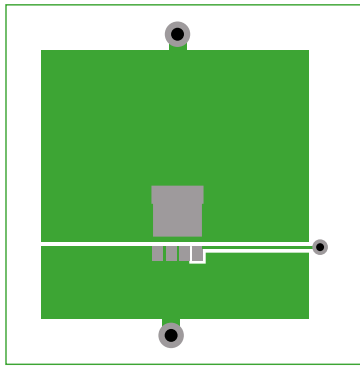
## 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter                                         | Conditions | Min | Typ  | Max  | Unit |
|----------------|---------------------------------------------------|------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4     | -   | 0.69 | 0.77 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | Fig. 5     | -   | 42   | -    | K/W  |
|                |                                                   | Fig. 6     | -   | 85   | -    | K/W  |

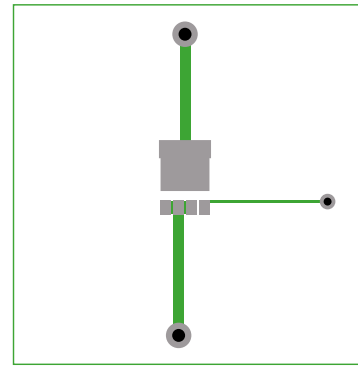


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Copper area 25.4 mm square; 70 μm thick on FR4 board

**Fig. 5. PCB layout for thermal resistance from junction to ambient**



70 μm thick copper on FR4 board

**Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient**

## 10. Characteristics

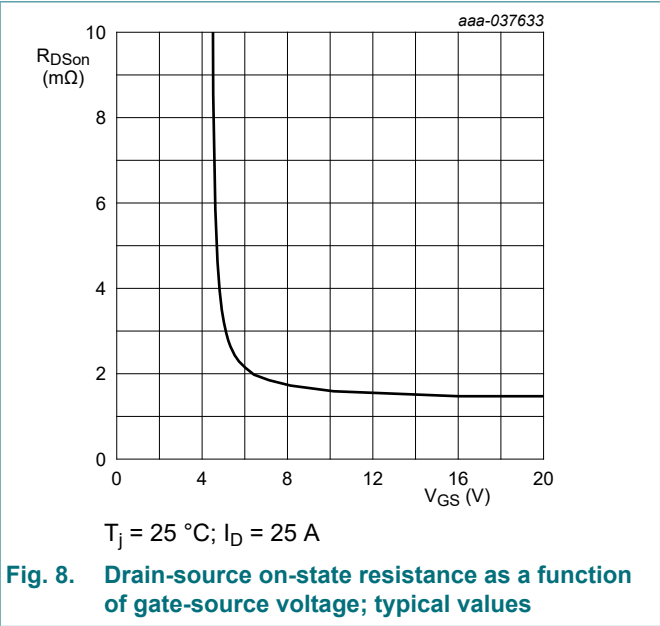
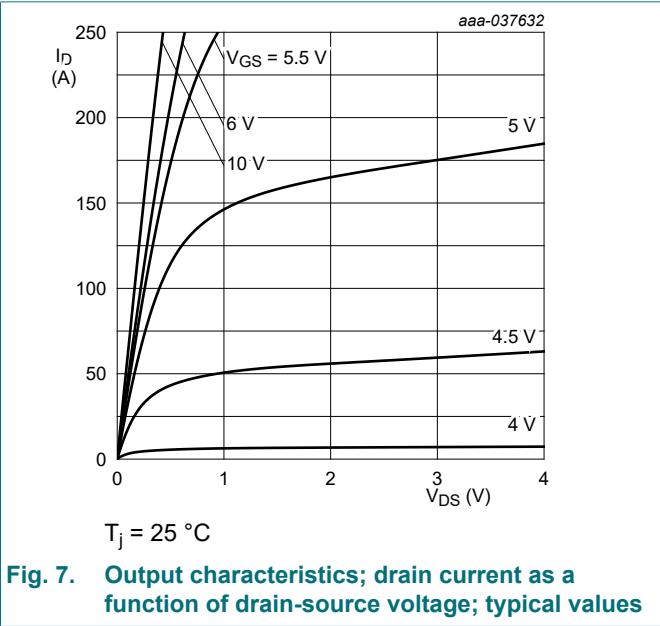
**Table 7. Characteristics**

| Symbol                         | Parameter                                                | Conditions                                                                                                           | Min | Typ  | Max | Unit       |
|--------------------------------|----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----|------|-----|------------|
| <b>Static characteristics</b>  |                                                          |                                                                                                                      |     |      |     |            |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage                           | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$                                                                    | 40  | -    | -   | V          |
|                                |                                                          | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$                                                                   | 36  | -    | -   | V          |
| $V_{GS(th)}$                   | gate-source threshold voltage                            | $I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$                                                                      | 2.4 | 3.1  | 3.6 | V          |
| $\Delta V_{GS(th)}/\Delta T$   | gate-source threshold voltage variation with temperature | $25^\circ C \leq T_j \leq 150^\circ C$                                                                               | -   | -7.2 | -   | mV/K       |
| $I_{DSS}$                      | drain leakage current                                    | $V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25^\circ C$                                                                      | -   | 0.01 | 1   | $\mu A$    |
|                                |                                                          | $V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125^\circ C$                                                                     | -   | 2.3  | -   | $\mu A$    |
| $I_{GSS}$                      | gate leakage current                                     | $V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$                                                                      | -   | 2    | 100 | nA         |
|                                |                                                          | $V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$                                                                     | -   | 2    | 100 | nA         |
| $R_{DS(on)}$                   | drain-source on-state resistance                         | $V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C;$<br><a href="#">Fig. 10</a>                                            | -   | 1.6  | 1.9 | m $\Omega$ |
|                                |                                                          | $V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C;$<br><a href="#">Fig. 11</a>                                           | -   | -    | 3.7 | m $\Omega$ |
| $R_G$                          | gate resistance                                          | $f = 1 MHz; T_j = 25^\circ C$                                                                                        | 0.4 | 1    | 2.5 | $\Omega$   |
| <b>Dynamic characteristics</b> |                                                          |                                                                                                                      |     |      |     |            |
| $Q_{G(tot)}$                   | total gate charge                                        | $I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$<br>$T_j = 25^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a> | 36  | 56   | 78  | nC         |
|                                |                                                          | $I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V;$<br>$T_j = 25^\circ C$                                                      | -   | 54   | -   | nC         |
| $Q_{GS}$                       | gate-source charge                                       | $I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$<br>$T_j = 25^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a> | 11  | 18   | 27  | nC         |
| $Q_{GS(th)}$                   | pre-threshold gate-source charge                         |                                                                                                                      | 7   | 12   | 18  | nC         |
| $Q_{GS(th-pl)}$                | post-threshold gate-source charge                        |                                                                                                                      | 3.6 | 6    | 9   | nC         |
| $Q_{GD}$                       | gate-drain charge                                        |                                                                                                                      | 2   | 7.6  | 15  | nC         |
| $V_{GS(pl)}$                   | gate-source plateau voltage                              | $I_D = 25 A; V_{DS} = 20 V; T_j = 25^\circ C;$<br><a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>                  | -   | 4.4  | -   | V          |

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| Symbol              | Parameter                    | Conditions                                                                                                                                |     | Min  | Typ  | Max  | Unit |
|---------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|------|
| C <sub>iss</sub>    | input capacitance            | V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz;<br>T <sub>j</sub> = 25 °C; Fig. 14                                              |     | 2924 | 4498 | 6297 | pF   |
| C <sub>oss</sub>    | output capacitance           |                                                                                                                                           |     | 915  | 1407 | 1970 | pF   |
| C <sub>rss</sub>    | reverse transfer capacitance |                                                                                                                                           |     | 55   | 183  | 403  | pF   |
| t <sub>d(on)</sub>  | turn-on delay time           | V <sub>DS</sub> = 20 V; R <sub>L</sub> = 0.8 Ω; V <sub>GS</sub> = 10 V;<br>R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C              |     | -    | 15   | -    | ns   |
| t <sub>r</sub>      | rise time                    |                                                                                                                                           |     | -    | 11   | -    | ns   |
| t <sub>d(off)</sub> | turn-off delay time          |                                                                                                                                           |     | -    | 33   | -    | ns   |
| t <sub>f</sub>      | fall time                    |                                                                                                                                           |     | -    | 13   | -    | ns   |
| Q <sub>oss</sub>    | output charge                | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; f = 1 MHz;<br>T <sub>j</sub> = 25 °C                                                       |     | -    | 44   | -    | nC   |
| Source-drain diode  |                              |                                                                                                                                           |     |      |      |      |      |
| V <sub>SD</sub>     | source-drain voltage         | I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; Fig. 15                                                             |     | -    | 0.8  | 1    | V    |
| t <sub>rr</sub>     | reverse recovery time        | I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;<br>V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C; Fig. 16 |     | -    | 33   | -    | ns   |
| Q <sub>r</sub>      | recovered charge             |                                                                                                                                           | [1] | -    | 26   | -    | nC   |
| t <sub>a</sub>      | reverse recovery rise time   |                                                                                                                                           |     | -    | 17   | -    | ns   |
| t <sub>b</sub>      | reverse recovery fall time   |                                                                                                                                           |     | -    | 15   | -    | ns   |

[1] includes capacitive recovery



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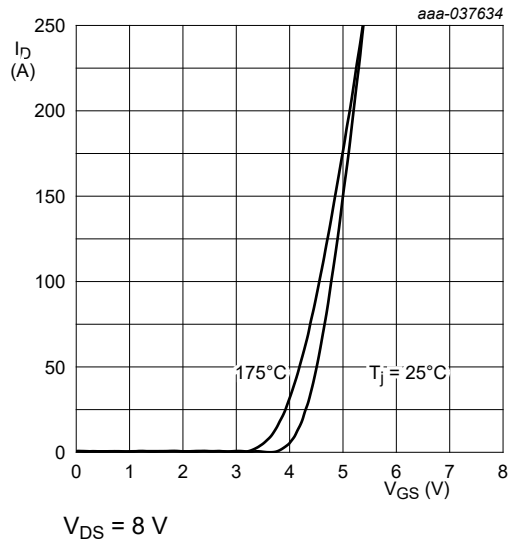


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

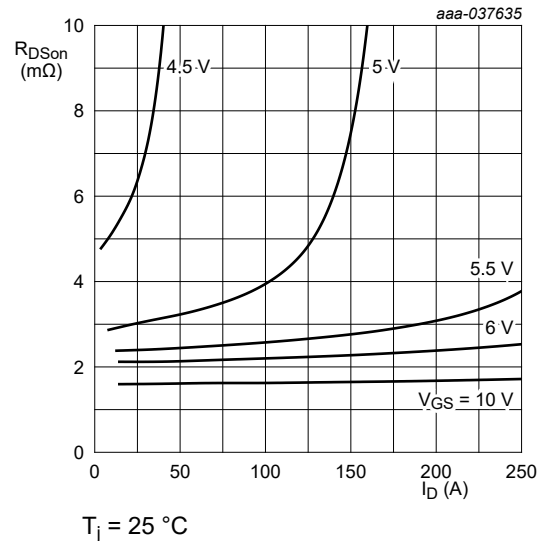


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

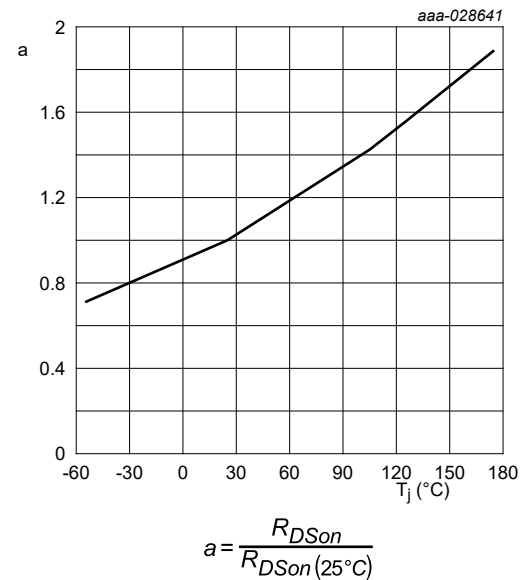


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

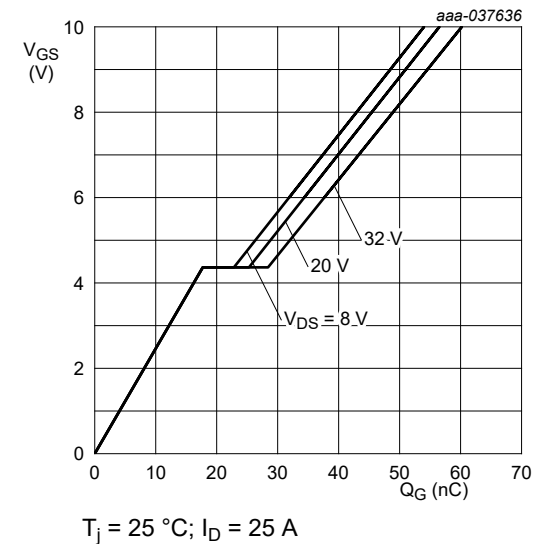


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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Fig. 13. Gate charge waveform definitions

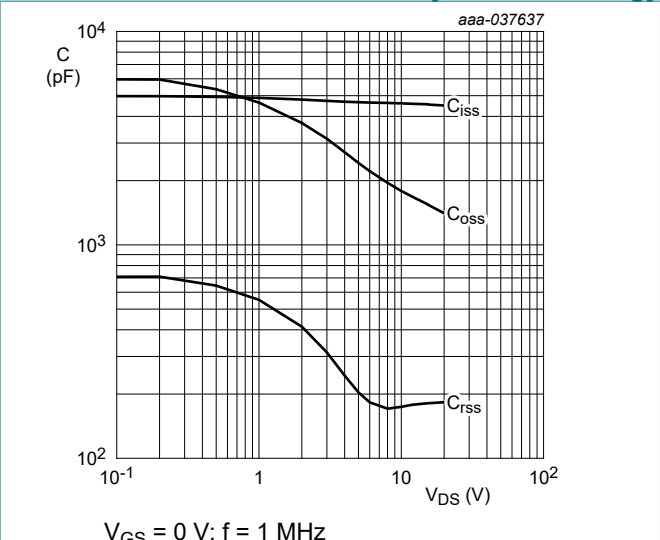


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

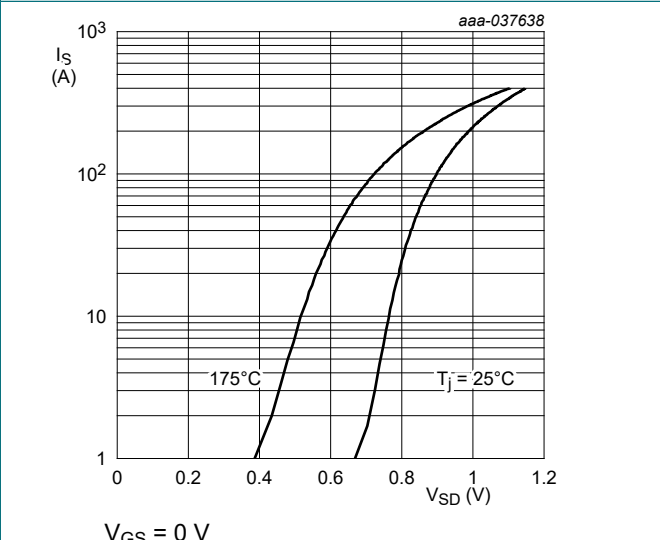


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

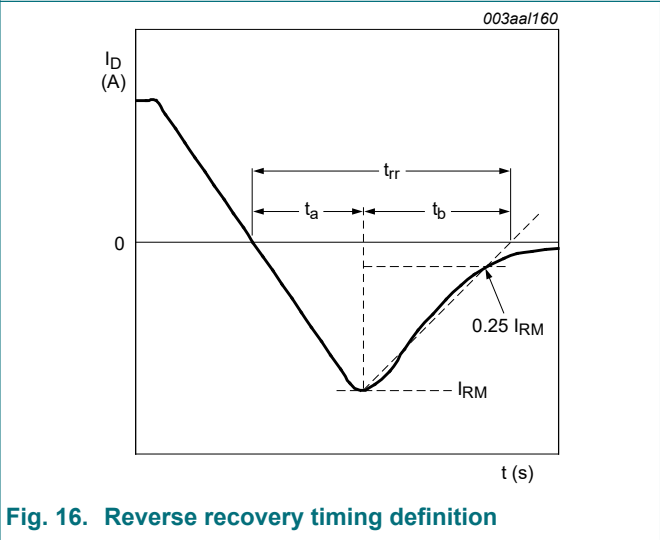


Fig. 16. Reverse recovery timing definition

11. Package outline

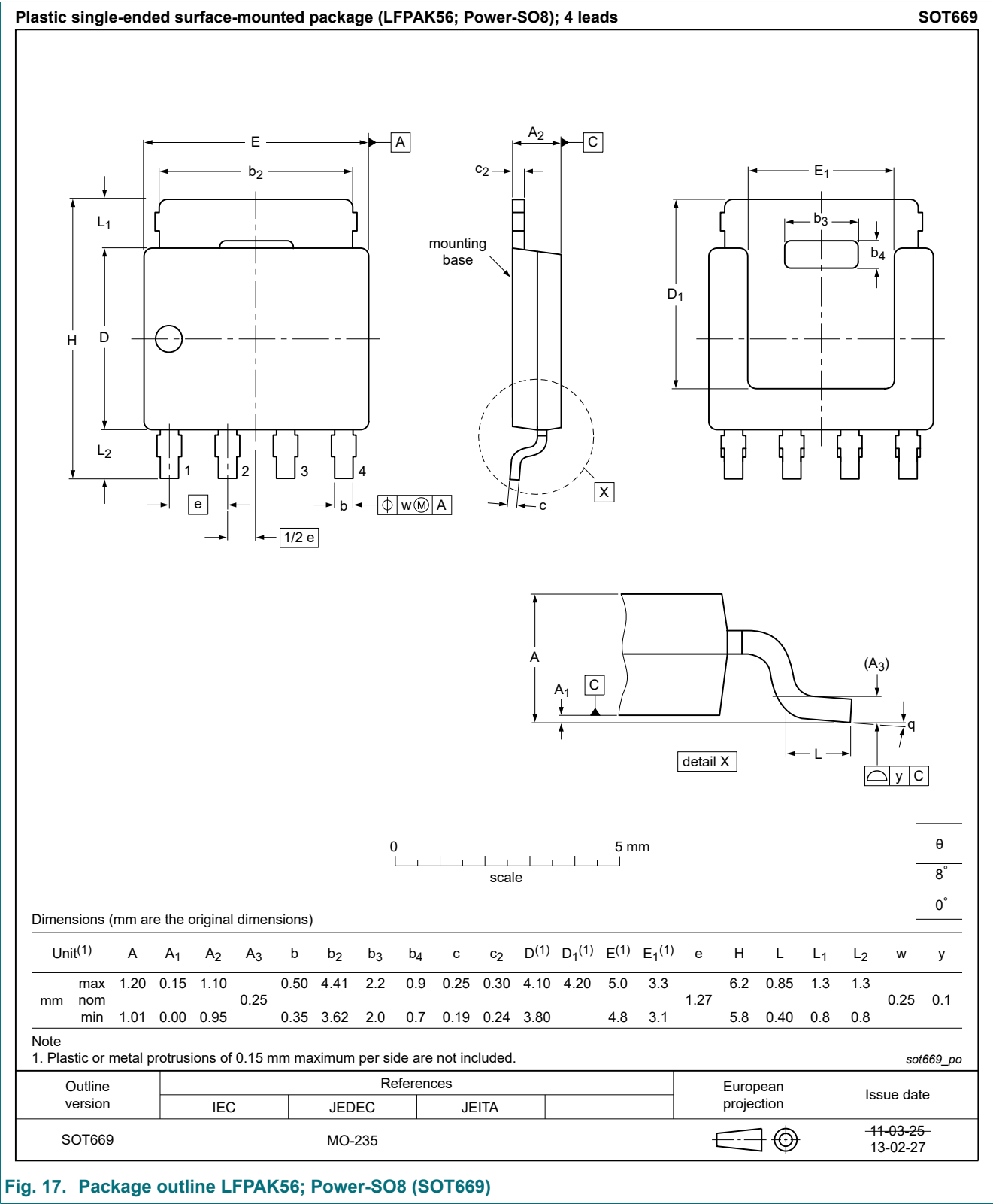
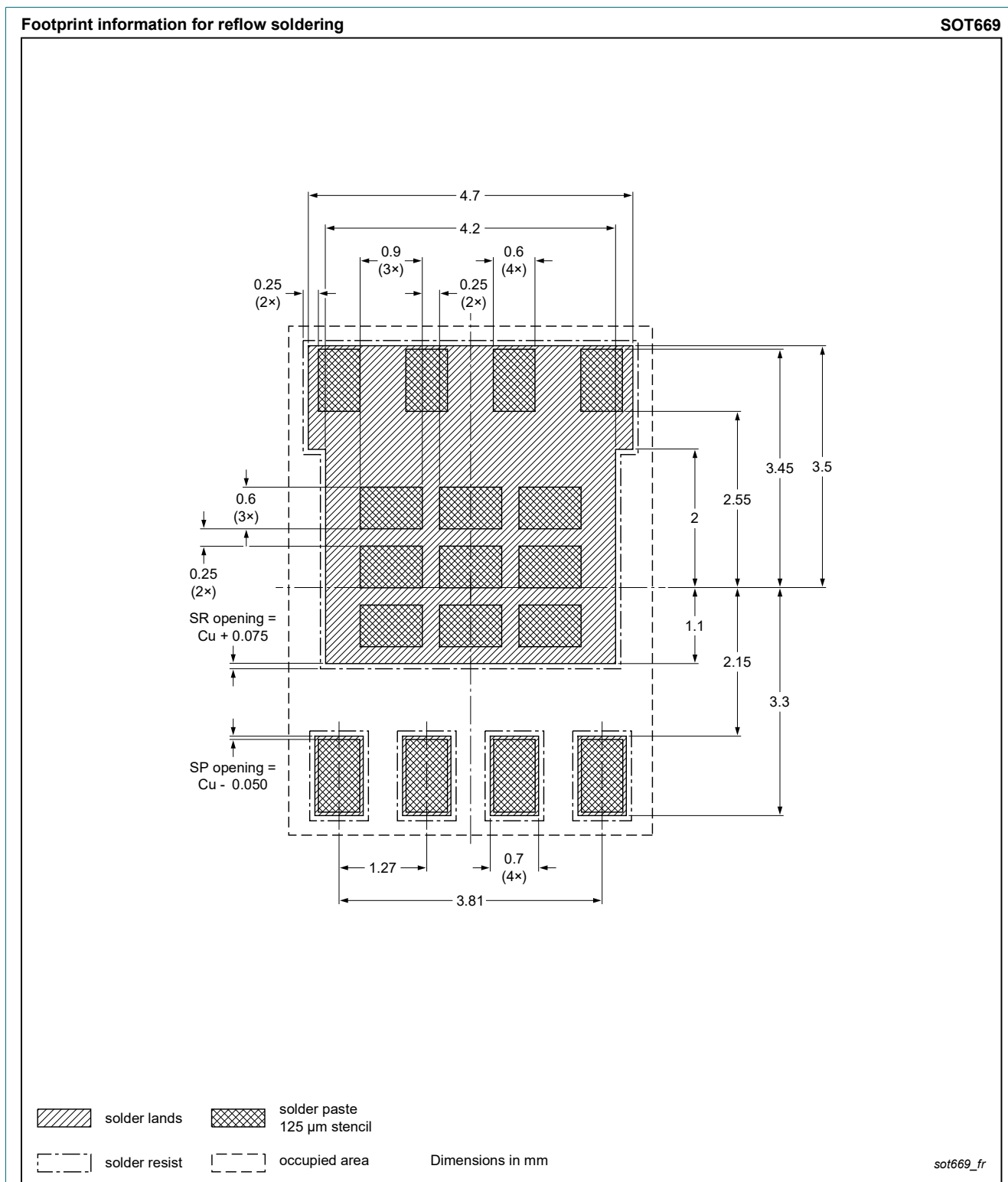


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Soldering



**Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)**

Wave soldering footprint information for LPAK56 package

SOT669

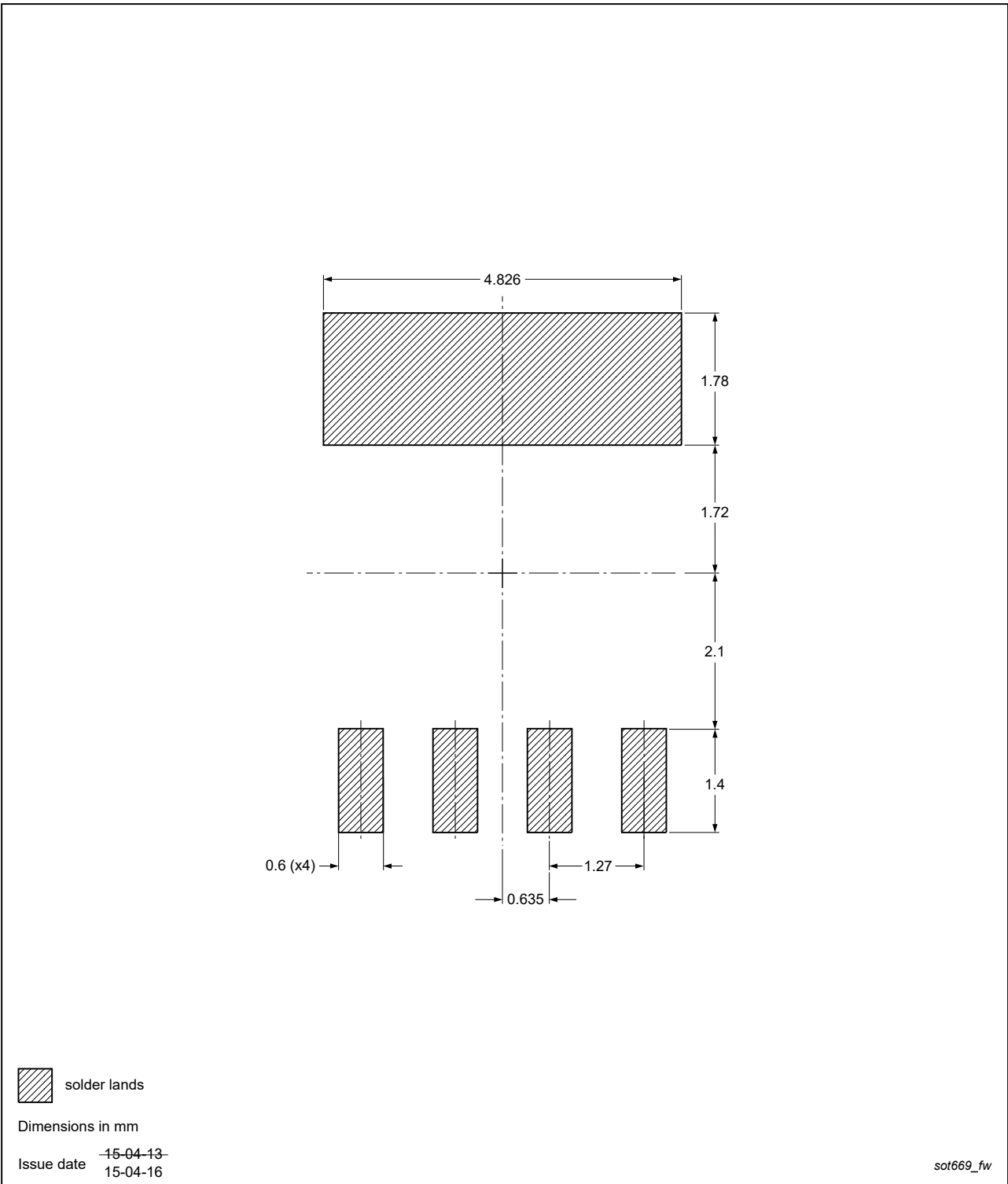


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

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13. Legal information

Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
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- [2] The term 'short data sheet' is explained in section "Definitions".
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