



PSMN4R2-80YSE

N-channel 80 V, 4.2 mOhm MOSFET with enhanced SOA in LPAK56E

25 June 2021

Preliminary data sheet

1. General description

N-channel enhancement mode MOSFET in a LPAK56E package qualified to 175 °C. Part of Nexperia's "ASFETs for hotswap" portfolio, the PSMN4R2-80YSE delivers very low $R_{DS(on)}$ and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LPAK56E package.

PSMN4R2-80YSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low $R_{DS(on)}$ to minimize I^2R losses delivering optimum efficiency when turned fully ON and an 80% smaller footprint than existing D2PAK types.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DS(on)}$ for low I^2R conduction losses
- LPAK56E package for applications that demand the highest performance and reliability in a 30 mm² footprint

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Table 1. General characteristics data

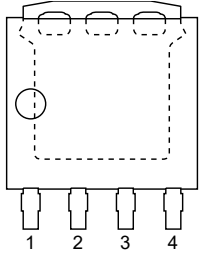
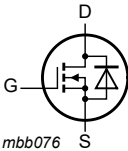
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	80	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	170	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	294	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	3.2	4.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13		-	4.6	6.4	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		3	11	26	nC
Q _{G(tot)}	total gate charge			37	73	110	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 57\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; Fig. 4	[1]	-	-	374	mJ
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 18		-	35	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R2-80YSE	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R2-80YSE	4E2S80J

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$		-	80	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1		-	294	W

Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2		-	170	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	123	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	698	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	170	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	698	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 57\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[1]	-	374	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[1]	-	57	A

[1] Protected by 100% test

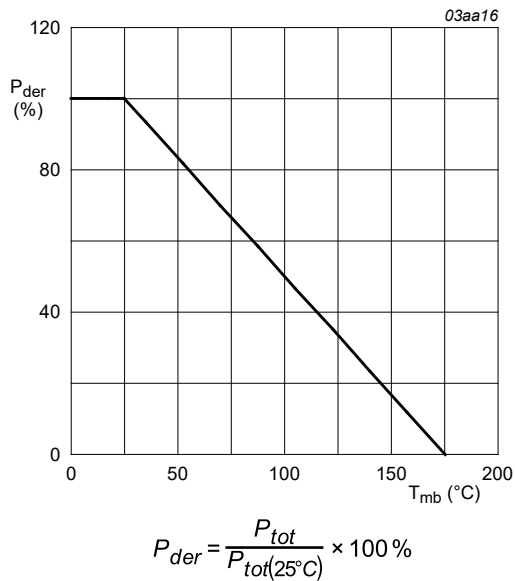
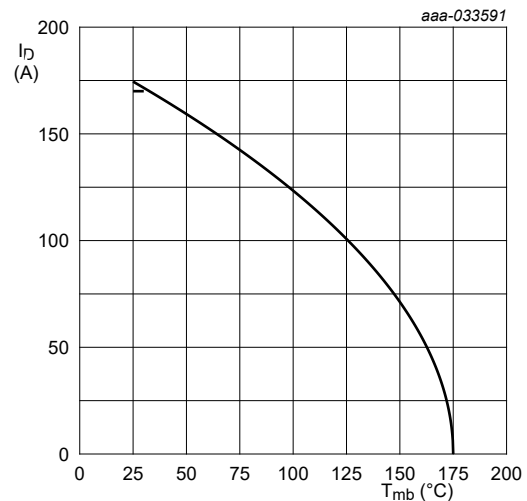


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$

(1) 170A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

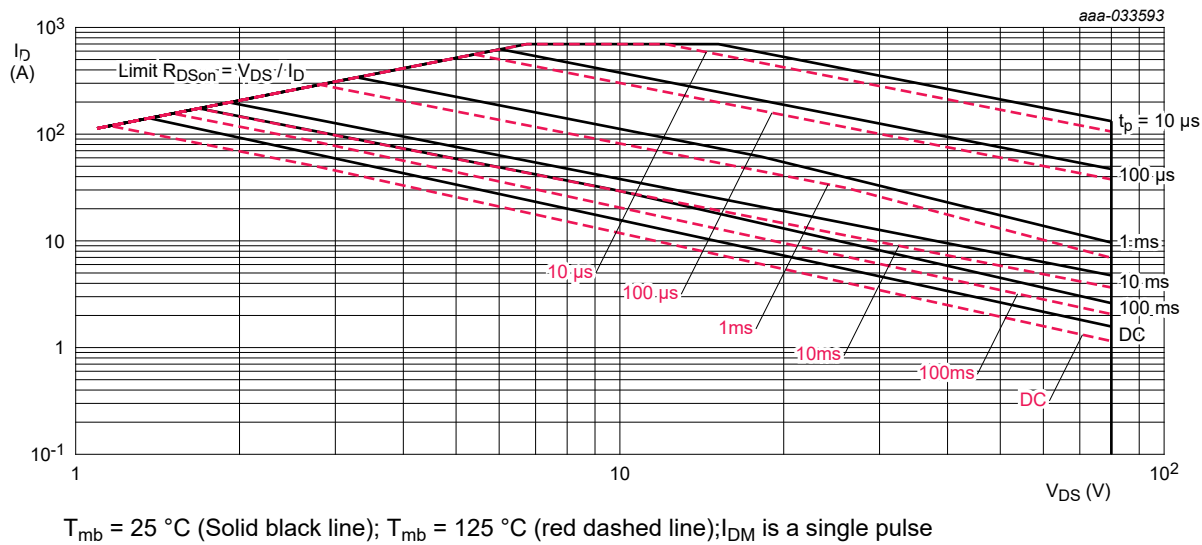


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

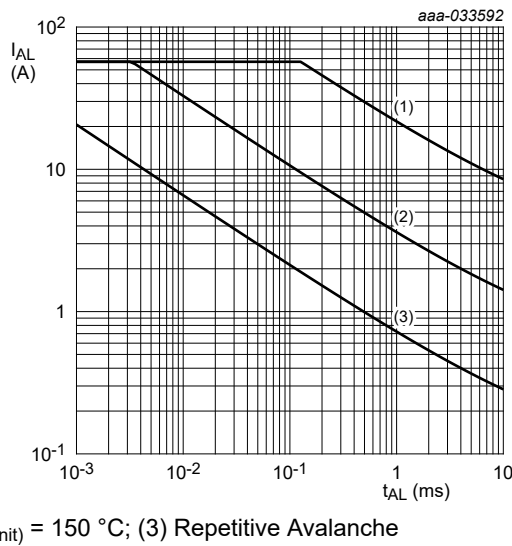


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	42	-	K/W
		Fig. 7	-	85	-	K/W

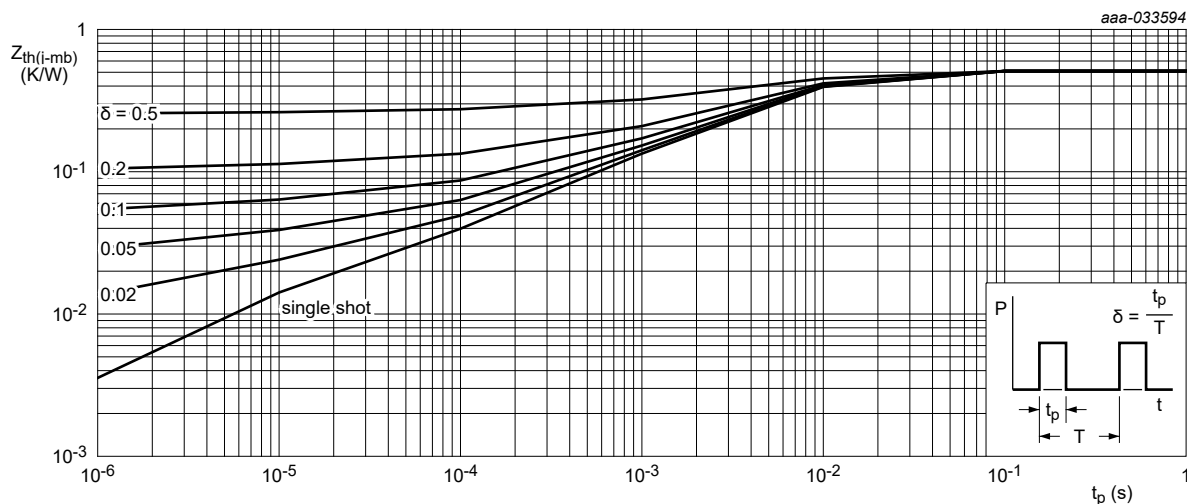
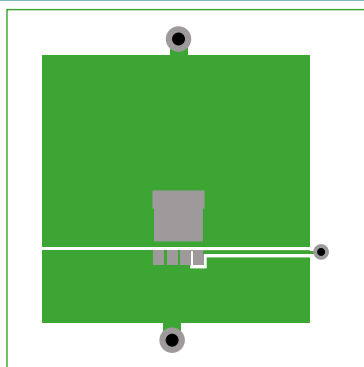
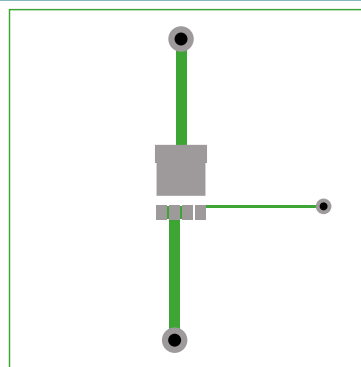


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	80	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = -55 ^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = 25 ^\circ C$; Fig. 11	2	2.6	3.6	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = 175 ^\circ C$	-	1.6	-	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = -55 ^\circ C$	-	3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_J \leq 150 ^\circ C$	-	-6.1	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 80 V$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	-	0.02	1	μA
		$V_{DS} = 80 V$; $V_{GS} = 0 V$; $T_J = 125 ^\circ C$	-	5.5	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA

N-channel 80 V, 4.2 mOhm MOSFET with enhanced SOA in LPAK56E

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12		-	3.2	4.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 100 °C; Fig. 13		-	4.6	6.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 13		-	6.3	9.3	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.52	1.04	2.08	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		37	73	110	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C		-	40	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15		18	31	43	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	16.2	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	14.8	-	nC
Q _{GD}	gate-drain charge			3	11	26	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 40 V; T _J = 25 °C; Fig. 14 ; Fig. 15		-	5.6	-	V
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 0.5 MHz; T _J = 25 °C; Fig. 16		3429	5714	8000	pF
C _{oss}	output capacitance			893	1488	2381	pF
C _{rss}	reverse transfer capacitance			5	55	164	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; R _L = 1.6 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	23	-	ns
t _r	rise time			-	25	-	ns
t _{d(off)}	turn-off delay time			-	32	-	ns
t _f	fall time			-	24	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17		-	0.81	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 40 V; T _J = 25 °C; Fig. 18		-	38	-	ns
Q _r	recovered charge	V _{DS} = 40 V; T _J = 25 °C; Fig. 18		-	35	-	nC

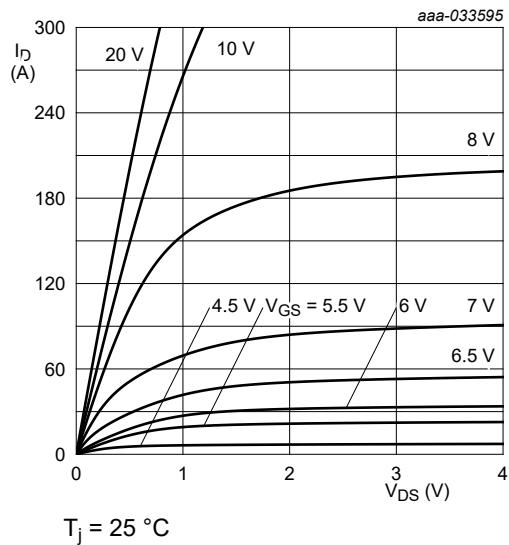


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

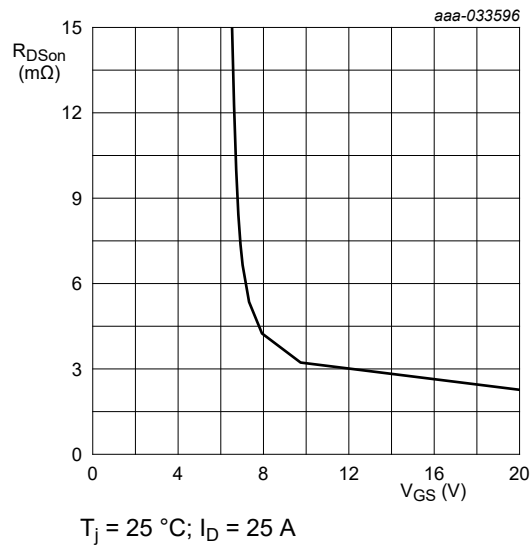


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

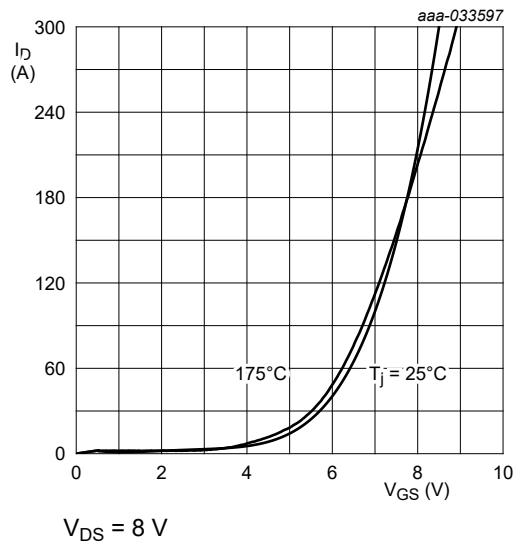


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

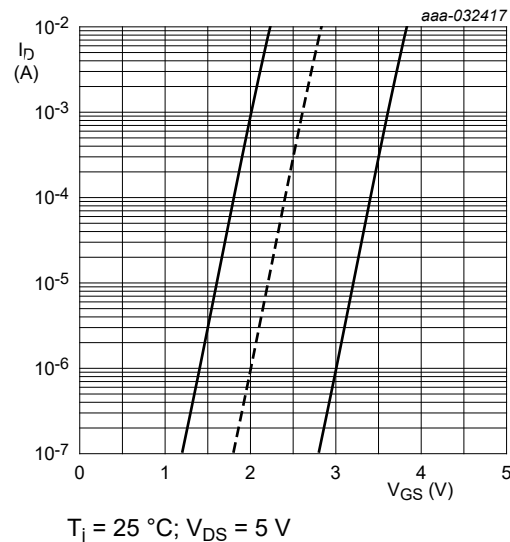


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

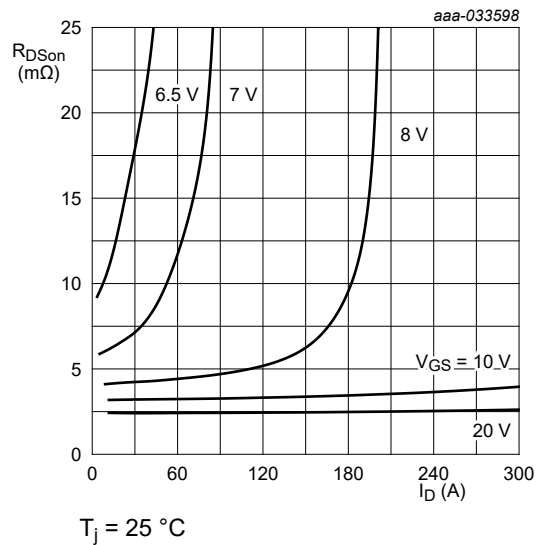


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

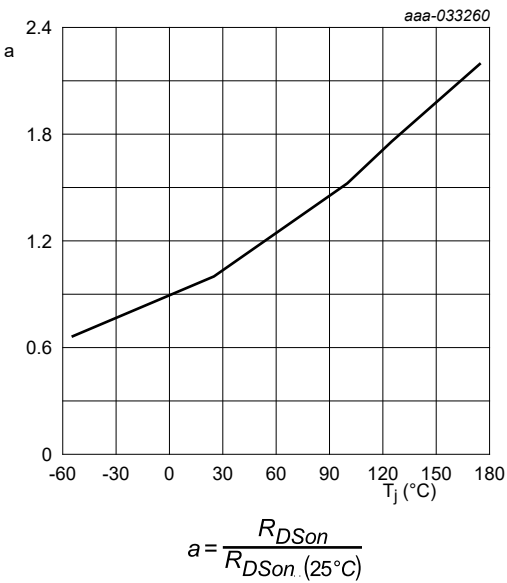


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

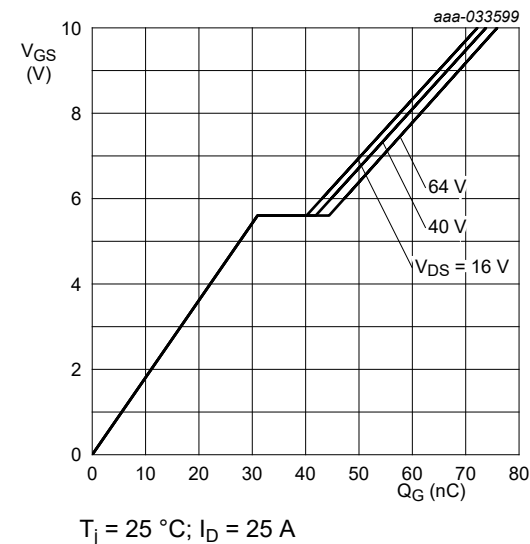


Fig. 14. Gate-source voltage as a function of gate charge; typical values

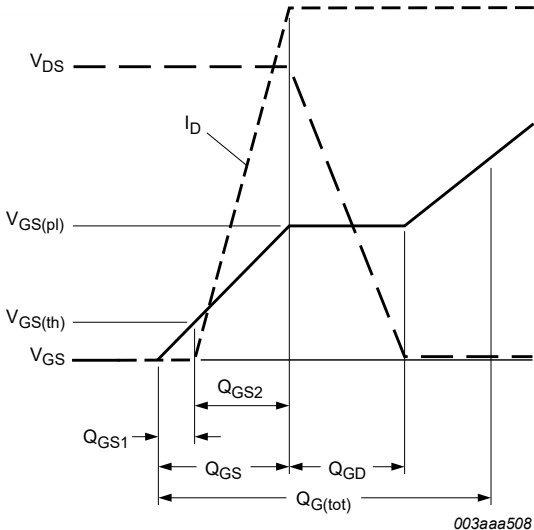


Fig. 15. Gate charge waveform definitions

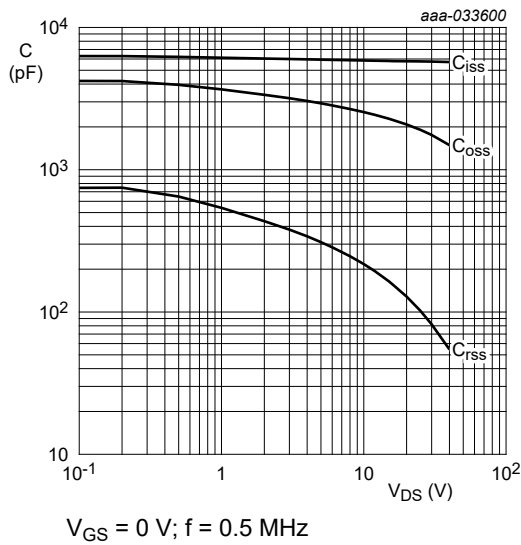


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

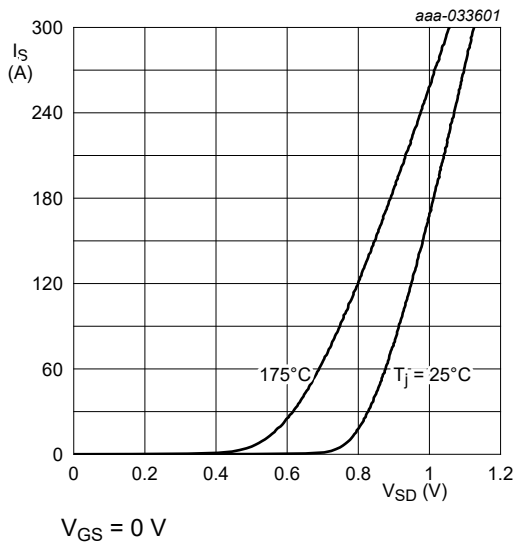


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

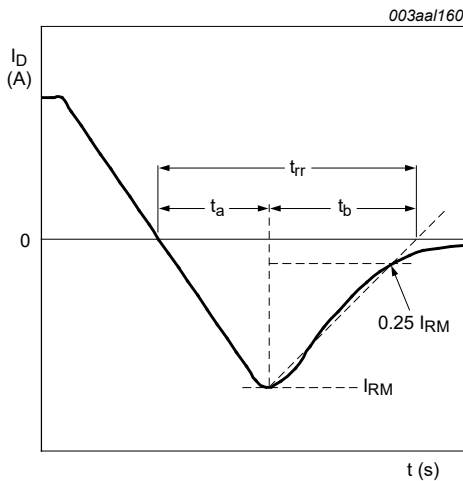


Fig. 18. Reverse recovery timing definition

11. Package outline

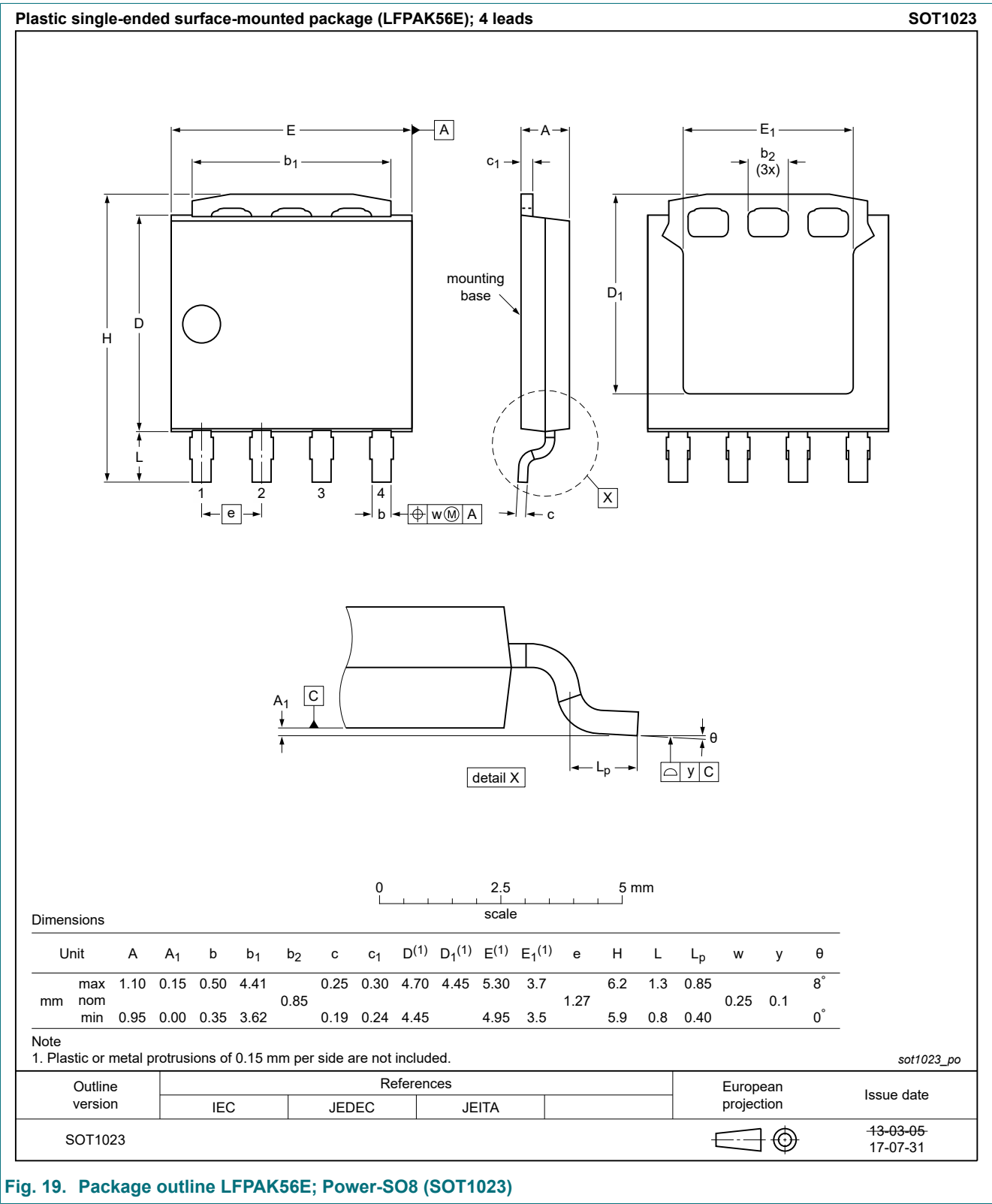


Fig. 19. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

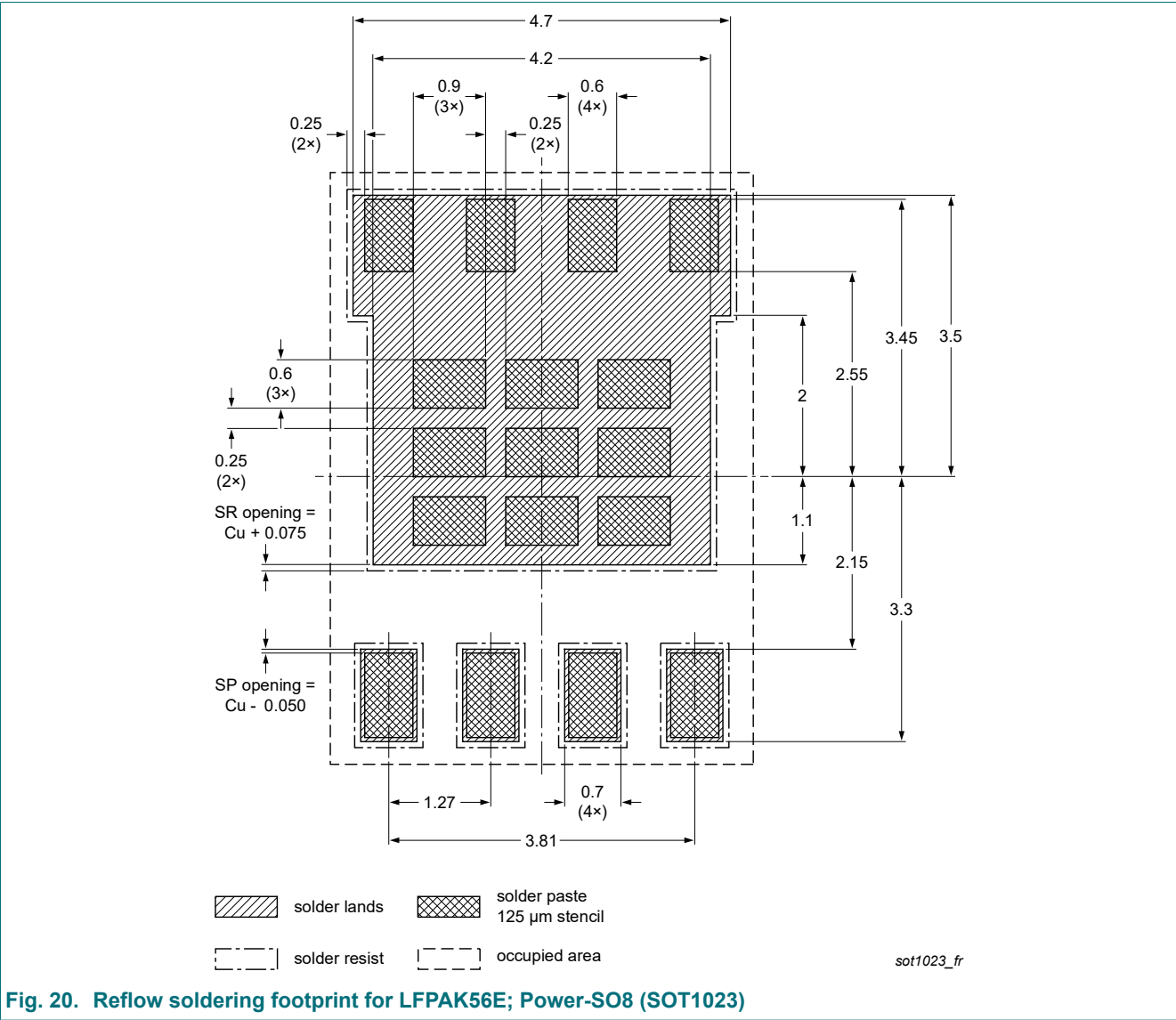


Fig. 20. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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