



PSMN047-100NSE

N-channel 100 V, 53 mOhm standard level ASFET with enhanced SOA in DFN2020. Designed for high power PoE, inrush management, eFuse and relay replacement

12 December 2023

Product data sheet

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90 W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements. These ASFETs combine enhanced SOA in a compact 2 mm x 2 mm footprint making them ideally placed for a variety of applications including PoE, eFuse and relay replacement.

2. Features and benefits

- Enhanced safe operating area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- 2 mm x 2 mm space-saving DFN2020 package, 60% smaller than LPAK33
- Very low I_{DSS} leakage

3. Applications

- High power PoE applications (60 W and higher)
- IEEE802.3at and proprietary PoE solutions
- Fault tolerant load switch - Inrush management and eFuse applications
- Battery management applications
- Relay replacement
- WIFI hotspots
- 5G picocells
- CCTV

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	18.4	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	42	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _j = 25 °C; Fig. 11		-	42	53.4	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _j = 100 °C; Fig. 12		-	66	85	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13 ; Fig. 14		0.5	1.5	3.5	nC
Q _{G(tot)}	total gate charge			4.5	9	13.5	nC

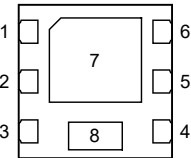
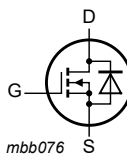
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 10.6\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 20\text{ }\mu\text{s}$; Fig. 4	[1]	-	-	13.8	mJ
Source-drain diode							
Q_r	recovered charge	$I_S = 5\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 17		-	22.3	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view DFN2020M-6 (SOT1220-2)	 mbb076
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN047-100NSE	DFN2020M-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN047-100NSE	ZT

8. Limiting values

Table 5. Limiting values

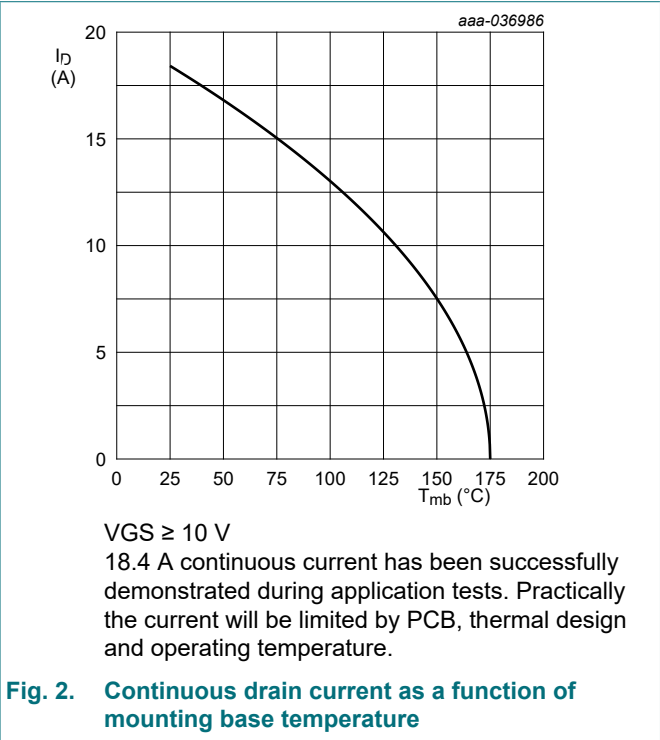
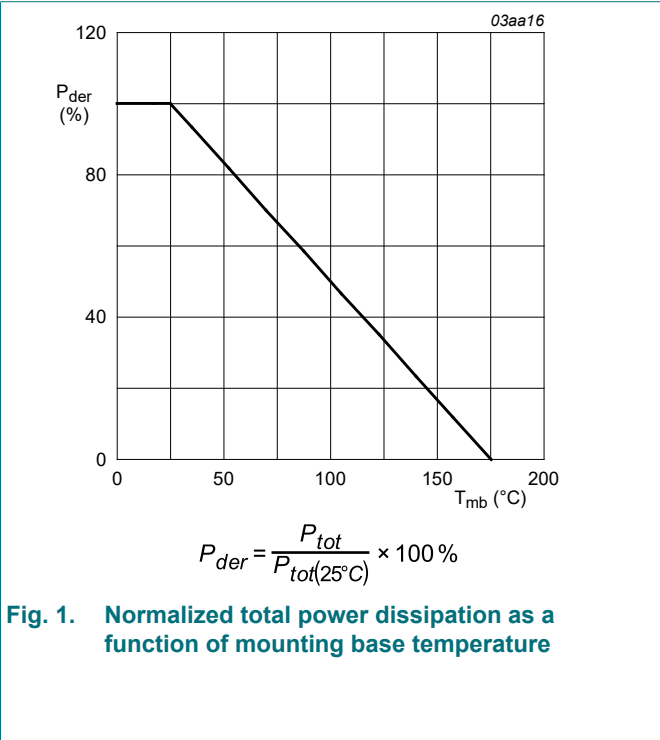
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_J \leq 175\text{ }^\circ\text{C}$		-	100	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_J \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1		-	42	W

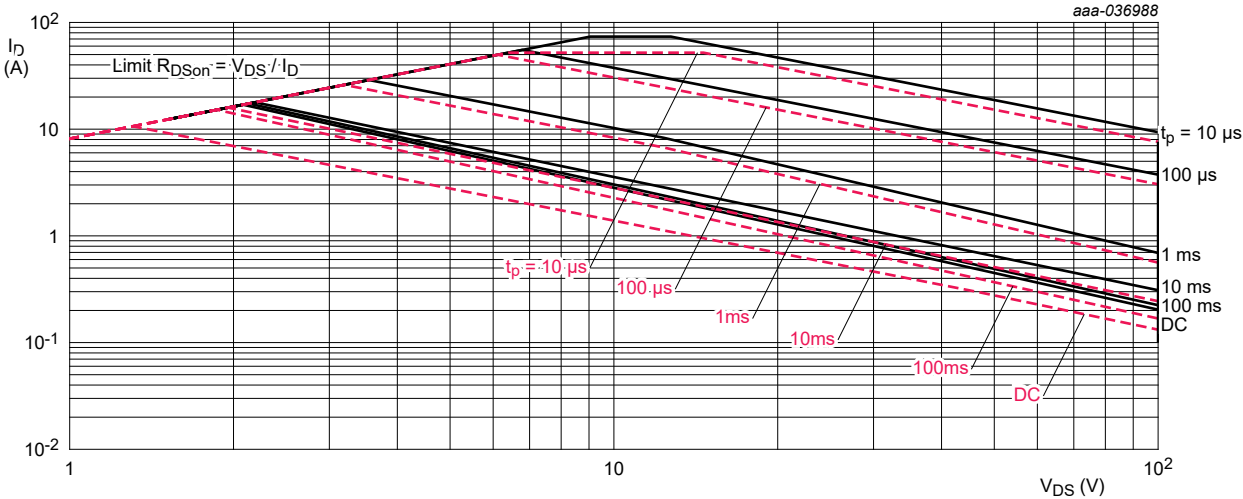
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Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	18.4	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	13	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	74	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	18.4	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	74	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 10.6 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 20 μs; Fig. 4	[1]	-	13.8	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	10.6	A

[1] Protected by 100% test

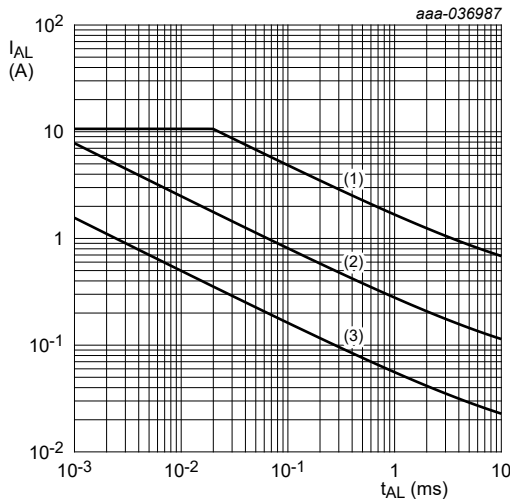


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$T_{mb} = 25 \text{ }^{\circ}\text{C}$ (solid black line); $T_{mb} = 125 \text{ }^{\circ}\text{C}$ (red dashed line); I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j \text{ (init)}} = 25 \text{ }^{\circ}\text{C}$; (2) $T_{j \text{ (init)}} = 150 \text{ }^{\circ}\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3.2	3.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	63	-	K/W
		Fig. 7	-	239	-	K/W

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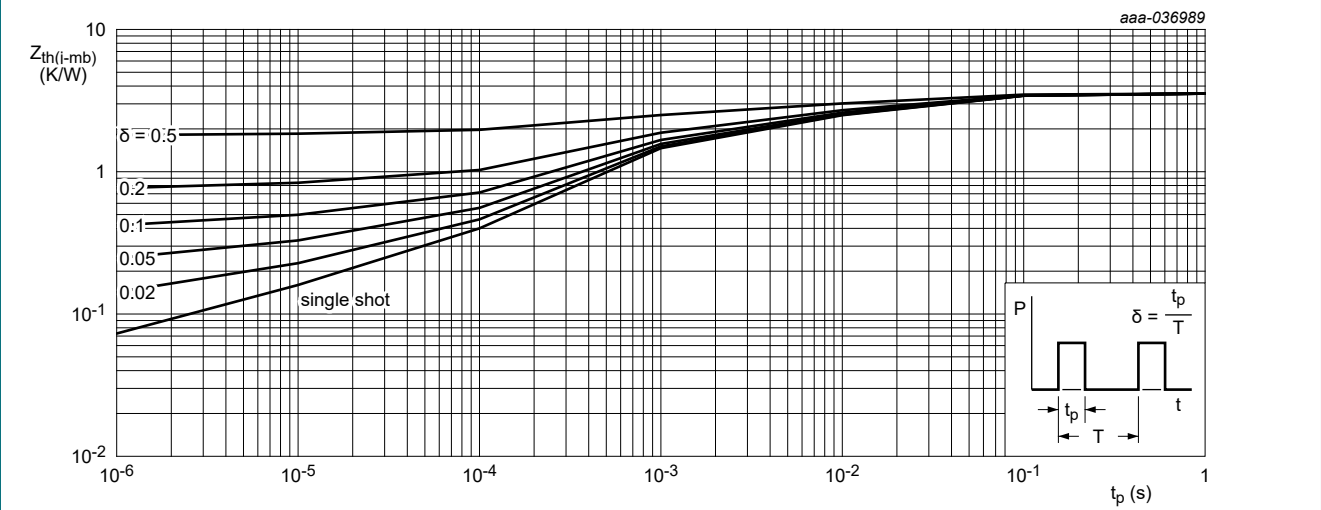


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-037076

Copper square 25.4 mm square; 70 μm thick on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient

aaa-037077

70 μm thick copper on FR4 board

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

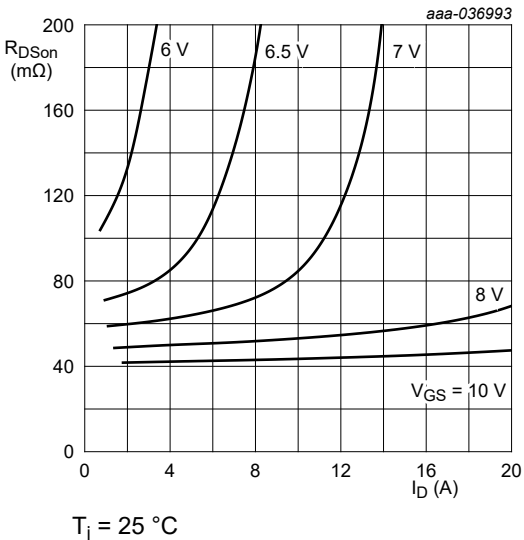
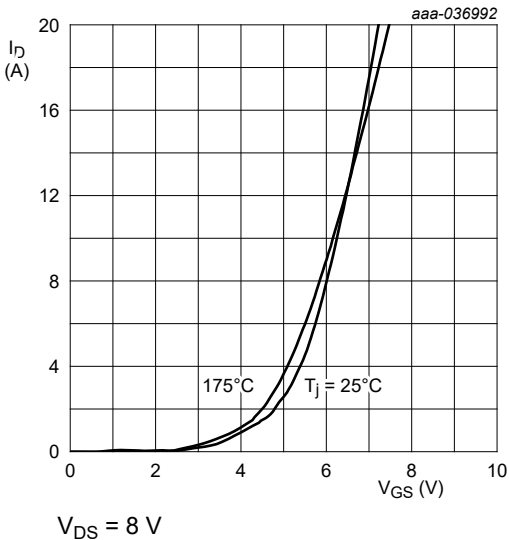
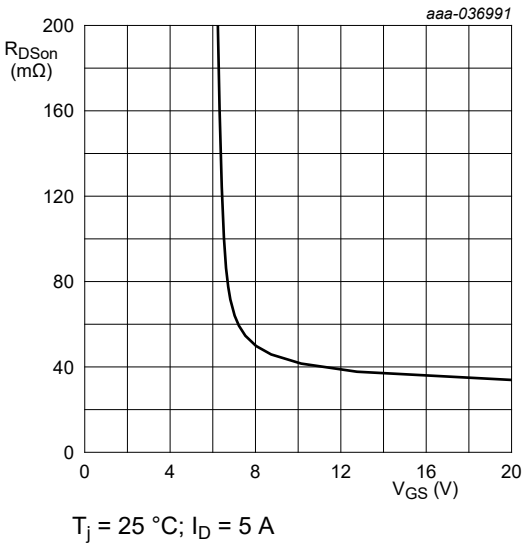
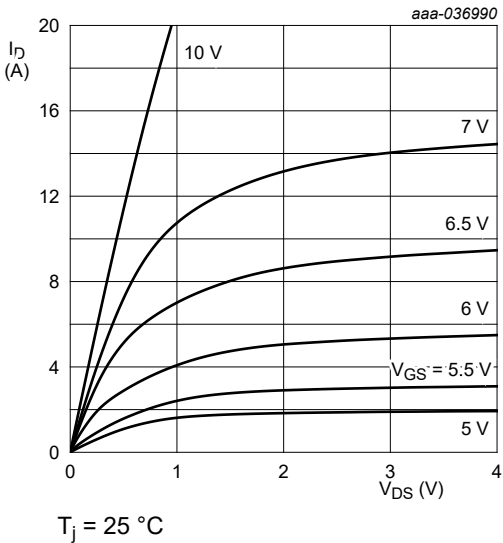
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C	2	2.8	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C	-	1.9	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C	-	3.1	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C	-	-5.2	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.01	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C	-	1.3	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _J = 25 °C; Fig. 11		-	42	53.4	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 100 °C; Fig. 12		-	66	85	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 175 °C; Fig. 12		-	93	121	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.5	1	2	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		4.5	9	13.5	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C		-	8	-	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		2.4	4	5.6	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	2	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	2	-	nC
Q _{GD}	gate-drain charge			0.5	1.5	3.5	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 5 A; V _{DS} = 50 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	5.9	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15		363	605	847	pF
C _{oss}	output capacitance			91.2	152	243	pF
C _{rss}	reverse transfer capacitance			0.6	5.7	15	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 10 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	4.4	-	ns
t _r	rise time			-	3.3	-	ns
t _{d(off)}	turn-off delay time			-	6.2	-	ns
t _f	fall time			-	6.1	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.85	1	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _J = 25 °C; Fig. 17		-	28.5	-	ns
Q _r	recovered charge	V _{DS} = 50 V; T _J = 25 °C; Fig. 17		-	22.3	-	nC

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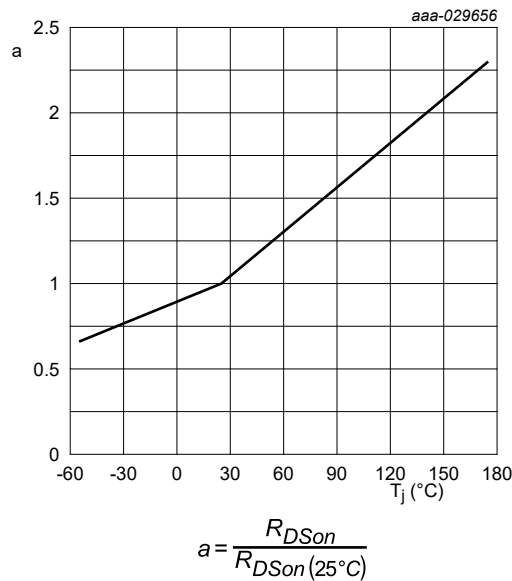


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

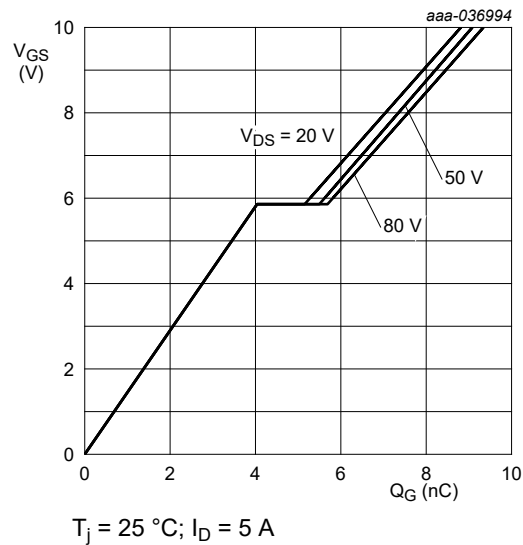


Fig. 13. Gate-source voltage as a function of gate charge; typical values

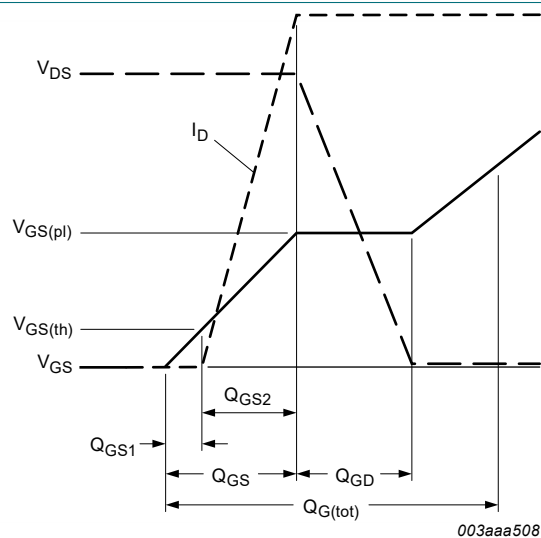


Fig. 14. Gate charge waveform definitions

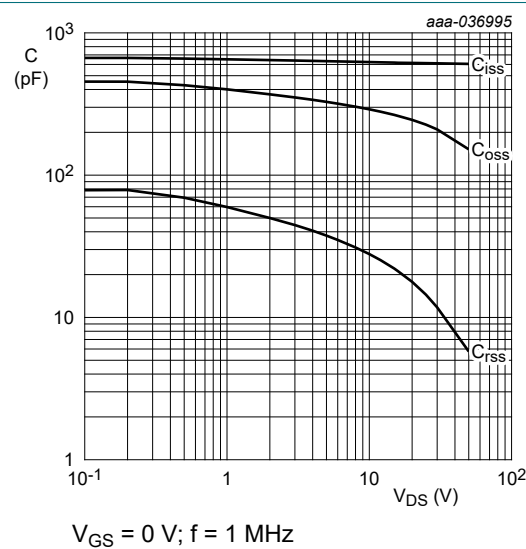


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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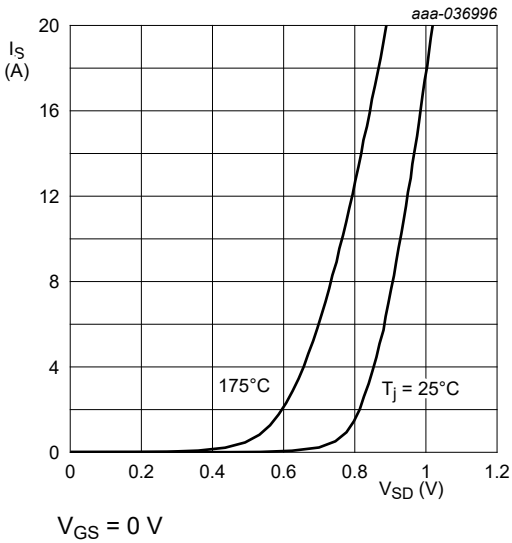


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

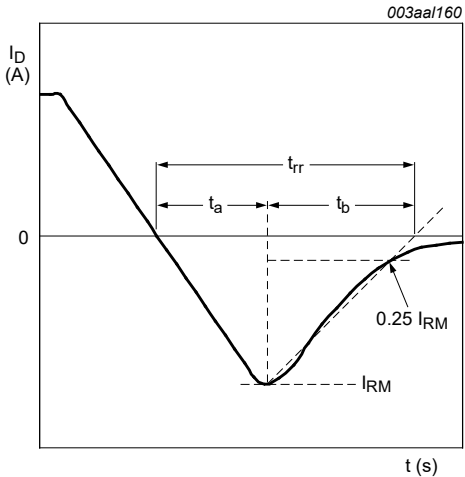


Fig. 17. Reverse recovery timing definition

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11. Package outline

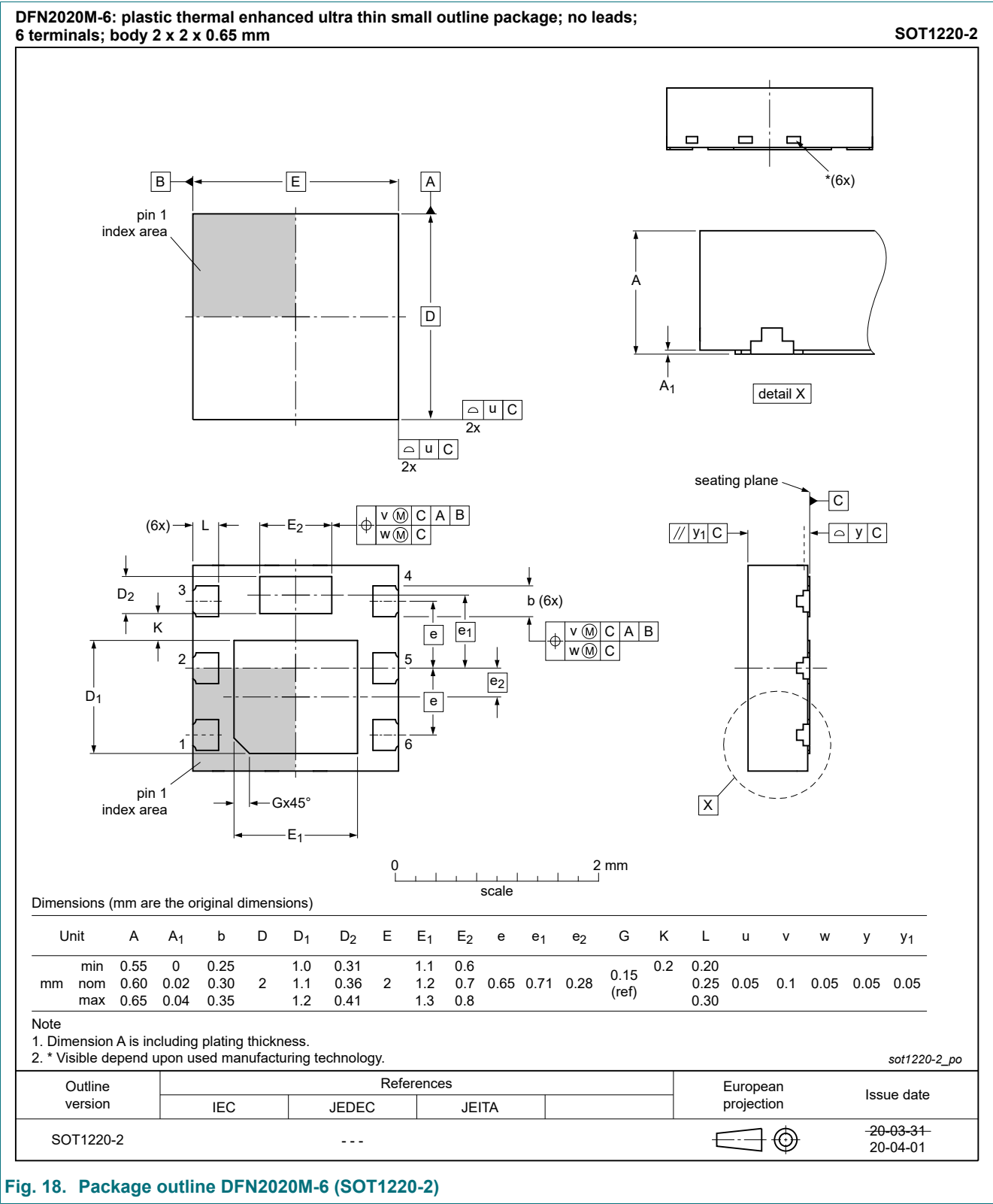


Fig. 18. Package outline DFN2020M-6 (SOT1220-2)

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12. Soldering

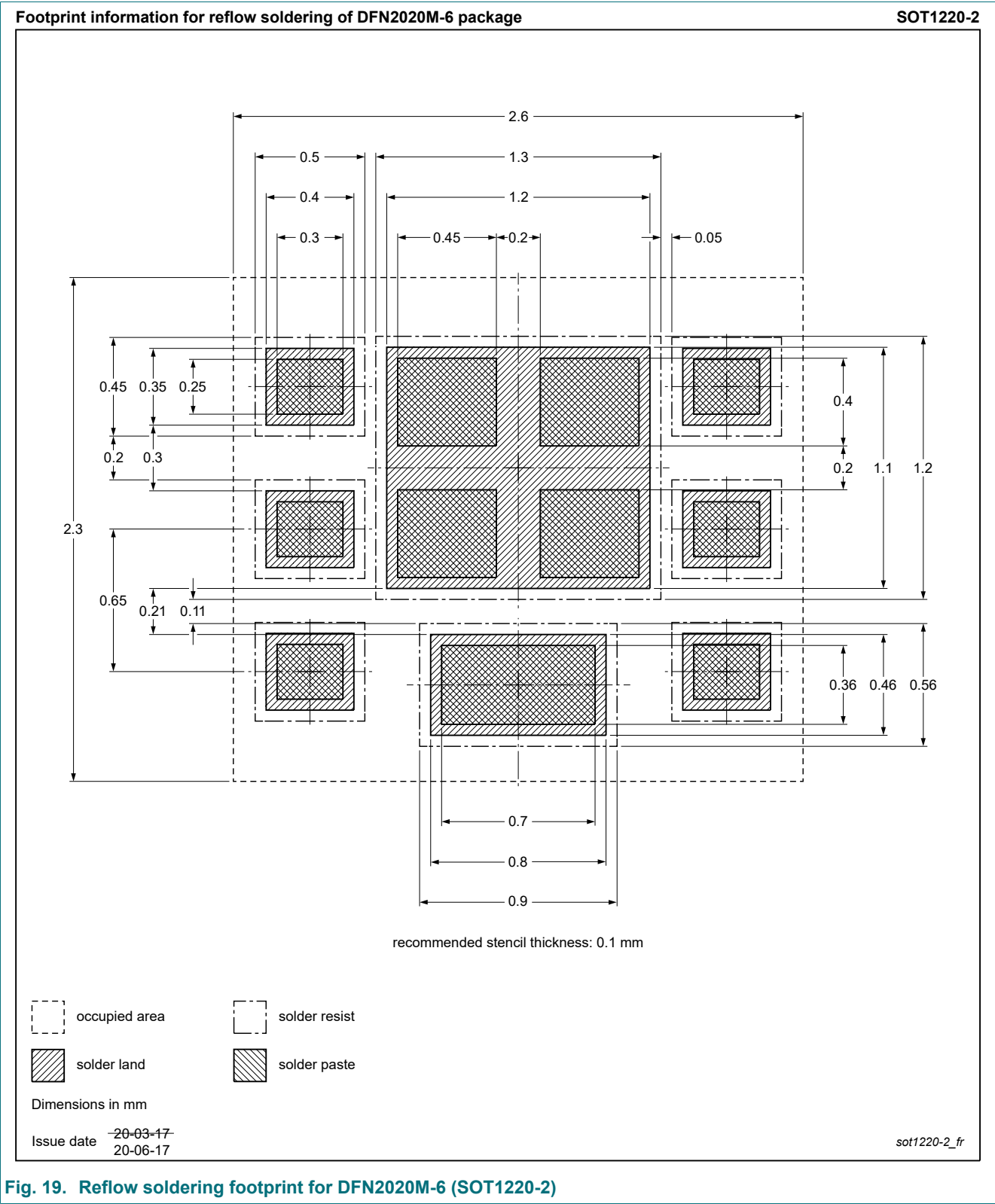


Fig. 19. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 2

9. Thermal characteristics..... 4

10. Characteristics..... 5

11. Package outline..... 10

12. Soldering..... 11

13. Legal information.....12

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