

NP75N04YLG

40 V – 75 A – N-channel Power MOS FET

Application: Automotive

R07DS1247EJ0100

Rev.1.00

Mar 02, 2015

Description

The NP75N04YLG is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
 $R_{DS(on)} = 4.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 38 \text{ A)}$
 $R_{DS(on)} = 8.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 38 \text{ A)}$
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP75N04YLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP75N04YLG-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 75	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 225	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	138	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *3	I_{AR}	35	A
Repetitive Avalanche Energy *3	E_{AR}	123	mJ

Notes: *1 $T_C = 25^\circ\text{C}$, $P_W \leq 10 \text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$

*2 Mounted on glass epoxy substrate of 40 mm $\times$ 40 mm $\times$ 1.6 mm with 4% Copper area (35 μm)

*3 $T_{ch}(\text{peak}) \leq 150^\circ\text{C}$, $R_G = 25 \text{ }\Omega$

Thermal Resistance

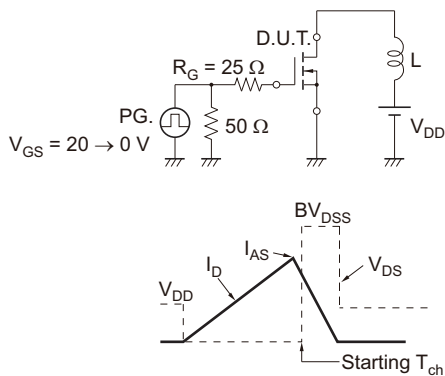
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.09	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	150	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

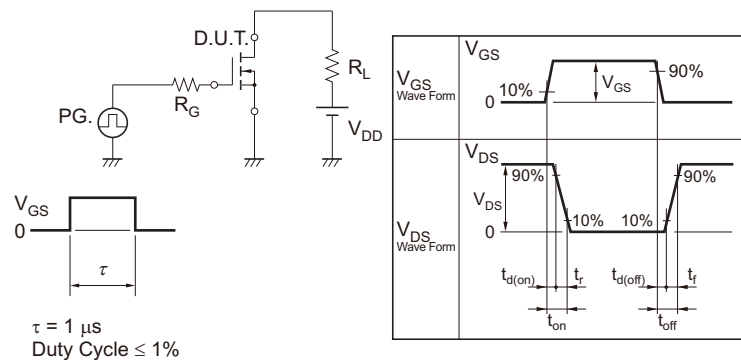
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.0	2.5	V	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$
Forward Transfer Admittance *1	$ y_{fs} $	40	46	—	S	$V_{DS} = 5\text{ V}$, $I_D = 38\text{ A}$
Drain to Source On-state Resistance *1	$R_{DS(on)}$	—	3.8	4.8	$\text{m}\Omega$	$V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$
		—	4.5	8.3	$\text{m}\Omega$	$V_{GS} = 4.5\text{ V}$, $I_D = 38\text{ A}$
Input Capacitance	C_{iss}	—	4300	6450	pF	$V_{DS} = 25\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}	—	400	600	pF	
Reverse Transfer Capacitance	C_{rss}	—	250	450	pF	
Turn-on Delay Time	$t_{d(on)}$	—	22	44	ns	$V_{DD} = 20\text{ V}$, $I_D = 38\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 0\text{ }\Omega$
Rise Time	t_r	—	17	41	ns	
Turn-off Delay Time	$t_{d(off)}$	—	40	140	ns	
Fall Time	t_f	—	11	27	ns	
Total Gate Charge	Q_G	—	77	116	nC	$V_{DD} = 32\text{ V}$ $V_{GS} = 10\text{ V}$ $I_D = 75\text{ A}$
Gate to Source Charge	Q_{GS}	—	20	—	nC	
Gate to Drain Charge	Q_{GD}	—	25	—	nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	$I_F = 75\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}	—	34	—	ns	$I_F = 75\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Charge	Q_{rr}	—	34	—	nC	

Note: *1 Pulsed test

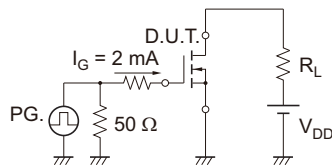
TEST CIRCUIT 1 AVALANCHE CAPABILITY



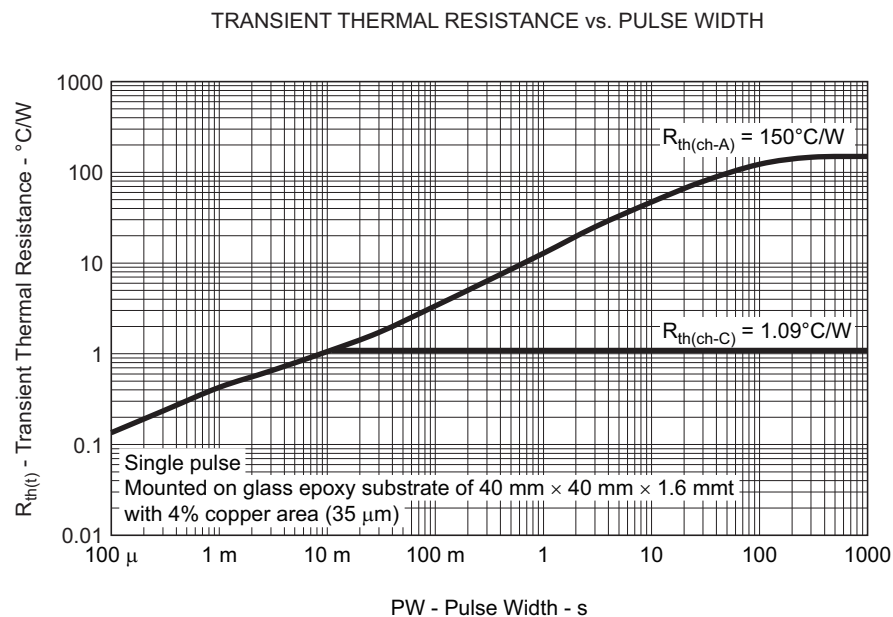
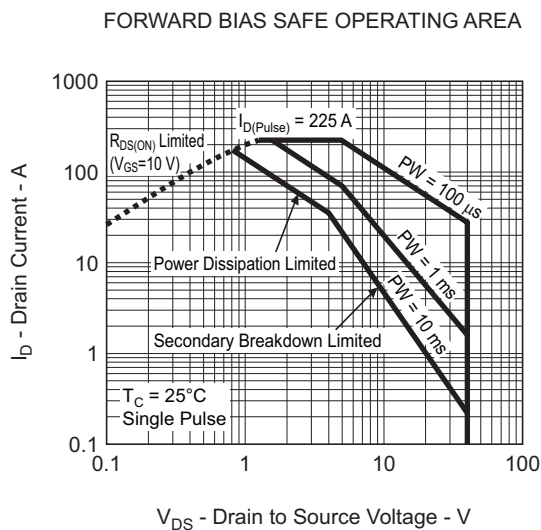
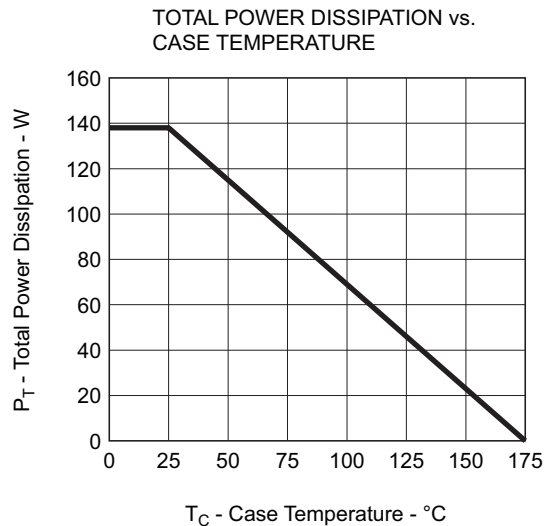
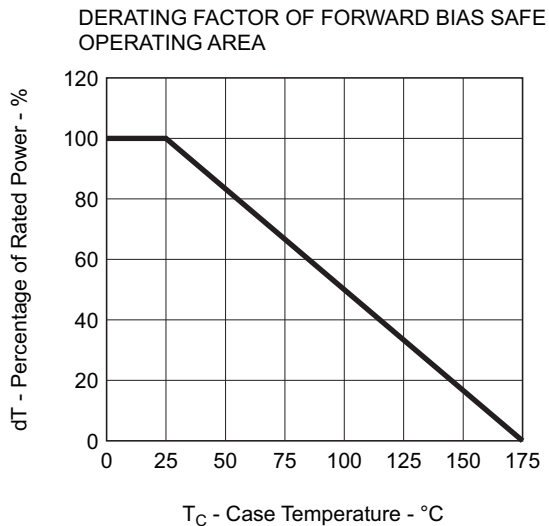
TEST CIRCUIT 2 SWITCHING TIME

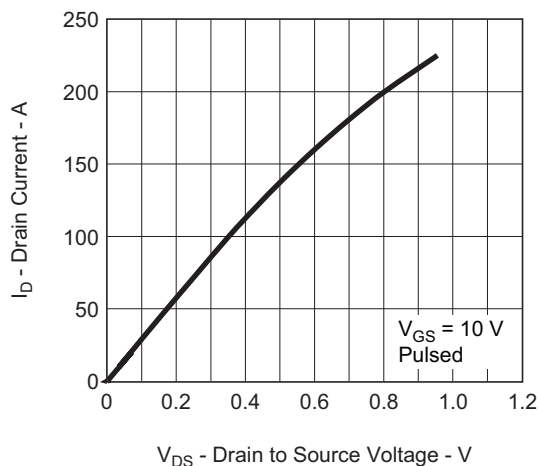


TEST CIRCUIT 3 GATE CHARGE

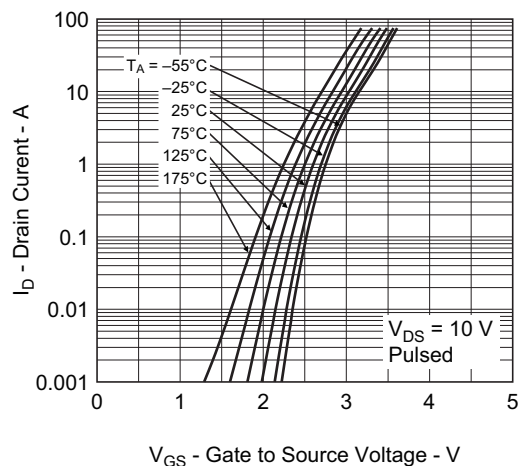
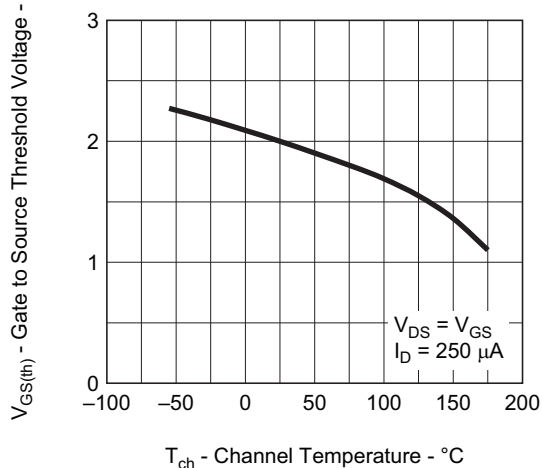
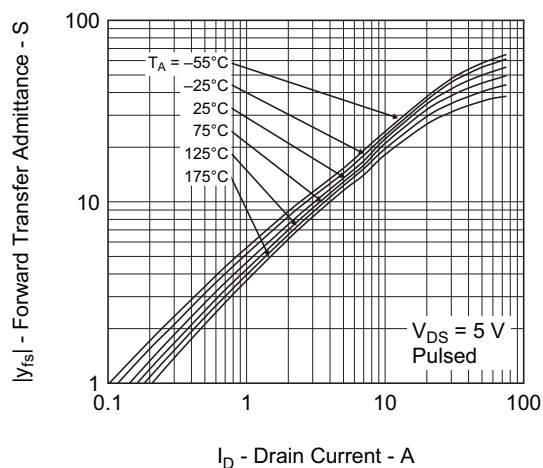
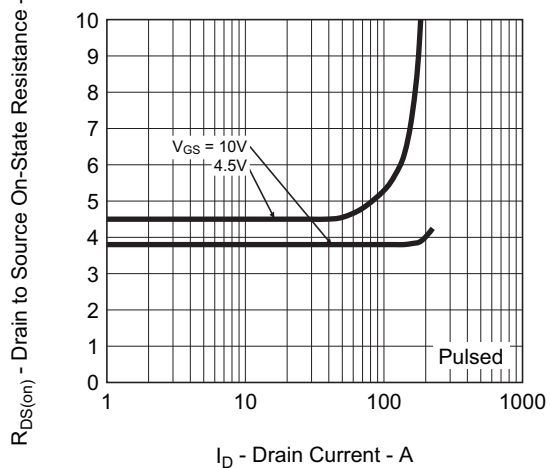
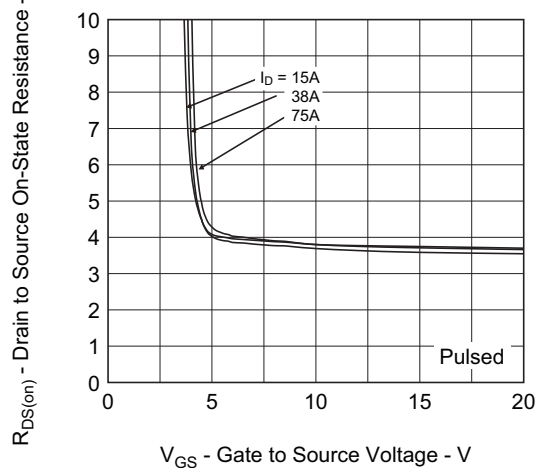


Typical Characteristics ($T_A = 25^\circ\text{C}$)

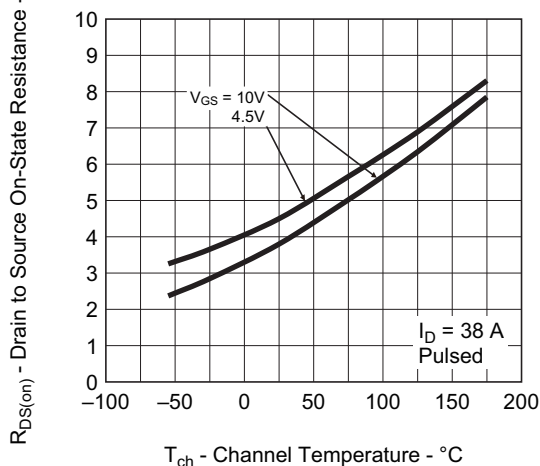


DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

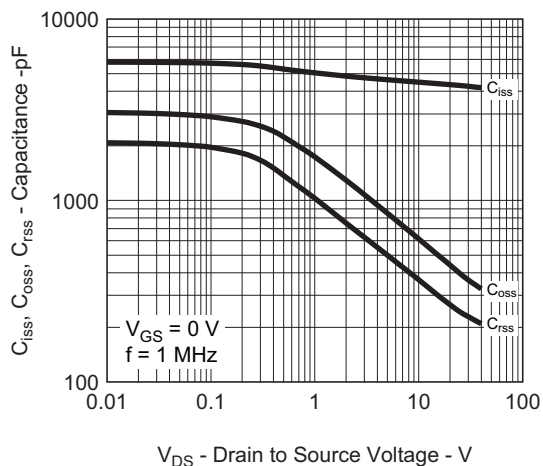
FORWARD TRANSFER CHARACTERISTICS

GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

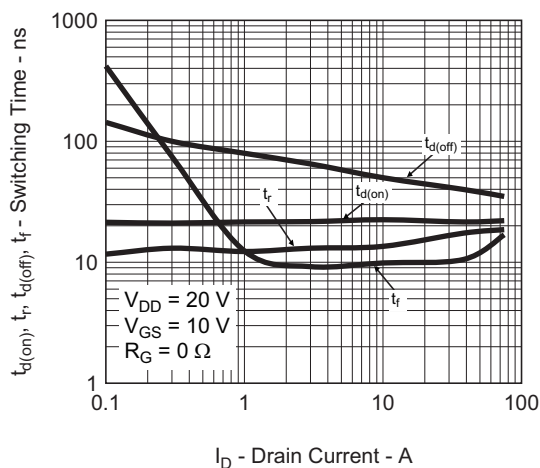
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



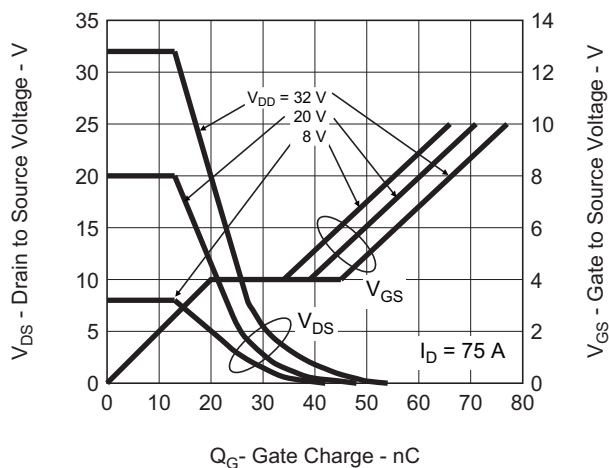
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



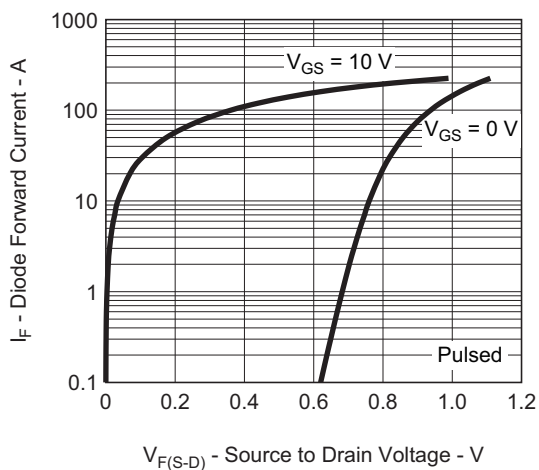
SWITCHING CHARACTERISTICS



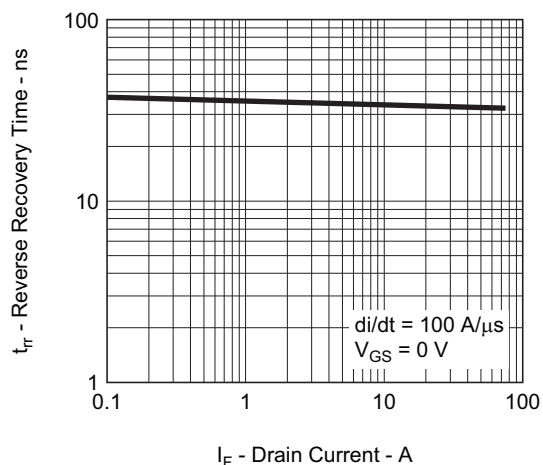
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



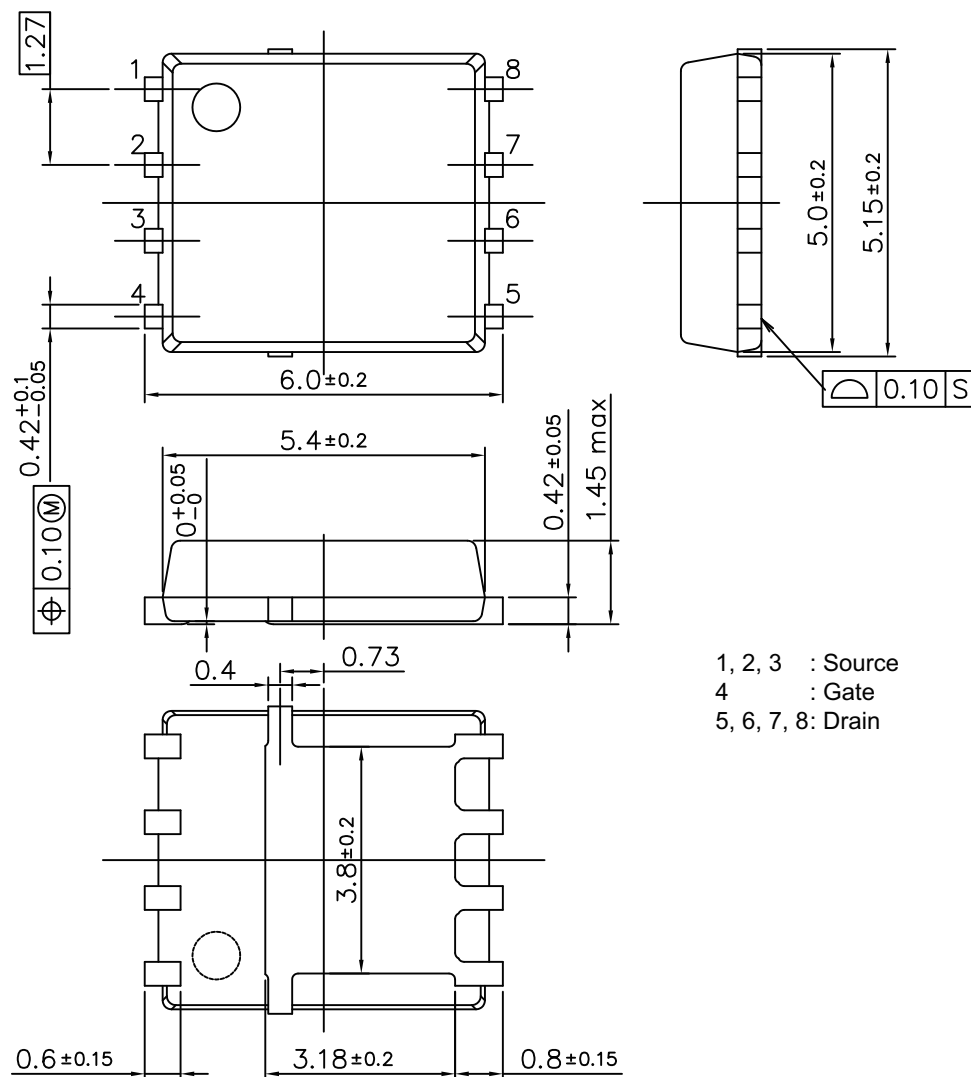
REVERSE RECOVERY TIME vs. DRAIN CURRENT



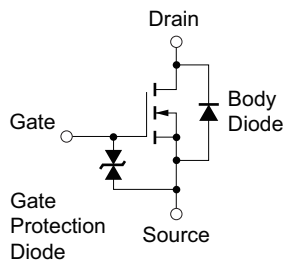
Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)

Renesas Code: PLSN0008KA-A



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP75N04YLG Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 02, 2015	—	First Edition Issued

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