

# NP45N06VUK, NP45N06PUK

60 V – 45 A – N-channel Power MOS FET

Application: Automotive

R07DS0953EJ0200

Rev.2.00

May 24, 2018

## Description

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

## Features

- Super low on-state resistance  
 $R_{DS(on)} = 9.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 23 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 1690 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$
- Designed for automotive application and AEC-Q101 qualified

## Ordering Information

| Part No.            | Lead Plating  | Packing          |                  | Package          |
|---------------------|---------------|------------------|------------------|------------------|
| NP45N06VUK-E1-AY *1 | Pure Sn (Tin) | Tape 2500 p/reel | Taping (E1 type) | TO-252 (MP-3ZP)  |
| NP45N06VUK-E2-AY *1 |               |                  | Taping (E2 type) |                  |
| NP45N06PUK-E1-AY *1 |               | Tape 800 p/reel  | Taping (E1 type) | TO-263 (MP-25ZP) |
| NP45N06PUK-E2-AY *1 |               |                  | Taping (E2 type) |                  |

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

| Item                                                    |            | Symbol         | Ratings              | Unit             |
|---------------------------------------------------------|------------|----------------|----------------------|------------------|
| Drain to Source Voltage ( $V_{GS} = 0\text{ V}$ )       |            | $V_{DSS}$      | 60                   | V                |
| Gate to Source Voltage ( $V_{DS} = 0\text{ V}$ )        |            | $V_{GSS}$      | $\pm 20$             | V                |
| Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )         |            | $I_{D(DC)}$    | $\pm 45$             | A                |
| Drain Current (pulse) *1, 3                             |            | $I_{D(pulse)}$ | $\pm 135$            | A                |
| Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )    |            | $P_{T1}$       | 75                   | W                |
| Total Power Dissipation<br>( $T_A = 25^\circ\text{C}$ ) | NP45N06VUK | $P_{T2}$       | 1.2                  | W                |
|                                                         | NP45N06PUK |                | 1.8                  | W                |
| Channel Temperature                                     |            | $T_{ch}$       | 175                  | $^\circ\text{C}$ |
| Storage Temperature                                     |            | $T_{stg}$      | $-55\text{ to }+175$ | $^\circ\text{C}$ |
| Repetitive Avalanche Current *2, 3                      |            | $I_{AR}$       | 19                   | A                |
| Repetitive Avalanche Energy *2, 3                       |            | $E_{AR}$       | 36                   | mJ               |

## Thermal Resistance

|                                       |                   |                                    |
|---------------------------------------|-------------------|------------------------------------|
| Channel to Case Thermal Resistance    | $R_{th(ch-C)} *3$ | 2.00 $^\circ\text{C/W}$            |
| Channel to Ambient Thermal Resistance | $R_{th(ch-A)} *3$ | NP45N06VUK 125 $^\circ\text{C/W}$  |
|                                       |                   | NP45N06PUK 83.3 $^\circ\text{C/W}$ |

Notes: \*1  $T_C = 25^\circ\text{C}$ ,  $P_W \leq 10 \text{ }\mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2  $R_G = 25 \text{ }\Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

\*3 Not subject of production test. Verified by design/characterization.

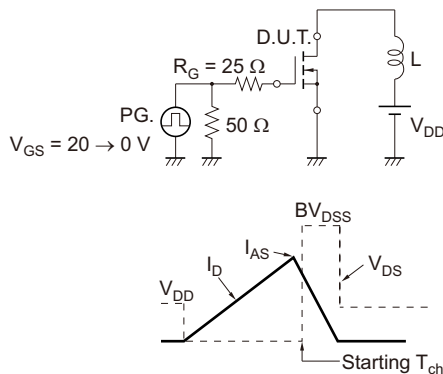
Electrical Characteristics ( $T_A = 25^\circ\text{C}$ )

| Item                                   | Symbol       | MIN. | TYP. | MAX.      | Unit          | Test Conditions                                                                                   |
|----------------------------------------|--------------|------|------|-----------|---------------|---------------------------------------------------------------------------------------------------|
| Zero Gate Voltage Drain Current        | $I_{DSS}$    | —    | —    | 1         | $\mu\text{A}$ | $V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$                                                    |
| Gate Leakage Current                   | $I_{GSS}$    | —    | —    | $\pm 100$ | nA            | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$                                                |
| Gate to Source Threshold Voltage       | $V_{GS(th)}$ | 2.0  | 3.0  | 4.0       | V             | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                                |
| Forward Transfer Admittance *1         | $ y_{fs} $   | 17   | 34   | —         | S             | $V_{DS} = 5\text{ V}$ , $I_D = 23\text{ A}$                                                       |
| Drain to Source On-state Resistance *1 | $R_{DS(on)}$ | —    | 7.8  | 9.6       | m $\Omega$    | $V_{GS} = 10\text{ V}$ , $I_D = 23\text{ A}$                                                      |
| Input Capacitance *2                   | $C_{iss}$    | —    | 1690 | 2540      | pF            | $V_{DS} = 25\text{ V}$<br>$V_{GS} = 0\text{ V}$<br>$f = 1\text{ MHz}$                             |
| Output Capacitance *2                  | $C_{oss}$    | —    | 155  | 240       | pF            |                                                                                                   |
| Reverse Transfer Capacitance *2        | $C_{rss}$    | —    | 70   | 130       | pF            |                                                                                                   |
| Turn-on Delay Time *2                  | $t_{d(on)}$  | —    | 15   | 40        | ns            | $V_{DD} = 30\text{ V}$ , $I_D = 23\text{ A}$<br>$V_{GS} = 10\text{ V}$<br>$R_G = 0\text{ }\Omega$ |
| Rise Time *2                           | $t_r$        | —    | 5    | 20        | ns            |                                                                                                   |
| Turn-off Delay Time *2                 | $t_{d(off)}$ | —    | 37   | 80        | ns            |                                                                                                   |
| Fall Time *2                           | $t_f$        | —    | 3    | 10        | ns            |                                                                                                   |
| Total Gate Charge *2                   | $Q_G$        | —    | 30   | 45        | nC            | $V_{DD} = 48\text{ V}$<br>$V_{GS} = 10\text{ V}$<br>$I_D = 45\text{ A}$                           |
| Gate to Source Charge                  | $Q_{GS}$     | —    | 8    | —         | nC            |                                                                                                   |
| Gate to Drain Charge                   | $Q_{GD}$     | —    | 8    | —         | nC            |                                                                                                   |
| Body Diode Forward Voltage *1          | $V_{F(S-D)}$ | —    | 0.9  | 1.5       | V             | $I_F = 45\text{ A}$ , $V_{GS} = 0\text{ V}$                                                       |
| Reverse Recovery Time                  | $t_{rr}$     | —    | 32   | —         | ns            | $I_F = 45\text{ A}$ , $V_{GS} = 0\text{ V}$                                                       |
| Reverse Recovery Charge                | $Q_{rr}$     | —    | 35   | —         | nC            | $di/dt = 100\text{ A}/\mu\text{s}$                                                                |

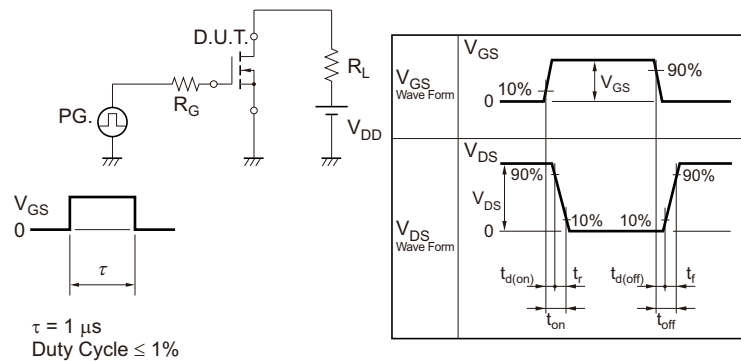
Note: \*1 Pulsed test

Note: \*2 Not subject of production test. Verified by design/characterization.

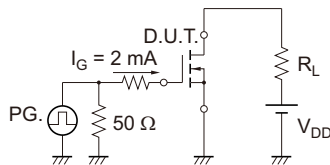
## TEST CIRCUIT 1 AVALANCHE CAPABILITY



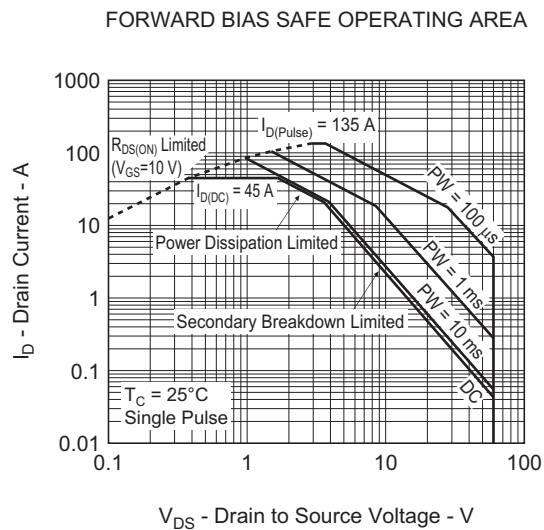
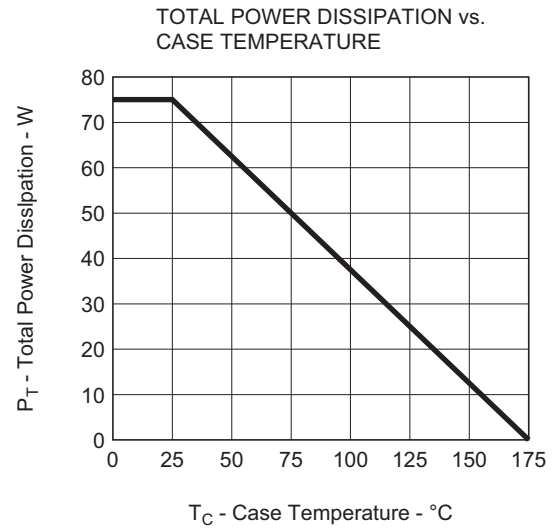
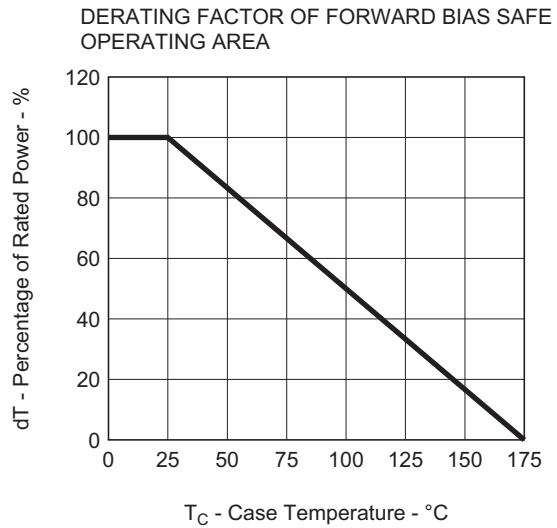
## TEST CIRCUIT 2 SWITCHING TIME



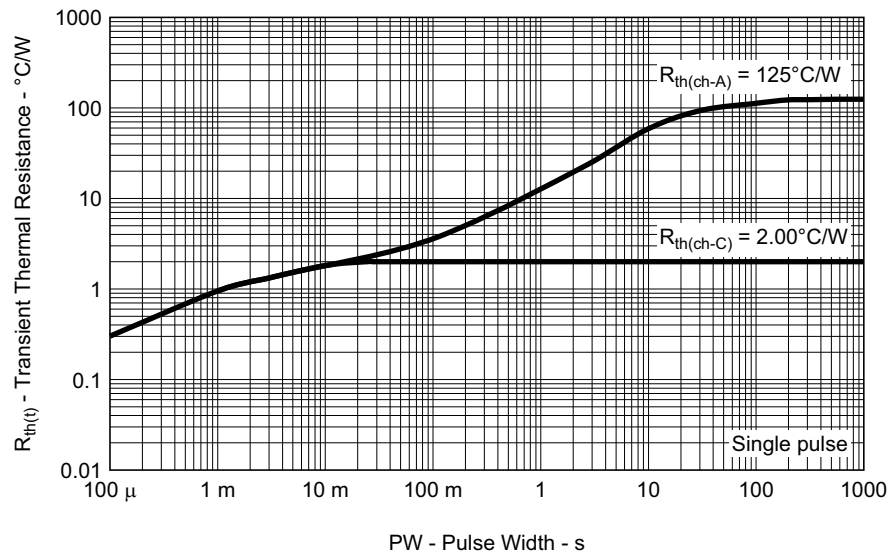
## TEST CIRCUIT 3 GATE CHARGE



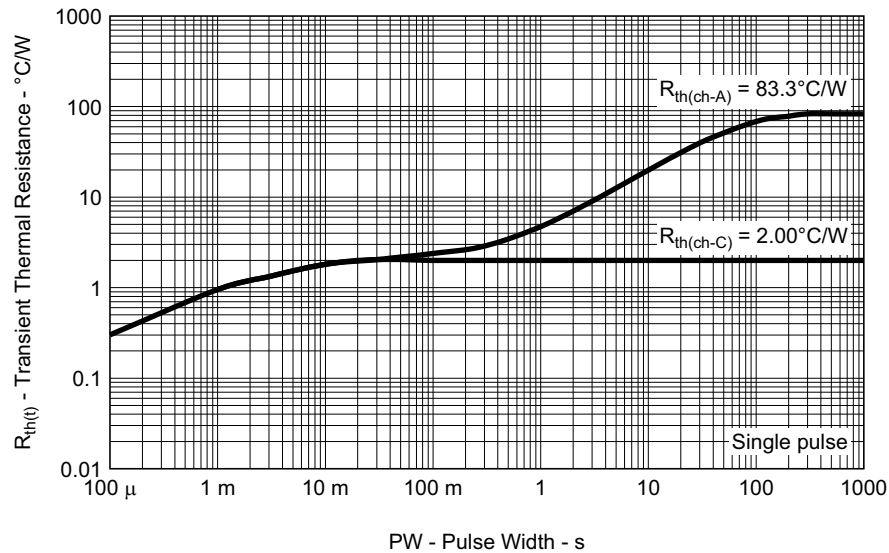
## Typical Characteristics ( $T_A = 25^\circ\text{C}$ )



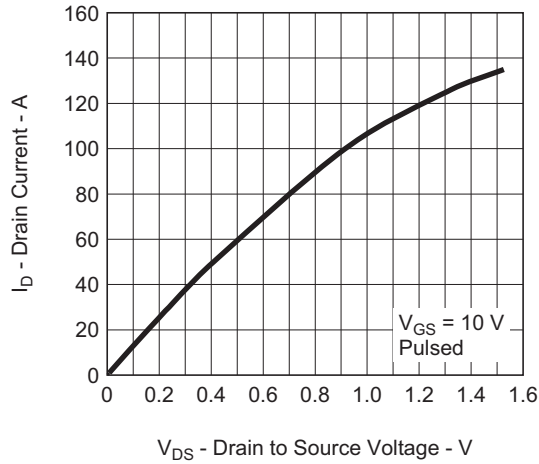
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP45N06VUK)



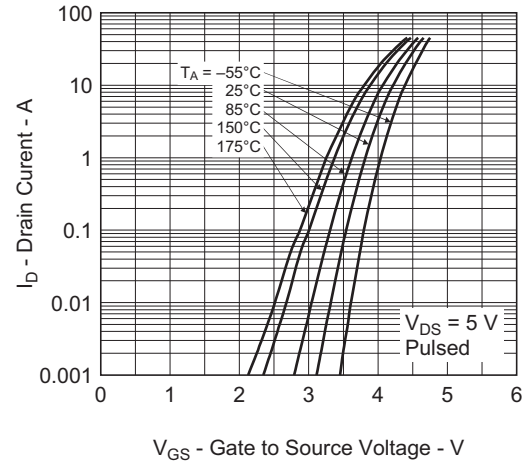
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP45N06PUK)



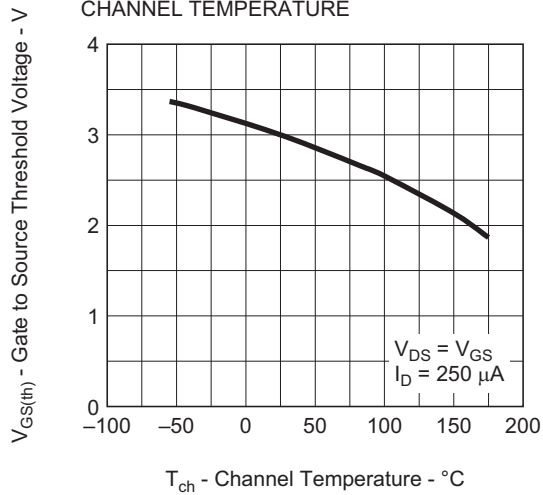
DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE



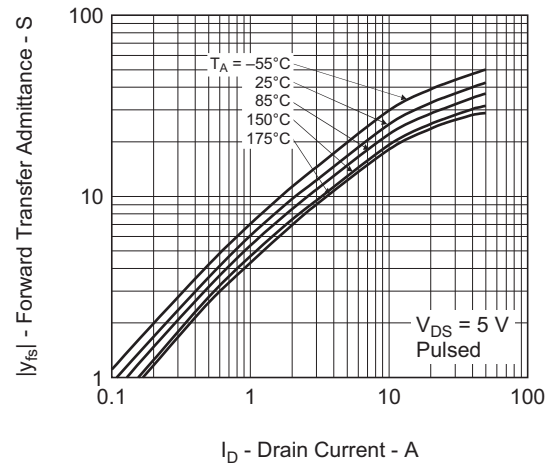
FORWARD TRANSFER CHARACTERISTICS



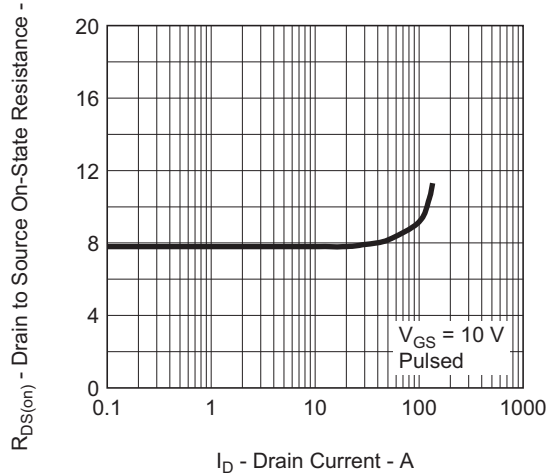
GATE TO SOURCE THRESHOLD VOLTAGE vs.  
CHANNEL TEMPERATURE



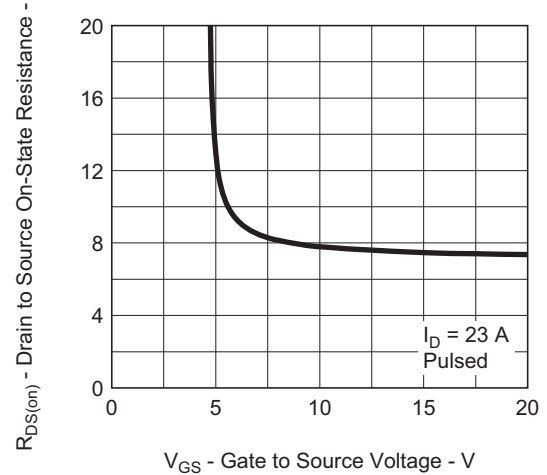
FORWARD TRANSFER ADMITTANCE vs.  
DRAIN CURRENT

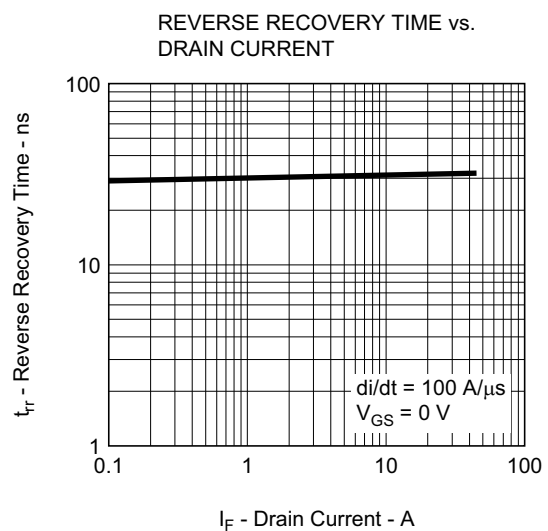
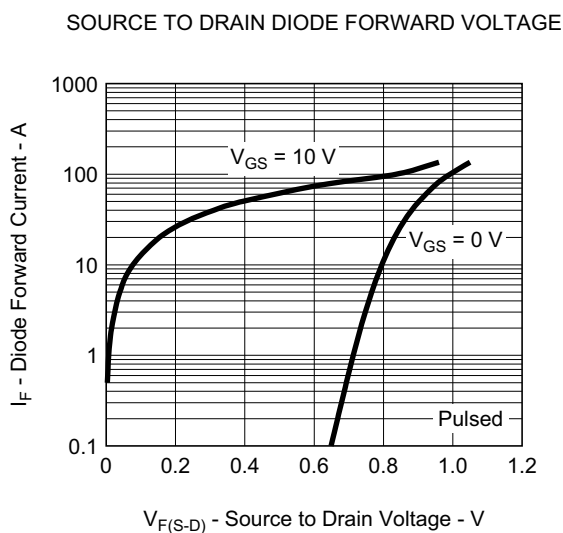
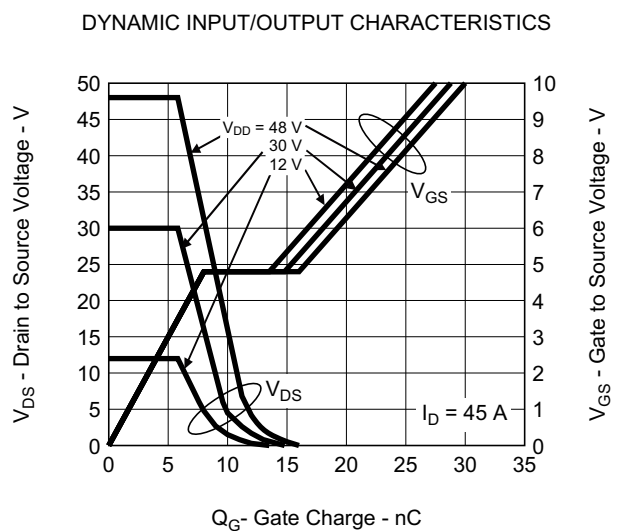
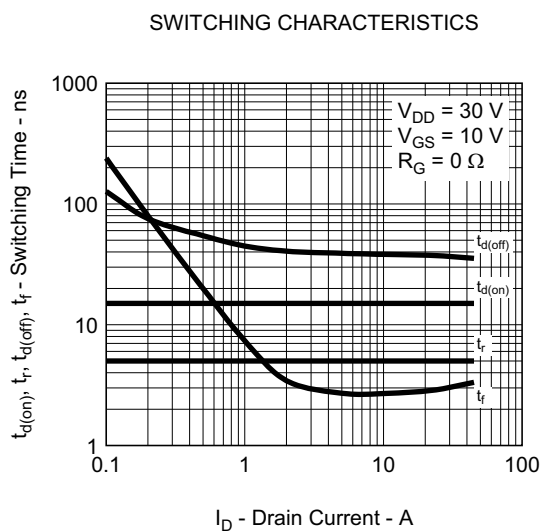
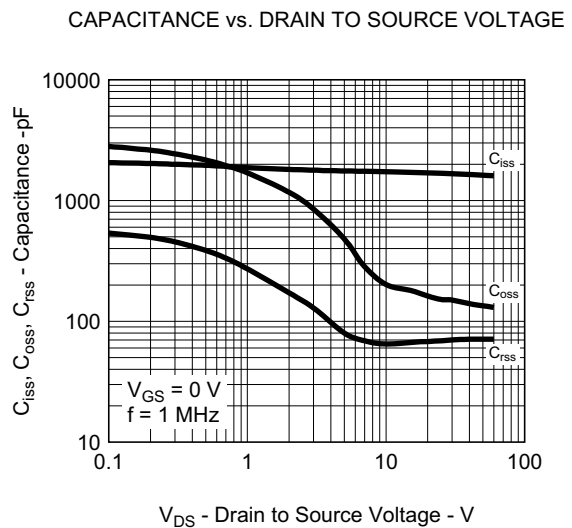
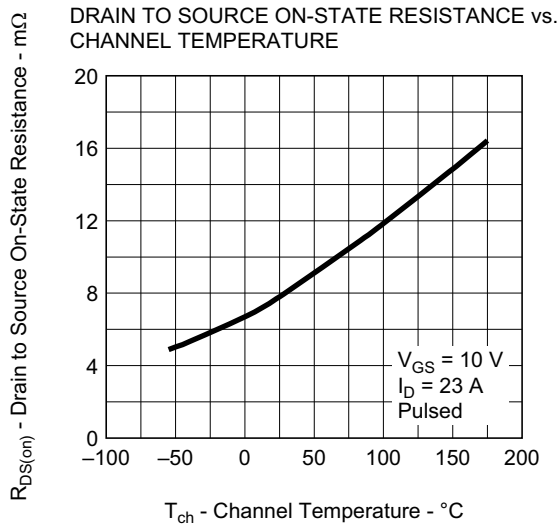


DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
DRAIN CURRENT



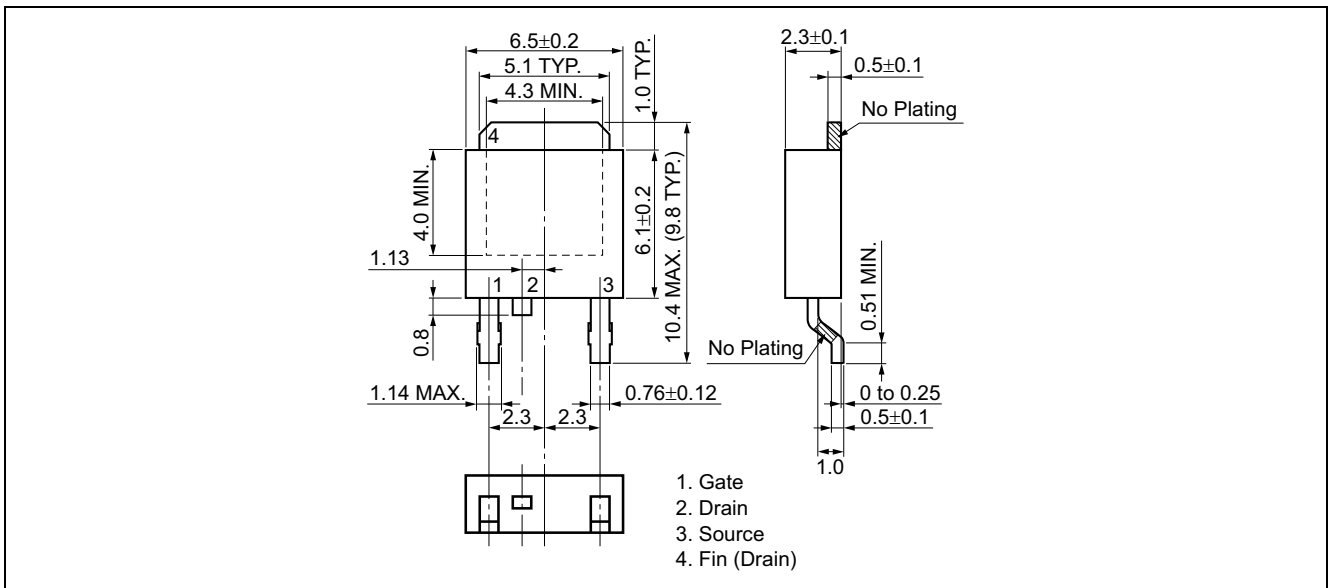
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
GATE TO SOURCE VOLTAGE



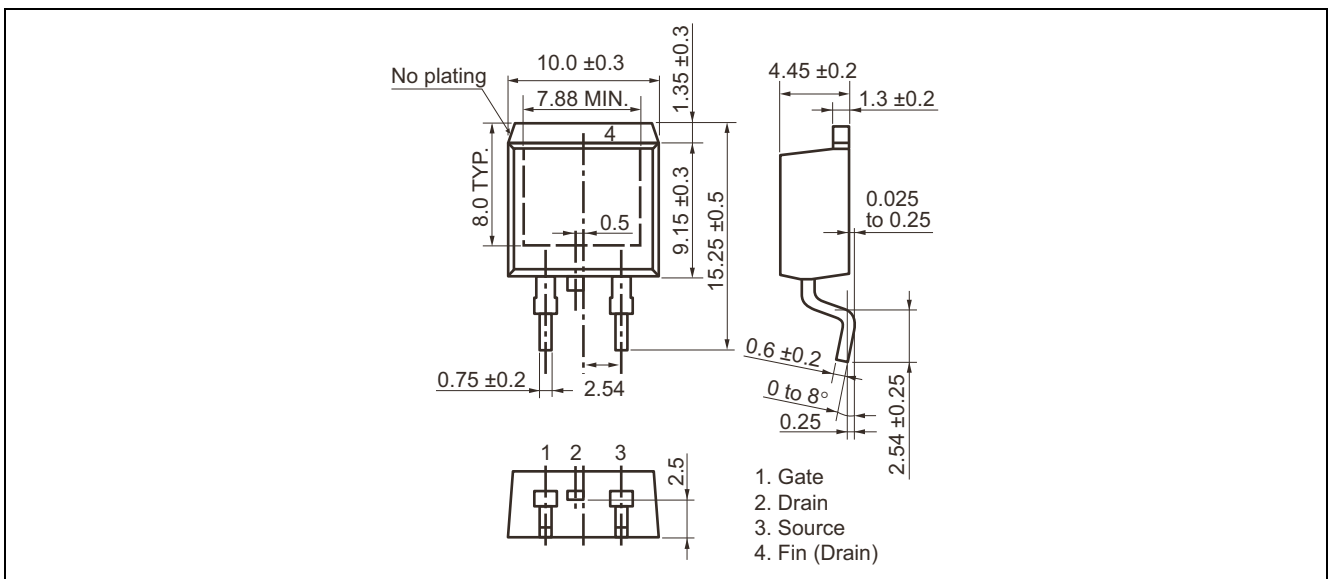


## Package Drawing (Unit: mm)

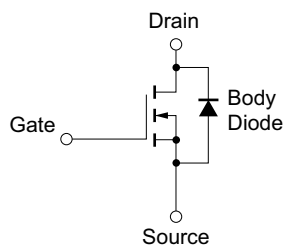
TO-252 (MP-3ZP) (Mass: 0.3 g TYP.)



TO-263 (MP-25ZP) (Mass: 1.48 g TYP.)



## Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



|                         |                                          |
|-------------------------|------------------------------------------|
| <b>Revision History</b> | <b>NP45N06VUK, NP45N06PUK Data Sheet</b> |
|-------------------------|------------------------------------------|

| Rev. | Date         | Description |                      |
|------|--------------|-------------|----------------------|
|      |              | Page        | Summary              |
| 1.00 | Nov 20, 2012 | —           | First Edition Issued |
| 2.00 | May 24 ,2018 | 1           | Note 3 was added     |
|      |              | 2           | Note 2 was added     |

|                                                                                       |
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(Rev.4.0-1 November 2017)



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