

NP109N04PUK

R07DS0544EJ0200

Rev. 2.00

May 24, 2018

MOS FIELD EFFECT TRANSISTOR

Description

NP109N04TUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
 $R_{DS(on)} = 1.75 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 55 \text{ A)}$
- Low Ciss Ciss = 7200 pF TYP. ($V_{DS} = 25 \text{ V}$)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP109N04PUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263(MP-25ZP)
NP109N04PUK-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (TA=25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25 \text{ }^\circ\text{C}$)	$I_{D(DC)}$	± 110	A
Drain Current (pulse) *1, 3	$I_{D(pulse)}$	± 440	A
Total Power Dissipation ($T_C = 25 \text{ }^\circ\text{C}$)	P_{T1}	250	W
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 175	$^\circ\text{C}$
Repetitive Avalanche Current *2, 3	I_{AR}	56	A
Repetitive Avalanche Energy *2, 3	E_{AR}	313	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}^{*3}$	0.60	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}^{*3}$	83.3	$^\circ\text{C/W}$

Notes *1. $T_C = 25 \text{ }^\circ\text{C}$, $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. $R_G = 25 \text{ } \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

*3. Not subject of production test. Verified by design/characterization.

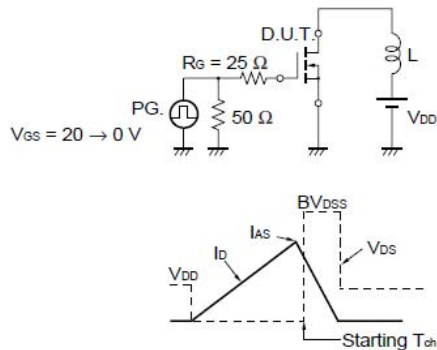
Electrical Characteristics (T_A=25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 40 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	V _{GS} = ± 20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	3.0	4.0	V	V _{DS} = V _{GS} , I _D = 250 μA
Forward Transfer Admittance *1	y _{fs}	50	100		S	V _{DS} = 5 V, I _D = 55 A
Drain to Source On-state Resistance *1	R _{DS(on)}		1.40	1.75	mΩ	V _{GS} = 10 V, I _D = 55 A
Input Capacitance *2	C _{iss}		7200	10800	pF	V _{DS} = 25 V V _{GS} = 0 V f = 1 MHz
Output Capacitance *2	C _{oss}		1040	1560	pF	
Reverse Transfer Capacitance *2	C _{rss}		390	710	pF	
Turn-on Delay Time *2	t _{d(on)}		30	70	ns	V _{DD} = 20 V, I _D = 55 A V _{GS} = 10 V R _G = 0 Ω
Rise Time *2	t _r		16	40	ns	
Turn-off Delay Time *2	t _{d(off)}		105	210	ns	
Fall Time *2	t _f		13	40	ns	
Total Gate Charge *2	Q _G		126	189	nC	V _{DD} = 32 V V _{GS} = 10 V I _D = 110 A
Gate to Source Charge	Q _{GS}		32		nC	
Gate to Drain Charge	Q _{GD}		31		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 110 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		62		ns	I _F = 110 A, V _{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		110		nC	

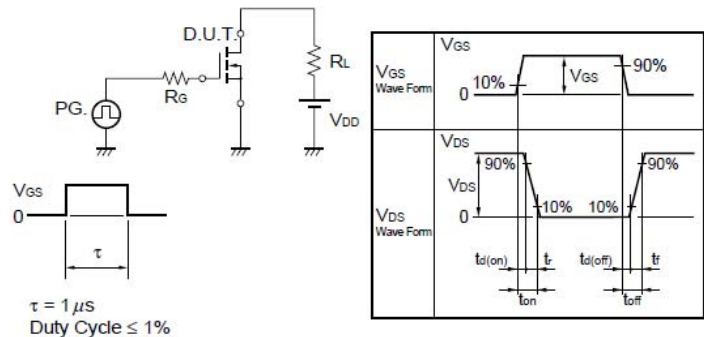
Note. *1 Pulse test

Note. *2 Not subject of production test. Verified by design/characterization.

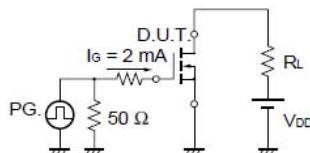
TEST CIRCUIT 1 AVALANCHE CAPABILITY

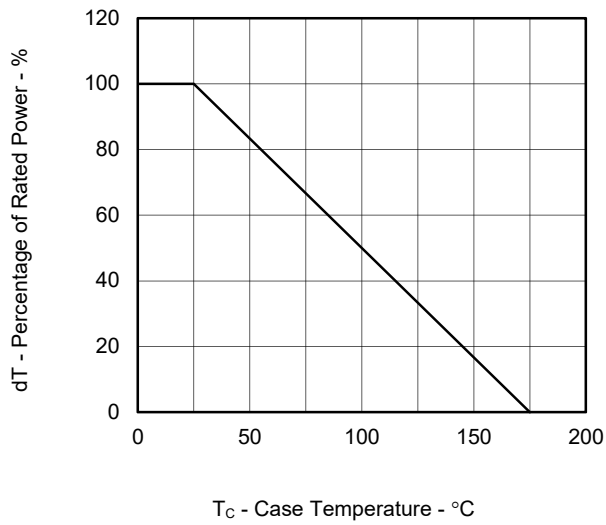
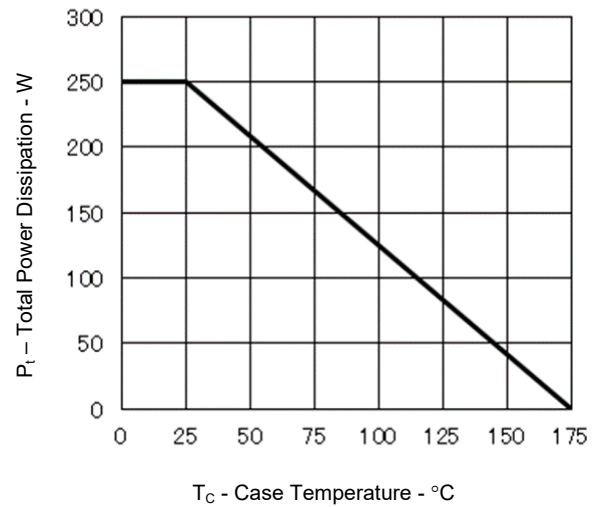


TEST CIRCUIT 2 SWITCHING TIME

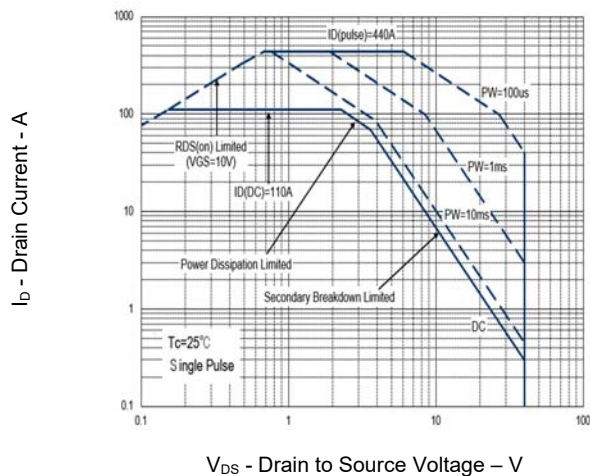


TEST CIRCUIT 3 GATE CHARGE

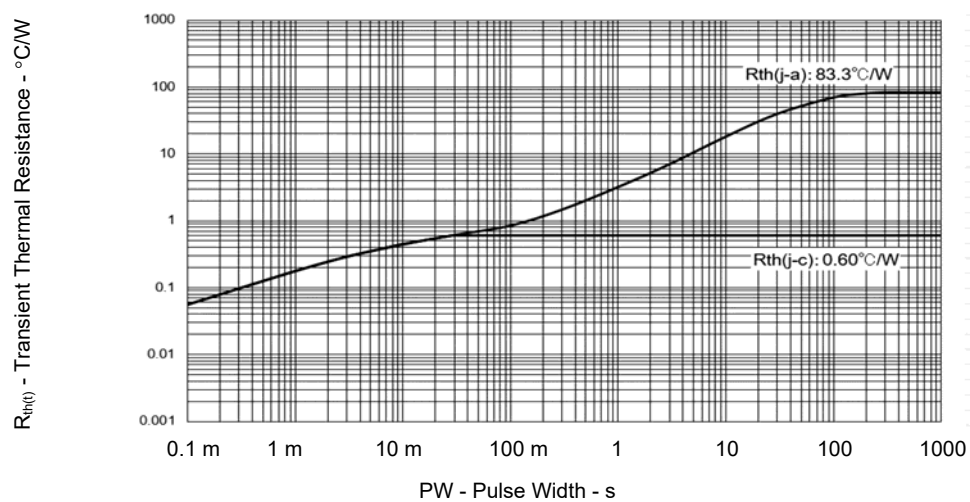


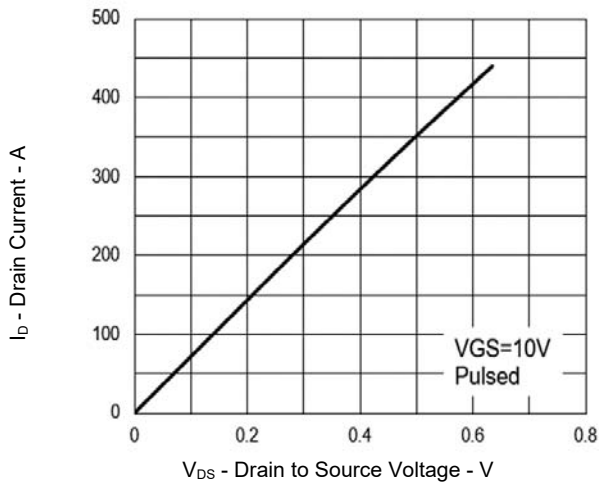
DERATING FACTOR OF FORWARD BIAS SAFE
OPERATING AREATOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

FORWARD BIAS SAFE OPERATING AREA

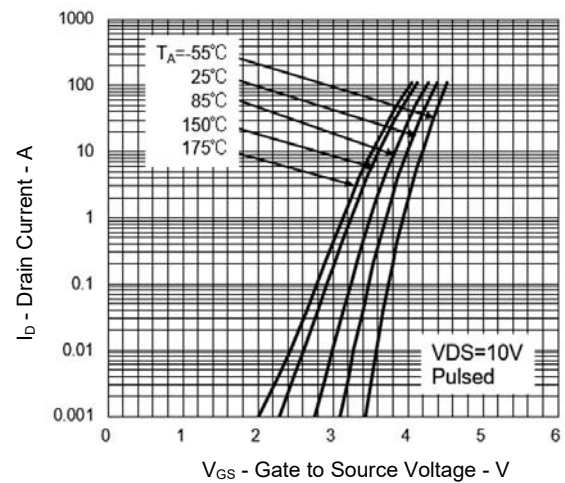
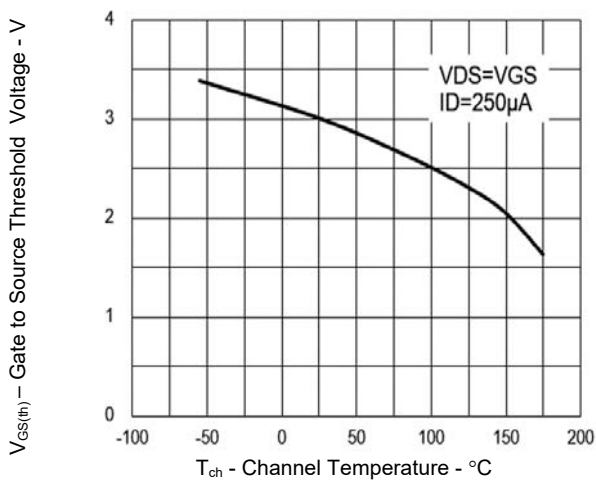
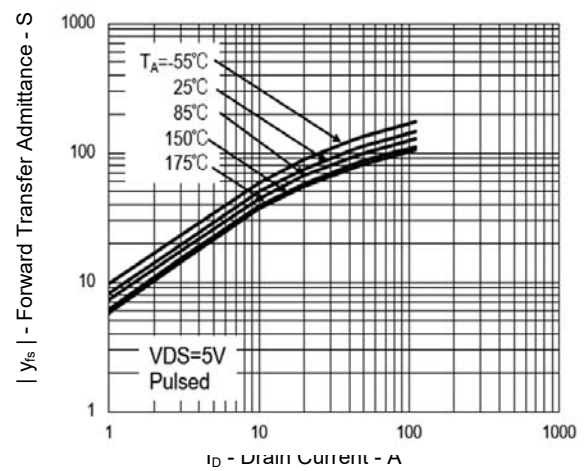
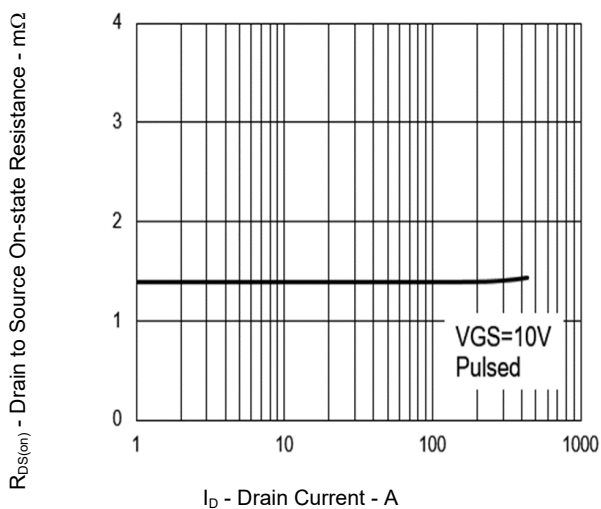
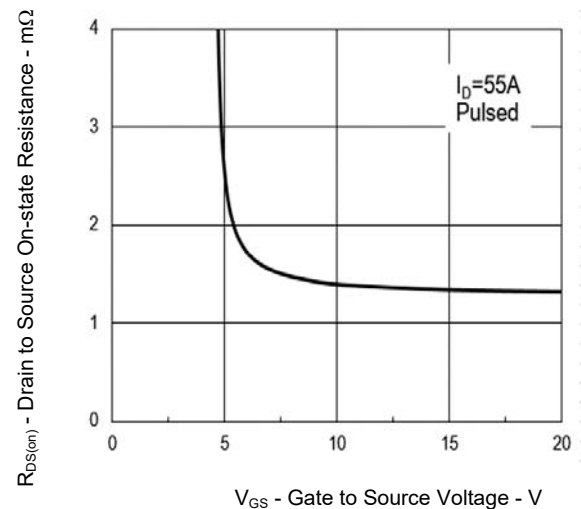


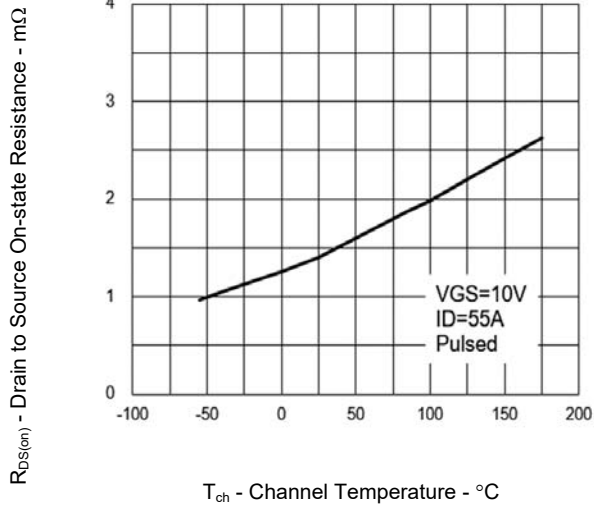
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



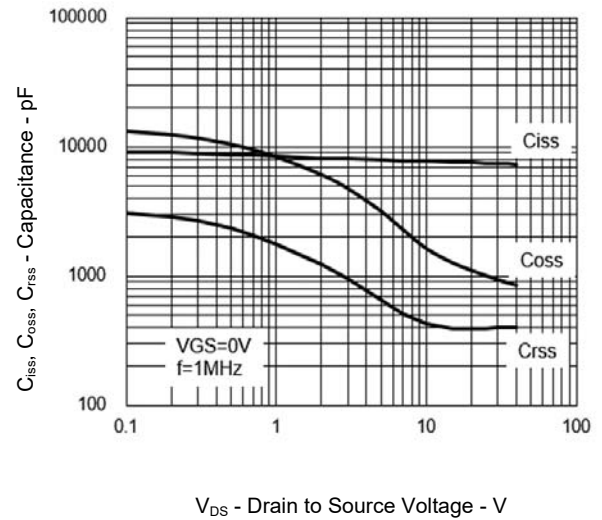
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

FORWARD TRANSFER CHARACTERISTICS

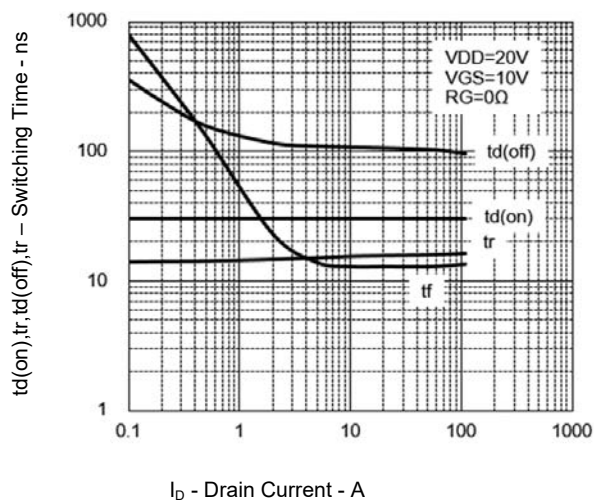
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE

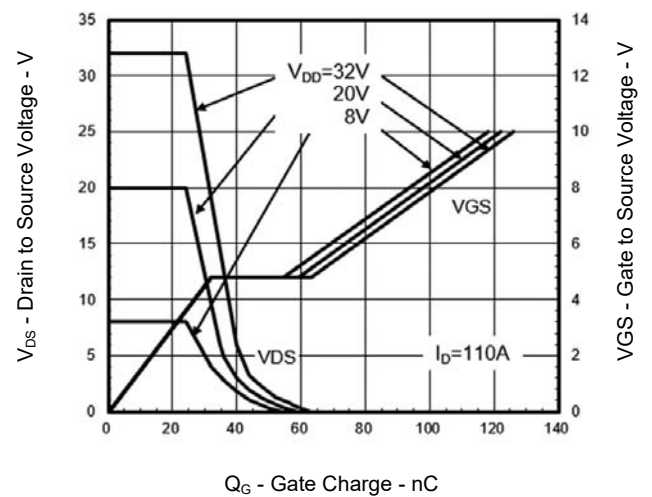
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



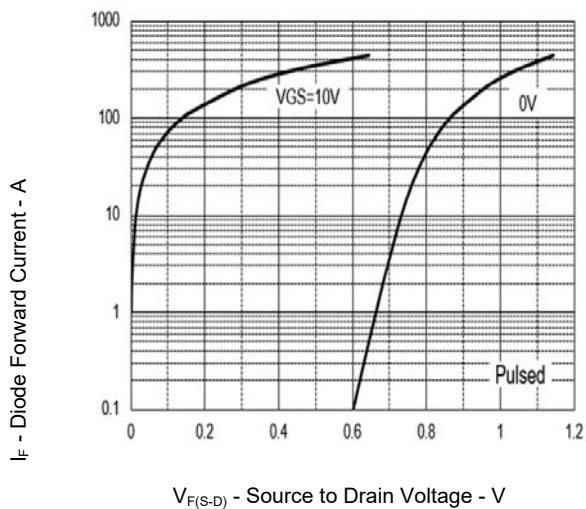
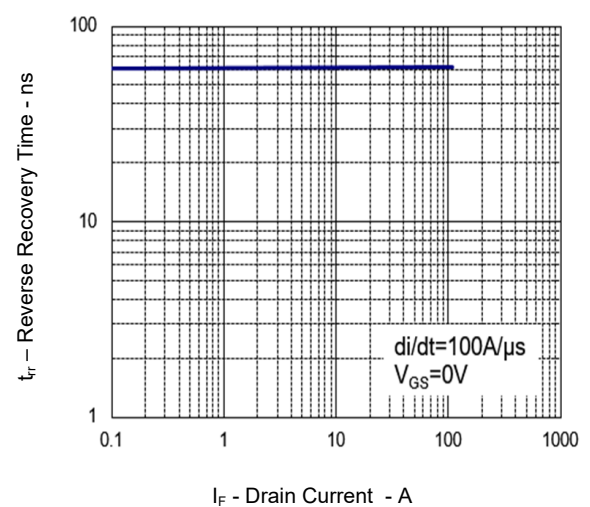
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

REVERSE RECOVERY TIME vs.
DRAIN CURRENT

Package Dimensions

Package Name	MASS (Typ.)	Unit : mm
TO-263 (MP-25ZP)	1.5 g	

Top view dimensions: 10.0 ±0.3, 7.88 MIN., 8.0 TYP., 0.5, 9.15 ±0.3, 1.35 ±0.3, 15.25 ±0.5, 0.75 ±0.2, 2.54.

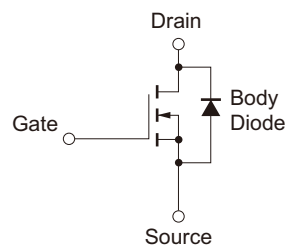
Side view dimensions: 4.45 ±0.2, 1.3 ±0.2, 0.025 to 0.25, 0.6 ±0.2, 0 to 8°, 0.25, 2.54 ±0.25.

Pin detail view dimensions: 2.5.

Legend:

- 1. Gate
- 2. Drain
- 3. Source
- 4. Fin (Drain)

Note: No plating



Equivalent circuit

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP180N04TUK Preliminary Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Apr 26, 2010	-	1st edition
2.00	May 24 ,2018	1	Note 3 was added
		2	Note 2 was added

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