

NP75P04YLG

R07DS0183EJ0200

Rev.2.00

Mar 16, 2011

MOS FIELD EFFECT TRANSISTOR

Description

The NP75P04YLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
— $R_{DS(on)} = 9.7 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = -10 \text{ V}$, $I_D = -37.5 \text{ A}$)
— $R_{DS(on)} = 14 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = -5 \text{ V}$, $I_D = -37.5 \text{ A}$)
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP75P04YLG -E1-AY ^{*1}	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP75P04YLG -E2-AY ^{*1}			8-pin HSON, Taping (E2 type)

Note: ^{*1}. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DS}	-40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 75	A
Drain Current (pulse) ^{*1}	$I_{D(pulse)}$	± 225	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	138	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{*2}	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Single Avalanche Current ^{*3}	I_{AS}	35	A
Single Avalanche Energy ^{*3}	E_{AS}	123	mJ

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Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)}$ 1.09 $^\circ\text{C/W}$

Channel to Ambient Thermal Resistance ^{*2} $R_{th(ch-A)}$ 150 $^\circ\text{C/W}$

Notes: ^{*1}. $T_C = 25^\circ\text{C}$, $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

^{*2}. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mm

^{*3}. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -20 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = -20 \rightarrow 0 \text{ V}$

The mark <R> shows major revised points.

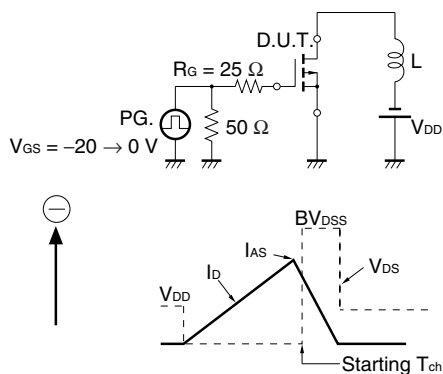
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

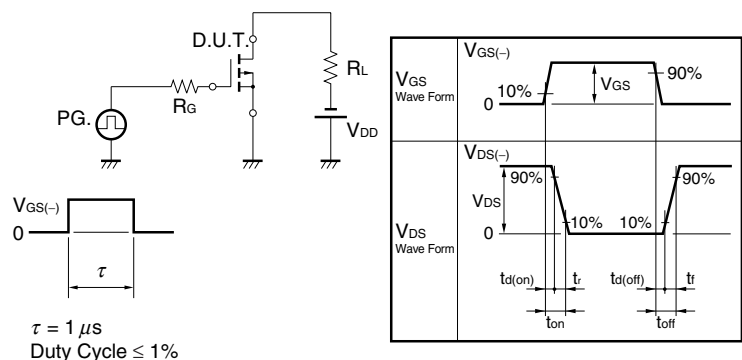
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			-1	μA	$V_{DS} = -40\text{ V}$, $V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.0	-1.7	-2.5	V	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$
Forward Transfer Admittance *1	$ y_{fs} $	31	63		S	$V_{DS} = -5\text{ V}$, $I_D = -37.5\text{ A}$
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		7.7	9.7	$\text{m}\Omega$	$V_{GS} = -10\text{ V}$, $I_D = -37.5\text{ A}$
	$R_{DS(on)2}$		9.3	14	$\text{m}\Omega$	$V_{GS} = -5\text{ V}$, $I_D = -37.5\text{ A}$
Input Capacitance	C_{iss}		3200	4800	pF	$V_{DS} = -25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		460	600	pF	
Reverse Transfer Capacitance	C_{rss}		250	450	pF	
Turn-on Delay Time	$t_{d(on)}$		12	24	ns	$V_{DD} = -20\text{ V}$, $I_D = -37.5\text{ A}$, $V_{GS} = -10\text{ V}$, $R_G = 0\text{ }\Omega$
Rise Time	t_r		11	27	ns	
Turn-off Delay Time	$t_{d(off)}$		320	640	ns	
Fall Time	t_f		180	440	ns	$V_{DD} = -32\text{ V}$, $V_{GS} = -10\text{ V}$, $I_D = -75\text{ A}$
Total Gate Charge	Q_G		91	140	nC	
Gate to Source Charge	Q_{GS}		14		nC	
Gate to Drain Charge	Q_{GD}		26		nC	$I_F = -75\text{ A}$, $V_{GS} = 0\text{ V}$
Body Diode Forward Voltage *1	$V_{F(S-D)}$		1.02	1.5	V	
Reverse Recovery Time	t_{rr}		43		ns	
Reverse Recovery Charge	Q_{rr}		57		nC	$di/dt = -100\text{ A}/\mu\text{s}$

Note: *1. Pulsed

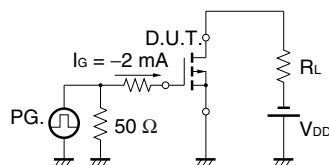
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

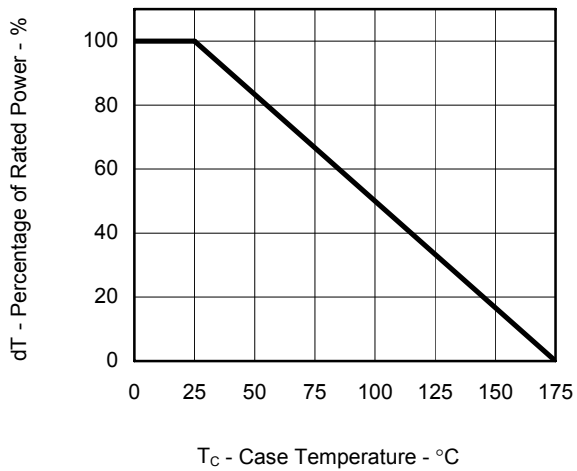


TEST CIRCUIT 3 GATE CHARGE

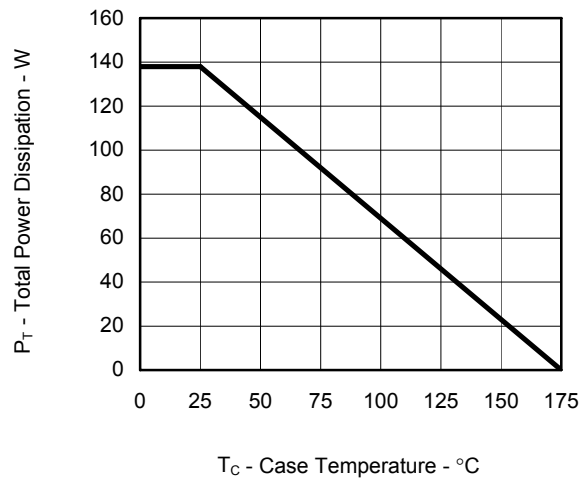


Typical Characteristics ($T_A = 25^\circ\text{C}$)

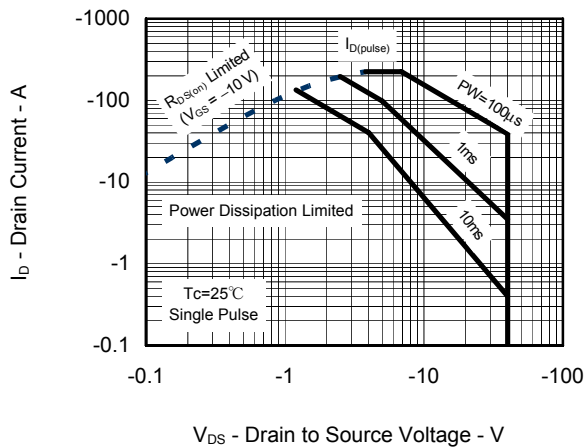
DERATING FACTOR OF FORWARD BIAS SAFE
OPERATING AREA



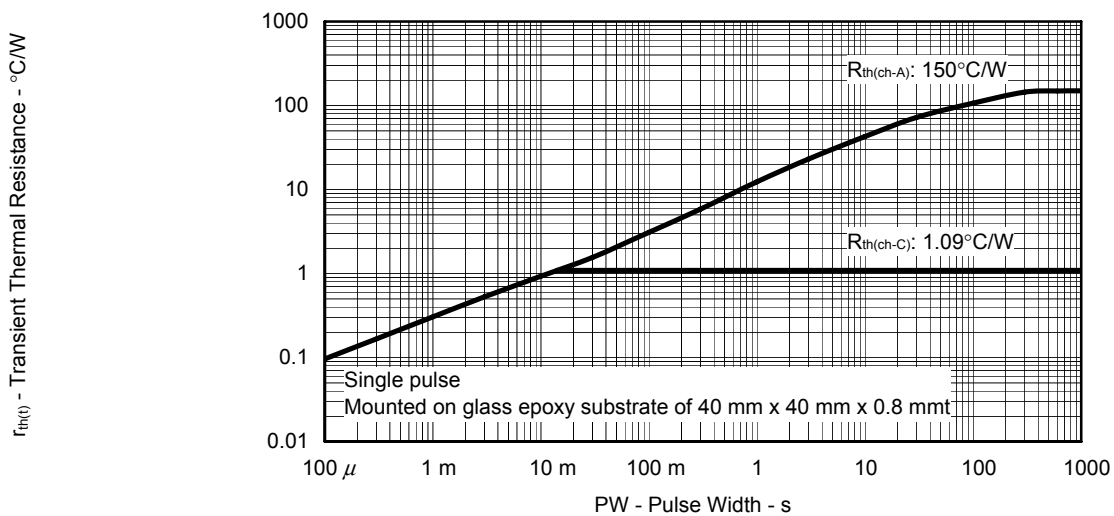
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

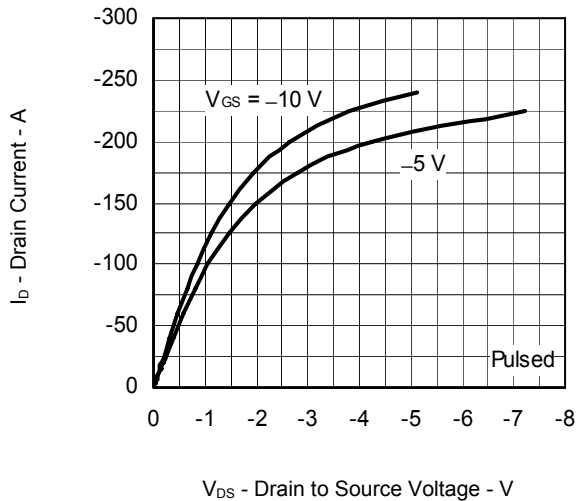


FORWARD BIAS SAFE OPERATING AREA

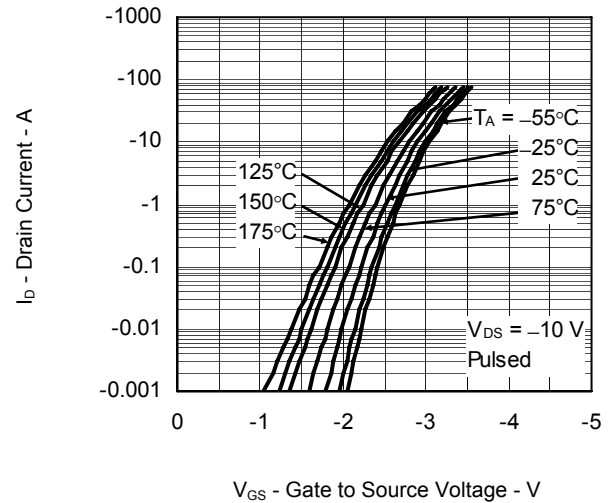
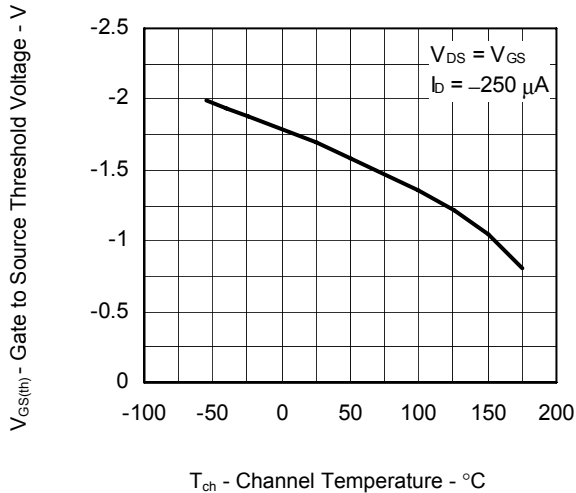
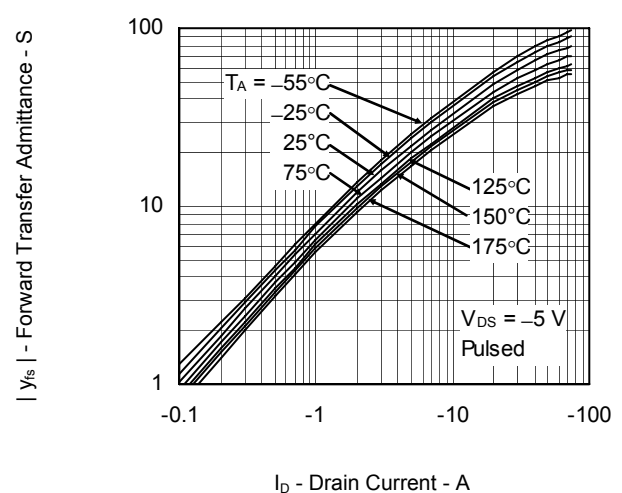
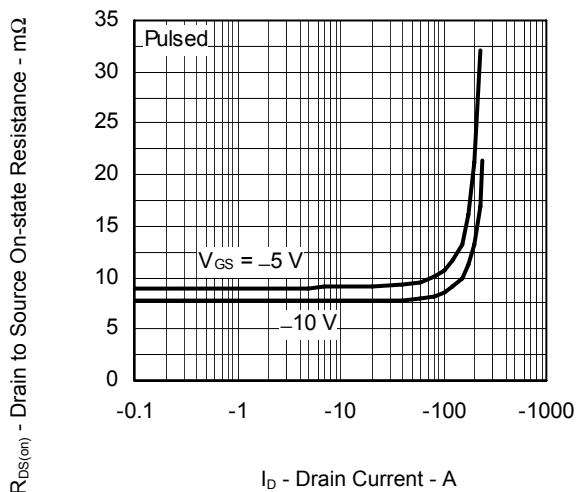
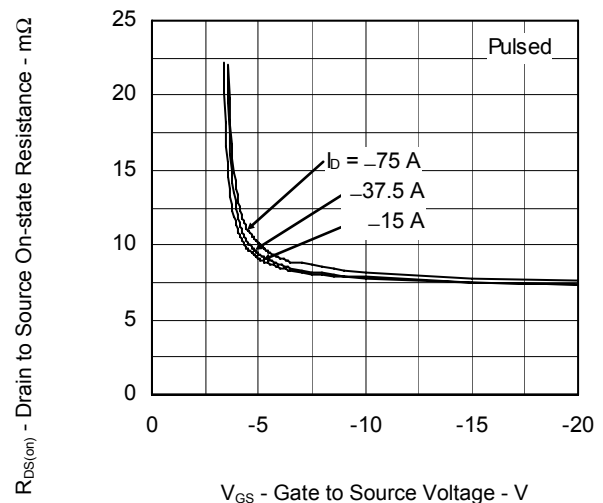


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

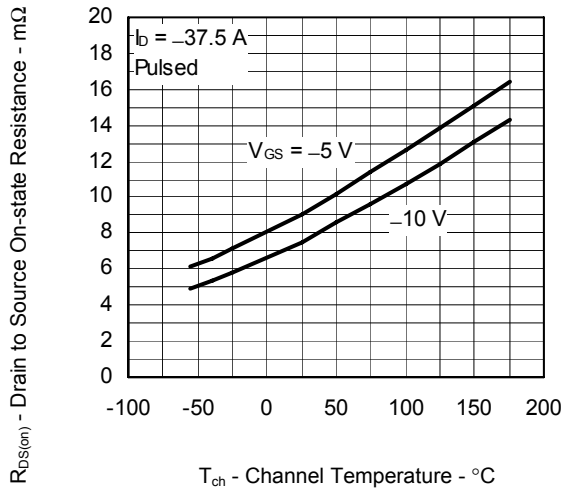


DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

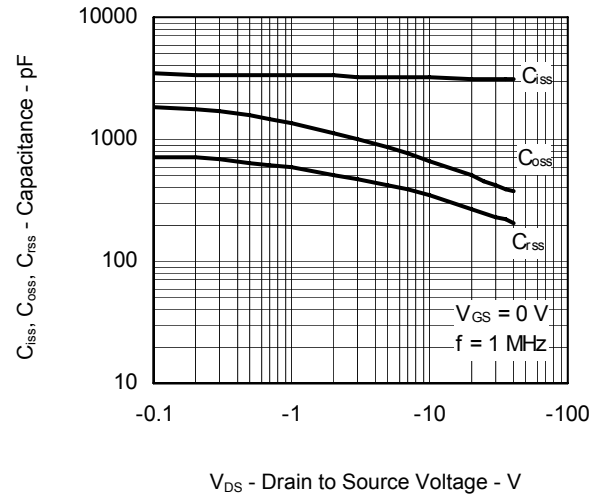
FORWARD TRANSFER CHARACTERISTICS

GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

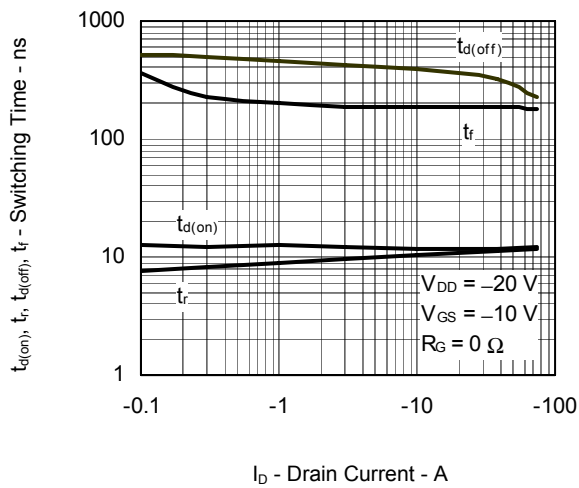
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



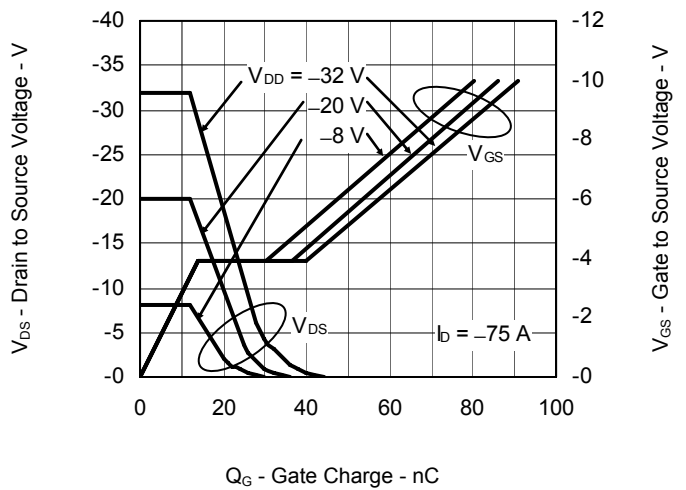
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



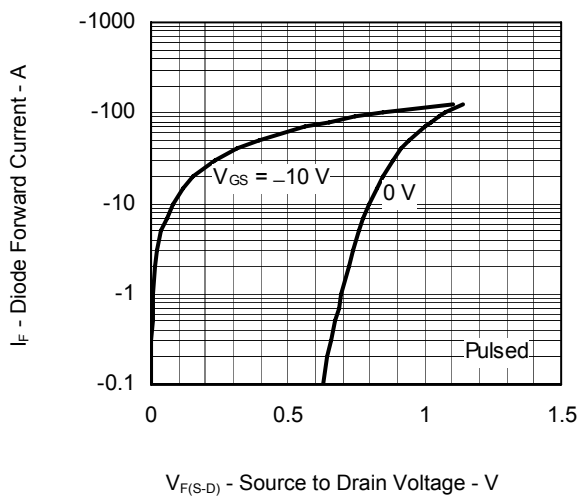
SWITCHING CHARACTERISTICS



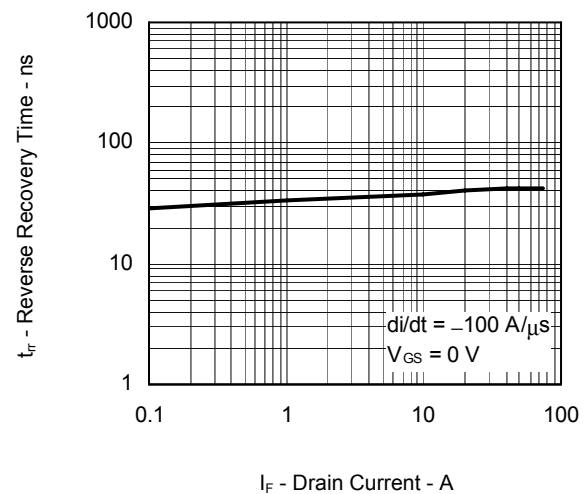
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

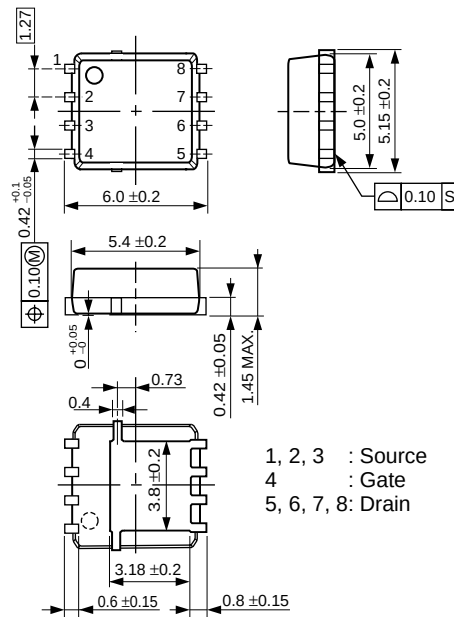


REVERSE RECOVERY TIME vs. DRAIN CURRENT

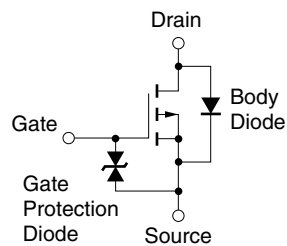


Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	NP75P04YLG Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Oct 22, 2010	–	First Edition Issued
2.00	Mar 16, 2011	p.1	Repetitive Avalanche Current -> Single Avalanche Current Repetitive Avalanche Energy -> Single Avalanche Energy Modification of Note *3

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